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Spec No: 001-44209

Spec Title: AN44209 - CAPSENSE(R) EXPRESS(TM)
POWER AND SLEEP CONSIDERATIONS

Replaced by: None

AN44209

CapSense® Express™ Power and Sleep Considerations

Author: Pramodh Prakash

Associated Project: No

Associated Part Family: CY8C201xx

Software Version: PSoC Designer™ 5.0 SP6

Related Application Notes: [AN42137](#)

To get the latest version of this application note, or the associated project file, please visit <http://www.cypress.com/go/AN44209>.

This application note describes the different power and sleep operation modes supported by CapSense® Express™. It also explores the power consumption of the device in these modes.

Contents

1	Introduction.....	1	3.5	Configuring Deep Sleep Mode in End System Boards.....	10
2	Operation Modes.....	2	3.6	Bi-Directional Sleep Control Pin Configuration ..	10
2.1	Active Mode.....	2	3.7	Registers Related to Sleep Operation	12
2.2	Sleep Mode.....	2	4	Summary.....	14
2.3	Deep Sleep Mode.....	2		Document History.....	15
3	Configuring Sleep and Deep Sleep Modes using CapSense Express.....	3		Worldwide Sales and Design Support.....	16
3.1	Configuring Sleep Mode in Software Tool.....	3		Products.....	16
3.2	Saving Sleep Mode Configuration to Flash.....	5		PSoC® Solutions	16
3.3	Configuring Sleep Mode in End System Boards	6		Cypress Developer Community.....	16
3.4	Configuring Deep Sleep Mode in the Software Tool	7		Technical Support	16

1 Introduction

The CY8C201xx CapSense Express is a family of low-power, I²C configurable CapSense controllers.

These controllers have three operation modes namely Active, Sleep, and Deep Sleep, which help to optimize device power consumption.

This application note describes these operation modes and explains how to configure the operation modes using PSoC Designer 5.0 SP6.

2 Operation Modes

CapSense Express devices are configured to operate in any of the following three modes to meet different power consumption requirements:

- Active Mode
- Sleep Mode
- Deep Sleep Mode

2.1 Active Mode

In the active mode, all the device blocks including the CapSense subsystem are powered. Typical active current consumption of the device across the operating voltage range is 1.5 mA.

2.2 Sleep Mode

Sleep mode provides an intermediate power operation mode. It is enabled by configuring the corresponding device register. When enabled, the device enters sleep mode and wakes up after a specified sleep interval. It scans the capacitive sensors before going back to sleep again. The device can also wake up from sleep mode with a GPIO interrupt.

The following sleep intervals are supported in CapSense Express. The sleep interval is configured through registers.

- 1.95 ms (512 Hz)
- 15.6 ms (64 Hz)
- 125 ms (8 Hz)
- 1 s (1 Hz)

Table 1 captures the values of current consumption in the sleep mode for different sleep intervals with the CapSense block enabled. These are typical values from an example CapSense Express board with five I/Os enabled as CapSense inputs.

Table 1. Sleep Current Consumption at 5 V

Sleep Interval	Current
1.95 ms	2.3 mA
15.6 ms	650 μ A
125 ms	200 μ A
1 s	33 μ A

With the CapSense block disabled (no pin configured as CapSense input), the sleep current consumption for 1 s sleep interval is measured as 4.7 μ A.

2.3 Deep Sleep Mode

Deep sleep mode provides the lowest power operation. In this mode, the device is woken up only using an external GPIO interrupt. A sleep timer interrupt cannot wake up the device from deep sleep mode. This is effectively a continuous sleep mode as there are no periodic wakeups.

The current consumption in deep sleep mode is measured as 4 μ A.

3 Configuring Sleep and Deep Sleep Modes using CapSense Express

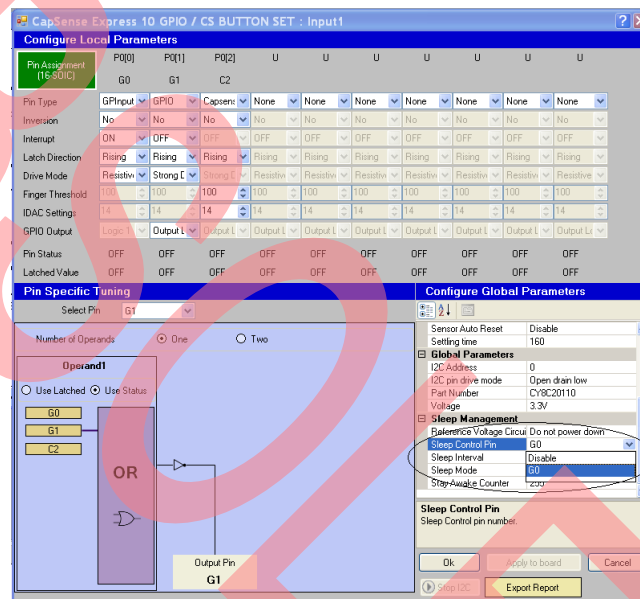
A CapSense Express software driver is supported in PSoC® Designer™ 5.0. This software tool is used to configure the CapSense Express devices for various options including sleep modes. Refer to the application note [AN42137](#) for details on using this tool.

3.1 Configuring Sleep Mode in Software Tool

Figure 1 to Figure 6 illustrate the steps involved in setting up the sleep mode configuration.

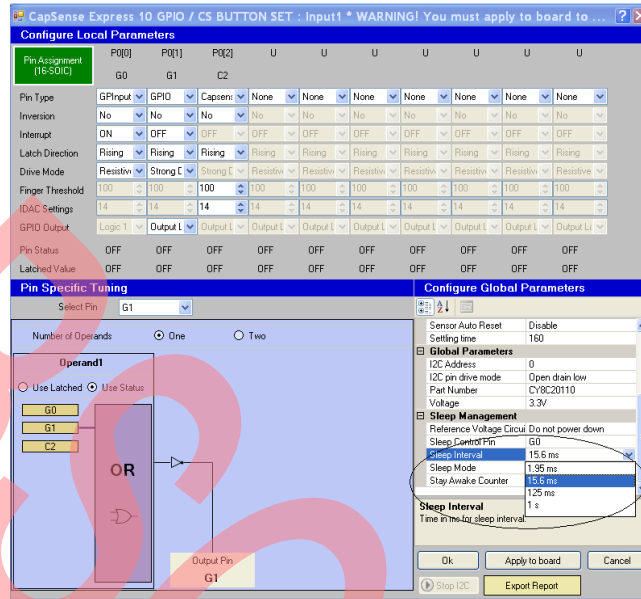
1. Select a sleep control pin to successfully put the device into sleep mode. Only pins that have the “GPIInput” type in the software tool are available for selection as a sleep control pin (“G0” in Figure 1). When selected, the interrupt property for the pin is enabled automatically.

Figure 1. Select a Sleep Control Pin



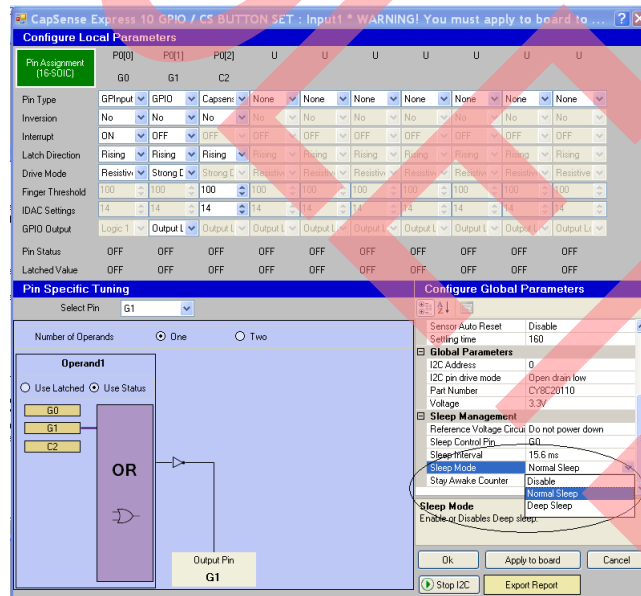
- Select one of the four available sleep interval options.

Figure 2. Select a Sleep Interval



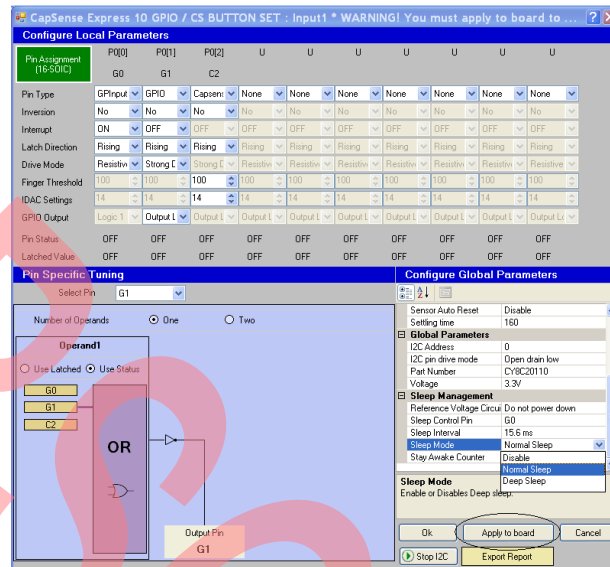
- Select the “Normal Sleep” option.

Figure 3. Select Normal Sleep Mode



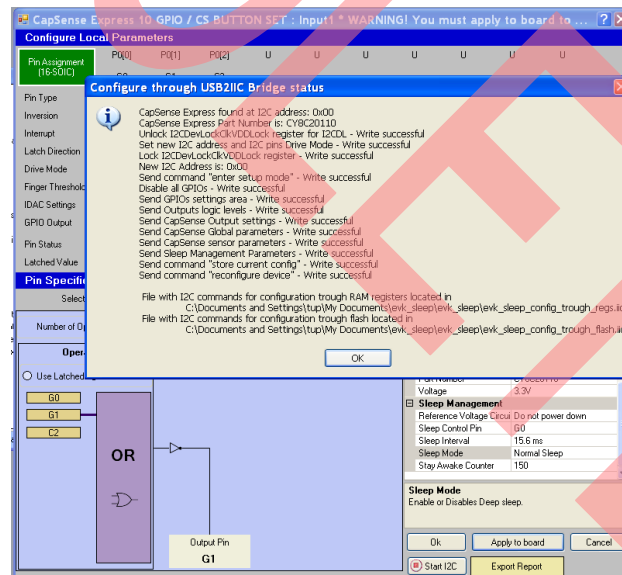
4. Download configuration to the board by clicking the “Apply to board” button.

Figure 4. Download Configuration



5. When step 4 is executed, two .IIC files containing the I²C commands for this configuration are generated. A popup window (Figure 5) shows whether the configuration is downloaded successfully and where the .IIC files are located.

Figure 5. Configuration Window



3.2 Saving Sleep Mode Configuration to Flash

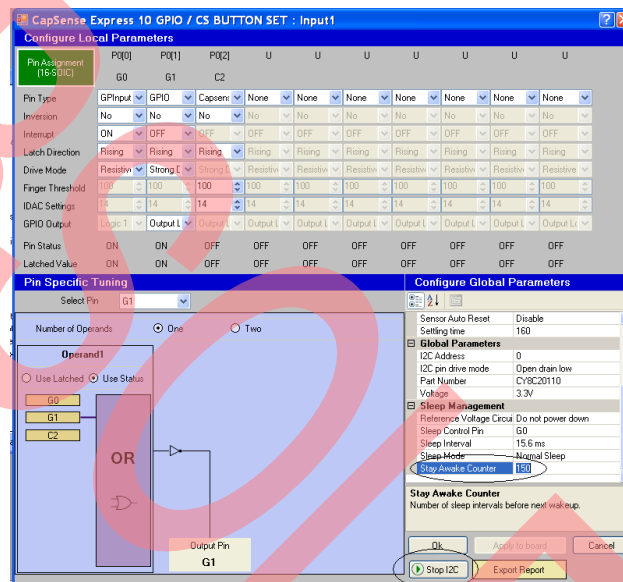
The configuration is written to the device as a series of I²C commands from the .IIC files. The “Enable Sleep I²C” command is executed before the “Save Configuration to Flash” command. When the Enable Sleep command is executed, the device enters sleep mode. Therefore, the Save Configuration to Flash command is not executed.

To overcome this, the Stay Awake Counter (Figure 6) must be set to a value in the range of 100 to 255. This counter ensures that the device does not enter sleep mode for a minimum duration of (sleep interval)*(Stay Awake Counter) after the execution of the Enable Sleep command. This gives enough time to save the configuration to flash.

Also, continuous I²C communication with the device must be stopped (by clicking the “Stop I2C” button in Figure 4) when downloading the configuration. This is because the software cannot control the sleep control pin and results in unreliable I²C communication after downloading the configuration. The device enters a sleep state periodically (if the sleep control pin is high). The I²C communication is not reliable if the device is in sleep mode. Therefore, stopping the I²C solves the problem.

To perform tuning and monitoring, I²C communication should be started. Make sure that the sleep control pin is pulled low during the process.

Figure 6. Set Stay Awake Counter and Stop I2C



3.3 Configuring Sleep Mode in End System Boards

The previous section illustrated steps to successfully set up a sleep mode configuration using the CapSense Express software tool. The same can be mapped to an end system.

Configure sleep mode by sending I²C commands from a host to the CapSense Express device on the end application board.

- Select a sleep control pin.
- Select a sleep interval.
- Set a Stay Awake Counter value depending on the design requirement.
- Pull the sleep control pin LOW and send the I2C command to Enable Sleep mode.
- Reset the sleep control pin to HIGH.

The device enters sleep mode after (sleep interval)*(Stay Awake Counter) duration of inactivity.

Configure sleep mode using the .IIC file generated with the software tool.

- Select a sleep control pin in the software tool.
- Select a sleep interval.
- Set a Stay Awake Counter value depending on the design requirement.

- Select the Normal Sleep option.
- Generate the .IIC configuration file by clicking the “Apply to board” button.

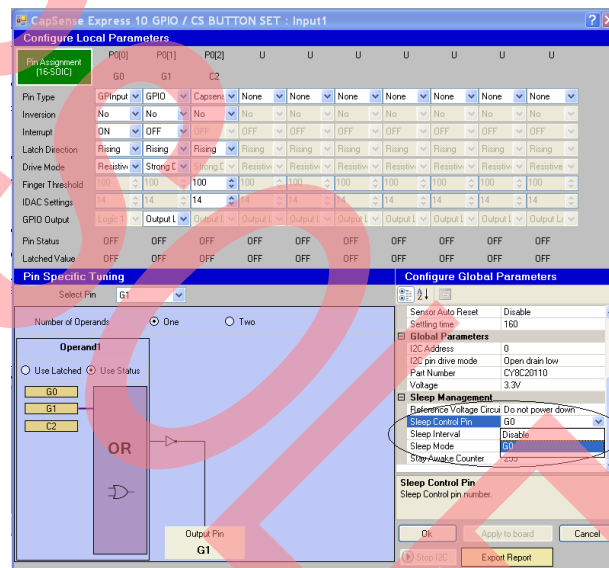
As shown in Figure 5, two .IIC files are generated. The second .IIC file uses an I²C command which writes the configuration to flash in the inactive mode. The registers are written with the values in the I²C commands but are not executed. Hence, the device does not enter sleep mode before saving the configuration. This .IIC file is used to configure all CapSense Express devices before mounting them on the end application board.

3.4 Configuring Deep Sleep Mode in the Software Tool

Figure 7 to Figure 12 illustrate the steps involved to set up the deep sleep mode configuration.

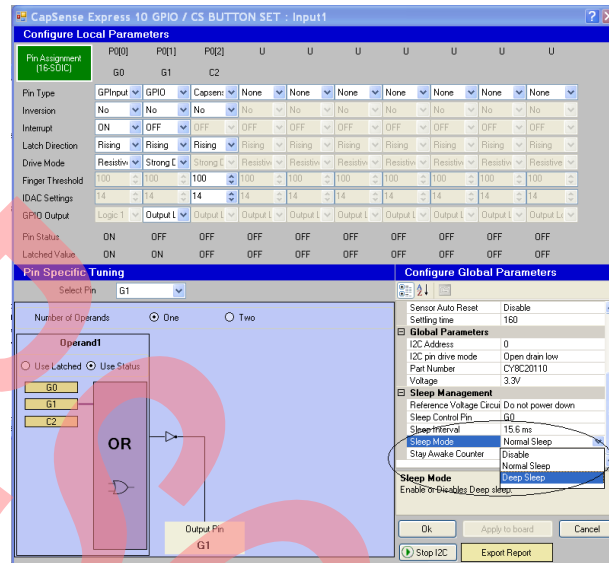
1. Select a sleep control pin to put the device into deep sleep mode. Only pins that have the type “GPInput” in the software tool are available for selection as a sleep control pin (“G0” in Figure 7). When selected, the interrupt for the pin is enabled automatically.

Figure 7. Select a Sleep Control Pin



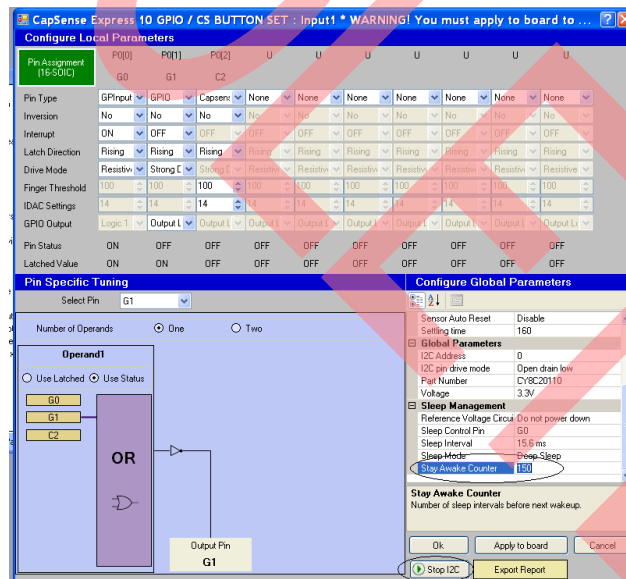
2. Select the “Deep Sleep” option.

Figure 8. Select Deep Sleep Mode



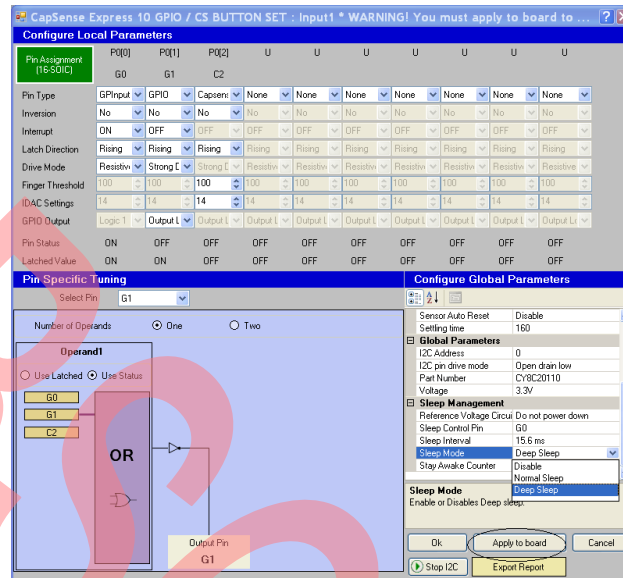
3. Set the Stay Awake Counter and Stop I2C before downloading configuration.

Figure 9. Stay Awake Counter and Stop I2C



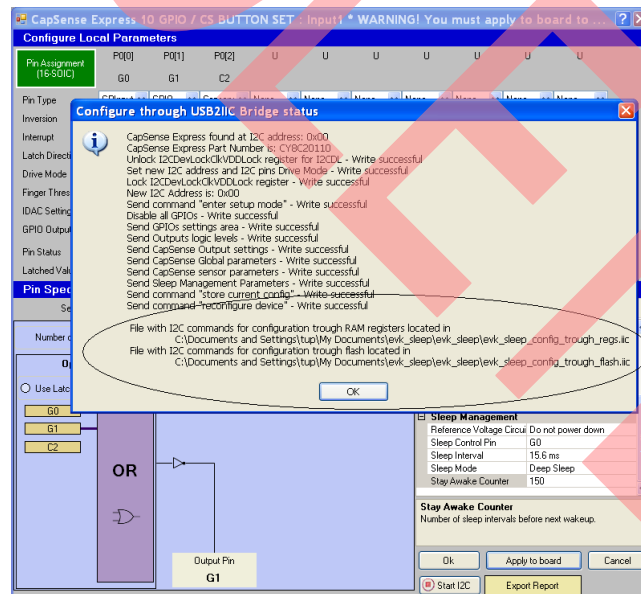
- Download the configuration to the board by clicking the “Apply to board” button.

Figure 10. Download Configuration



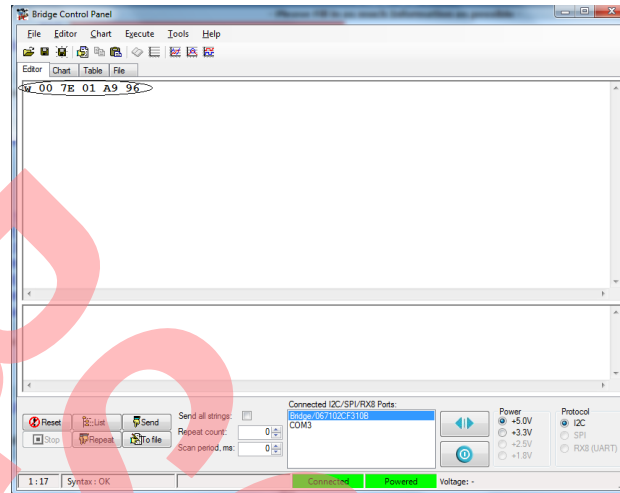
- When step 4 is executed, two .IIC files containing the I²C commands for this configuration are generated. A popup window (Figure 11) shows whether the configuration is downloaded successfully and where the .IIC files are located.

Figure 11. Configuration Window



- Open Bridge Control Panel (Start > All Programs > Cypress > Bridge Control Panel) and execute the Enable Deep Sleep I²C command “W 00 7E 01 A9 96” as shown in Figure 12.

Figure 12. Execute Enable Deep Sleep Command from Bridge Control Panel Software



Successful download of the configuration from the software tool does not enable the deep sleep mode.

In deep sleep mode, the device sleeps continuously (no scanning is performed) drawing the lowest possible current. Ensure that the device never wakes up (on power on or reset) in the deep sleep mode.

Only “Normal Sleep” is allowed at power on or reset. Deep sleep mode must be consciously enabled by the master (host) device that controls the CapSense Express device. To facilitate this, saving deep sleep mode configuration to flash is not allowed.

When step 4 is executed, the configuration is downloaded to flash. However, the deep sleep mode is not enabled (its corresponding bit in the register is not set). Hence, the device wakes up with the previous configuration.

To enable deep sleep mode, open the .IIC file located in the project directory (Figure 11) using Bridge Control Panel software and execute the I²C command (Figure 12). When this command is executed, the device enters deep sleep mode and can be woken up only by an external GPIO interrupt.

3.5 Configuring Deep Sleep Mode in End System Boards

The previous section illustrated steps to successfully set up a deep sleep mode configuration using the CapSense Express software tool and Bridge Control Panel software. On an end system board, the deep sleep mode is consciously enabled by the host according to the application requirement. Before enabling, the host must perform the following steps by sending the corresponding I²C commands.

- Select a sleep control pin.
- Set the Stay Awake Counter value depending on the design requirement.

Enable deep sleep mode by sending the I²C command to write the Enable Deep Sleep bit in the CapSense Express register.

3.6 Bi-Directional Sleep Control Pin Configuration

The sleep control pin is a dedicated pin to enable sleep and deep sleep modes and to ensure reliable I²C communication. It results in the user having one less GPIO for either CapSense or GPIO functions. One of the frequently used GPIO functions is to configure a GPIO as an interrupt output pin to the host controller to signal the finger press on any CapSense button.

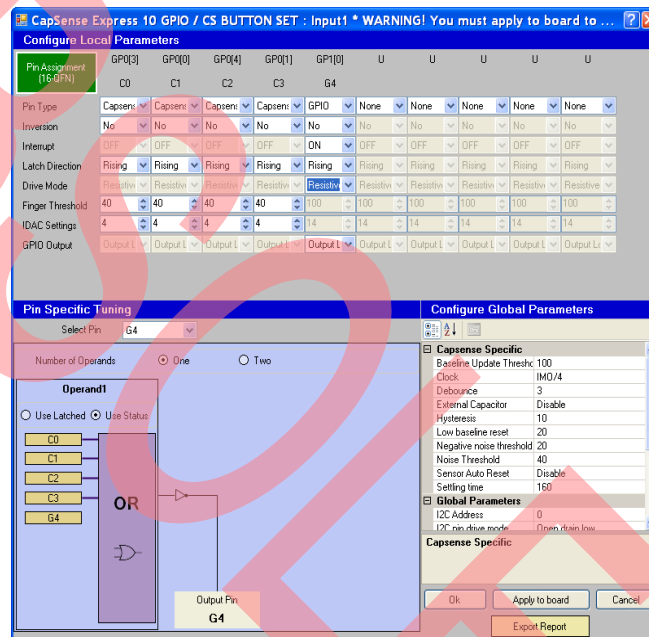
Users may prefer to use the same pin for sleep control and interrupt output function. If another pin is used for the interrupt feature, less number of pins are available for CapSense and other GPIO functions such as LED drive.

The current CapSense Express software tool supports only the “GPInput” mode for sleep control pin by default. To use the same sleep control pin for interrupt output feature, the pin needs to support the bi-directional drive feature. The bi-directional configuration for sleep control and interrupt output feature cannot be enabled using the CapSense Express software tool. This must be done using the Bridge Control Panel software.

The following example shows how to configure a CapSense Express part with four CapSense inputs and sleep mode enabled using one bi-directional pin for both sleep control and interrupt output functions. Here, GP10 is used as the sleep control pin and interrupt output pin, which is driven LOW when any of the four CapSense Inputs are activated.

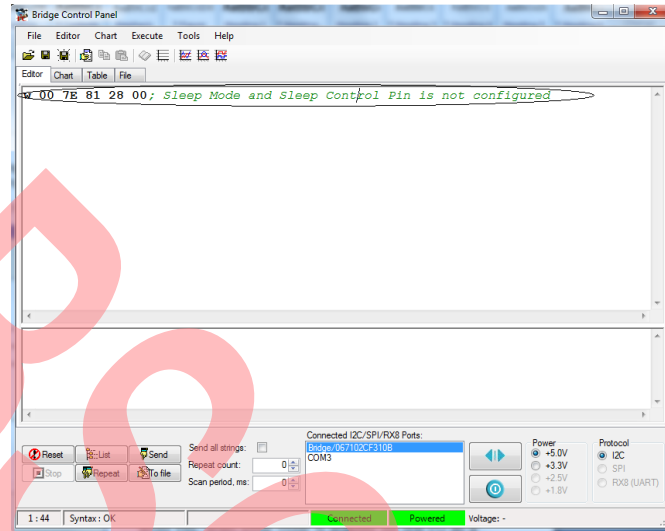
1. Configure the four CapSense inputs (GP00, GP01, GP03, and GP04) and GP10 with Pin Type as “GPIO”, Drive Mode as “Resistive Pull Up”, and GPIO Output as “Output Logic Operation”. Set the Logic Operation as shown in Figure 13 with GP10 being driven LOW when any of the CapSense inputs are activated. GP10 is also used as sleep control pin, but this configuration and enabling sleep mode is done using the Bridge Control Panel software.

Figure 13. Configuring CapSense, GPIO, and Logic Operation



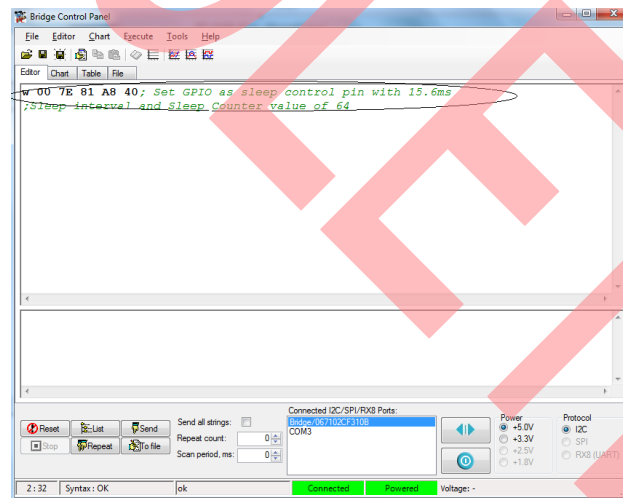
- Download the configuration by clicking “Apply to board”. Open Bridge Control Panel (**Start > All Programs > Cypress > Bridge Control Panel**).

Figure 14. Bridge Control Panel with Sleep Mode and Sleep Control Pin Configuration Commands



- Enable the sleep mode, configure the sleep control pin, set the sleep interval, and sleep counter values by writing to the corresponding registers in the Bridge Control Panel software with the following command “W 00 7E 81 28 00” as shown in Figure 14.

Figure 15. Configure Sleep Mode, Set Sleep Control Pin, and other Sleep Parameters



After executing step 3, GP10 is configured as a sleep control pin. GP10 is now a bi-directional pin capable of generating an interrupt output when any CapSense input is activated. It also acts as the sleep control input pin to the CapSense Express device. This is done by executing the command “W 00 7E 81 A8 40” as shown in Figure 15.

3.7 Registers Related to Sleep Operation

The registers related to sleep mode control and operation in the CapSense Express register map are 7Eh, 7Fh, and 80h.

3.7.1 Sleep Control Pin Register (7Eh)

This register is used to select the pin to control safe I²C communication when sleep mode is enabled.

Table 2. Register 7Eh—Sleep Control Pin Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Port	N/A	N/A	GPX[4]	GPX[3]	GPX[2]	GPX[1]	GPX[0]

The sleep mode forces the I²C block also to sleep. Therefore, when the device is in sleep mode an I²C communication results in unreliable I²C data transfers. To avoid this, when sleep mode is enabled set one I/O as a control pin for proper I²C communication. The host pulls the selected pin LOW before starting an I²C communication and holds it until the communication is completed. When the pin is pulled LOW, the CapSense Express device never enters into sleep mode.

Take proper care in setting the drive mode for the pin selected as sleep control pin. Typically, it is set to a bi-directional drive mode (resistive pull up or open drain low) when both master and slave must control the pin's status.

The I/O used as the sleep control pin is first enabled as a GPIO by writing to the corresponding bit in the registers 08h and 09h. The drive mode of the sleep control pin is also set by writing to the drive mode registers (10h–17h).

Table 3. Registers 08h and 09h—Port 0 and 1 GPIO Enable Registers

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
N/A	N/A	N/A	GP0[4]	GP0[3]	GP0[2]	GP0[1]	GP0[0]
N/A	N/A	N/A	GP1[4]	GP1[3]	GP1[2]	GP1[1]	GP1[0]

Table 4. Registers 10h and 13h—Port 0 Pull Up and Open Drain Low Drive Mode Registers

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
N/A	N/A	N/A	GP0[4]	GP0[3]	GP0[2]	GP0[1]	GP0[0]
N/A	N/A	N/A	GP0[4]	GP0[3]	GP0[2]	GP0[1]	GP0[0]

Table 5. Registers 14h and 17h—Port 1 Pull Up and Open Drain Low Drive Mode Registers

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
N/A	N/A	N/A	GP1[4]	GP1[3]	GP1[2]	GP1[1]	GP1[0]
N/A	N/A	N/A	GP1[4]	GP1[3]	GP1[2]	GP1[1]	GP1[0]

3.7.2 Sleep Control Register (7Fh)

This register is used to enable the sleep modes and to select different sleep intervals.

Table 6. Register 7Fh—Sleep Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Enable	N/A	Bandgap	Sleep[1:0]		N/A	N/A	Mode

The Enable bit controls whether to periodically enter into sleep mode.

The Bandgap bit controls whether to power the voltage bandgap during sleep to enable faster wakeup.

The Sleep bits are set according to this table.

Table 7. Sleep Bits

Sleep[1:0]	Sleep Interval
00	1.95 ms (512 Hz)
01	15.6 ms (64 Hz)
10	125 ms (8 Hz)
11	1s (1 Hz)

The Mode bit controls whether the deep sleep or normal sleep mode is enabled.

Setting the Mode bit to '1' enables the deep sleep mode during which only a GPIO interrupt is able to wake up the device. When awake, the device stays so for at least sleep counter (Register 80h) number of sleep interval (Sleep [1:0] bits in 7Fh) or more. If some activity is detected, the Mode bit is reset to '0' for normal sleep mode. To re-enter the deep sleep mode, the register must be written again with the Enable bit and the Mode bit set to '1'.

3.7.3 Stay Awake Counter Register (80h)

This register sets the number of sleep intervals the device stays awake, awaiting events before going into sleep again. Any new event (CapSense press or GPIO interrupt or I²C Read/Write) resets the counter to this register value.

Table 8. Register 80h—Stay Awake Counter Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]

4 Summary

CapSense Express is a low-power configurable device. The power consumption is further reduced by using the sleep and deep sleep modes supported by the device. These modes help to reduce the standby current consumption of CapSense Express devices significantly.

About the Author

Name: Pramodh Prakash.
Title: Product Mktg Engineer Sr.

Document History

Document Title: AN44209 - CapSense® Express™ Power and Sleep Considerations

Document Number: 001-44209

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2104726	TUP	02/29/08	New application note.
*A	2542831	TUP	07/24/08	Updated Configuring Sleep and Deep Sleep Modes using CapSense Express: Added Bi-Directional Sleep Control Pin Configuration.
*B	3194971	SLAN	03/14/2011	Updated Software Version as "PSoC Designer 5.0 SP6" in page 1. Updated hyperlink for Associated Application Notes in page 1.
*C	4290238	PRIA	02/24/2014	Updated to new template. Completing Sunset Review.
*D	4500920	PRIA	09/12/2014	Updated Introduction: Updated description.
*E	4622386	SSHH	01/13/2015	Replaced "USBtoI2C bridge program" with "Bridge Control Panel Software" in all instances across the document and also in figures. Updated to new template.
*F	5052963	PRIA	12/30/2015	Updated hyperlinks across the document. Updated to new template.
*G	5092581	PRIA	01/19/2016	Obsoleting the Application Note

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Cypress Semiconductor	Phone	: 408-943-2600
198 Champion Court	Fax	: 408-943-4730
San Jose, CA 95134-1709	Website	: www.cypress.com

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