AN43380

$\overline{\text{HSB}}$ Operation in nvSRAMs

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This application note describes the internal architecture and functionality of the Hardware STORE Busy ($\overline{\text{HSB}}$) pin of the Cypress nvSRAMs.

Introduction

Cypress's nonvolatile synchronous random access memory (nvSRAM) combines the best features of SRAM and EEPROM and makes it the fastest and the most reliable nonvolatile memory. Every bit of the nvSRAM is constituted by integrating a fast SRAM and a SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) nonvolatile memory. The SRAM is read from and written to it an infinite number of times, while independent nonvolatile data resides in the nonvolatile elements. Data in the SRAM is transferred to the nonvolatile cell (STORE operation) either automatically after the V_{CC} power drops below a minimum threshold level (V_{SWITCH}) or through firmware-controlled methods such as software STORE or hardware STORE (through the Hardware Store Busy ($\overline{\text{HSB}}$) pin). Data is retrieved from the nonvolatile cell to the SRAM at power-up cycle (RECALL operation).

This application note describes the internal architecture and functionalities of the $\overline{\text{HSB}}$ pin. For more details on the nvSRAM technology and functionalities, refer to the whitepaper "Nonvolatile SRAM (nvSRAM) Basics".

$\overline{\text{HSB}}$ Overview

The $\overline{\text{HSB}}$ pin of nvSRAM is a bi-directional pin and used for the following purposes:

As an output:

- Indicates that the nvSRAM is busy in executing power on boot up
- Indicates that a STORE cycle initiated by the software or the hardware pin ($\overline{\text{HSB}}$) is in progress
- Indicates that V_{CC} has dropped below the V_{SWITCH}

As an input:

- When pulled LOW externally, initiates a nonvolatile STORE operation

The $\overline{\text{HSB}}$ pin in nvSRAMs is used to control and acknowledge the STORE operations by means of a hardware pin. If either a STORE or RECALL operation is not in progress, the $\overline{\text{HSB}}$ pin can be used to trigger a hardware STORE by toggling it LOW externally. The ($\overline{\text{HSB}}$)-initiated STORE operation is an alternative to the software-initiated STORE operation, where it requires the host controller to send a specific soft sequence or a command opcode.

The $\overline{\text{HSB}}$ toggles LOW for $t_{HRECALL}$ and t_{STORE} duration during power-up and power-down cycles, which can be used to monitor the power-up and power-down events in the system.

Internal Architecture of $\overline{\text{HSB}}$ Pin

The internal architecture of the bi-directional $\overline{\text{HSB}}$ pin is shown in Figure 1. The $\overline{\text{HSB}}$ output has one strong NMOS pull-down transistor Q3 and two PMOS pull-up transistors: Q1, with standard output drive strength, and Q2, with weak output drive strength, are connected in parallel. When the $\overline{\text{HSB}}$ pin is driven LOW by the nvSRAM, it indicates that a STORE cycle is in progress. When the $\overline{\text{HSB}}$ pin is pulled LOW externally by a controller, it initiates a STORE operation and drives the $\overline{\text{HSB}}$ pin LOW and keeps it LOW until the STORE operation is completed. Similarly, when the system's V_{CC} collapses or transitions through V_{SWITCH}, the device executes AutoStore. The STORE operation, either due to the hardware pin ($\overline{\text{HSB}}$) or AutoStore will execute only if there is a WRITE to the SRAM (write latch is set) since the last STORE or RECALL operation. The controller can determine the end of the STORE cycle by monitoring the $\overline{\text{HSB}}$ pin status.

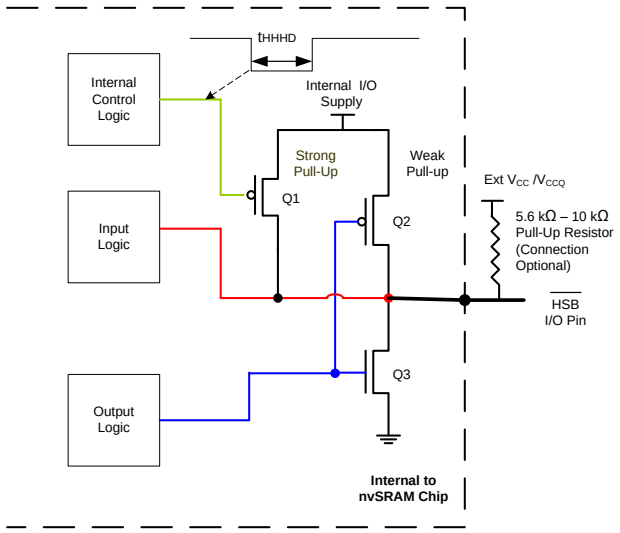
Once the STORE operation completes, the nvSRAM first drives $\overline{HSB}$ HIGH for a short duration (t_{HHHD}) by turning ON the strong pull-up driver Q1, after which Q1 turns OFF and Q2 turns ON, which keeps the $\overline{HSB}$ pin HIGH internally with a weak pull-up resistor. A strong pull-up on $\overline{HSB}$ during t_{HHHD} helps the $\overline{HSB}$ pin to quickly reach to the input HIGH voltage level (V_{IH}).

For a single power supply, the nvSRAM device where V_{CC} is used to supply power to the core and I/O blocks, Q1 and Q2 are pulled to V_{CC}. If the nvSRAM supports a dual power supply option, where it uses two power supplies to supply the power to device's core (V_{CC}) and I/O (V_{CCQ}) separately, then the Q1 and Q2 are pulled to the I/O power supply (V_{CCQ}).

Recommended $\overline{HSB}$ Configuration

If a controller I/O is connected to the $\overline{HSB}$ pin, it is recommended that $\overline{HSB}$ is pulled HIGH to V_{CC} or V_{CCQ} using an external pull-up resistor between 5.6 kΩ and 10 kΩ. This pull-up resistor will ensure that the external system I/O load on the $\overline{HSB}$ pin does not pull it below the V_{IH} level as the Q2 pull-up transistor is weak.

Figure 1. $\overline{HSB}$ Pin Architecture of nvSRAM



$\overline{HSB}$ Behavior at Power-up

During power-up, the $\overline{HSB}$ output is driven LOW after the internal POR (Power-on-Reset) is issued and remains LOW until the power-up RECALL is completed. The $\overline{HSB}$ output can glitch until internal POR is issued. The behavior of the $\overline{HSB}$ output during this period is explained as follows:

When the V_{CC} ramps up from initial voltage until it crosses a transistor threshold (V_{HDIS}) voltage, the $\overline{HSB}$ driver is off. During this time, if there is an external pull-up resistor connected on the pin, it tracks V_{CC}.

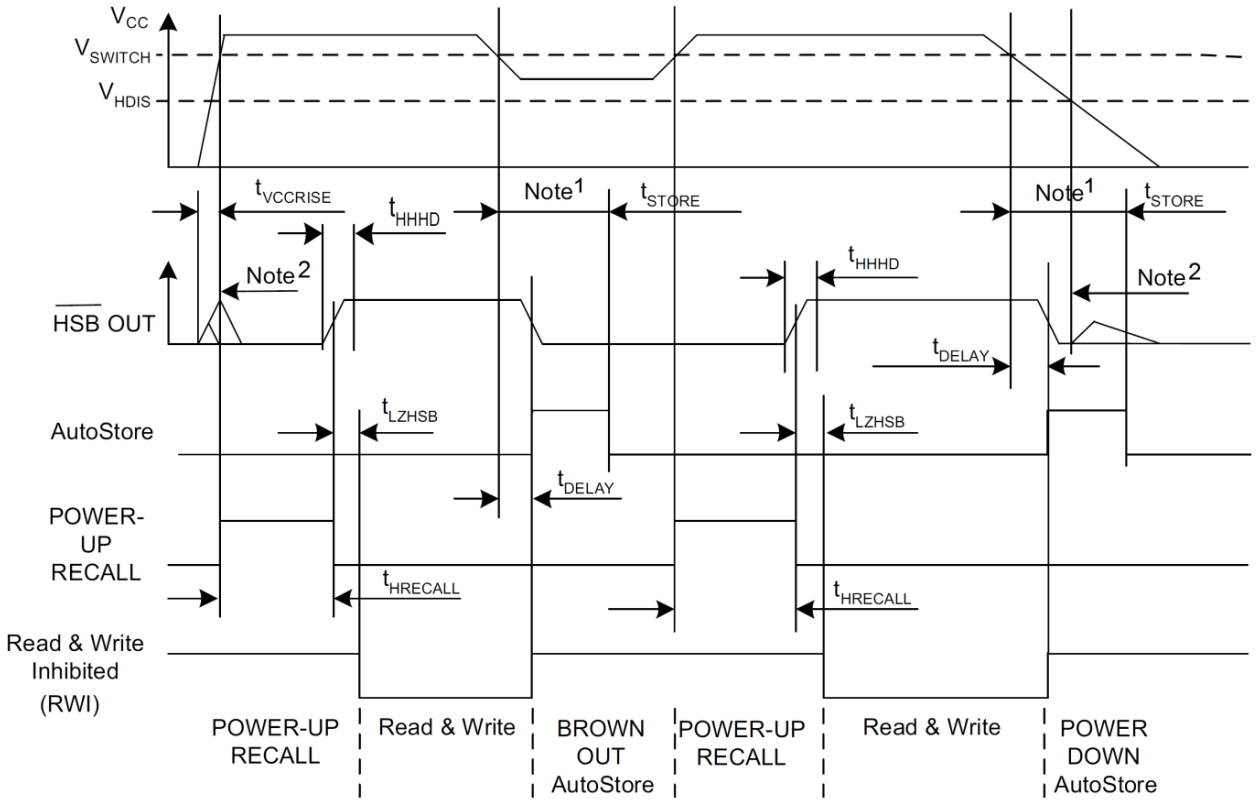
When V_{CC} crosses the V_{HDIS} threshold voltage, internal circuits turn on and an internal POR is initiated. During this period, the $\overline{HSB}$ output state is un-deterministic and it can be either HIGH or LOW and therefore, the voltage can either continue to rise with V_{CC} or fall to an output LOW level (V_{OL}). After V_{CC} crosses the V_{SWITCH} threshold, the $\overline{HSB}$ output is driven LOW. The $\overline{HSB}$ pin remains LOW until the power-up RECALL is completed. After the recall cycle is successful, the $\overline{HSB}$ pin is pulled HIGH (by the strong pull-up transistor Q1 for t_{HHHD} time and then the weak pull-up holds the Q2 pin HIGH thereafter). The nvSRAM can be accessed after t_{LZHSB} duration after the $\overline{HSB}$ pin transitions to HIGH.

Note During power-up, glitches on V_{CC} below V_{SWITCH} level can extend the $t_{HRECALL}$ duration. If glitches arrive consecutively during the power-up recall cycle, then the nvSRAM repeats RECALL operation and it extends the $t_{HRECALL}$ duration. Under an extreme brownout condition where multiple brownouts occur at very short intervals, the power-up recall duration may be extend up to twice the duration of normal recall time (2 x $t_{HRECALL}$) since the last stable power supply.

$\overline{HSB}$ Behavior at Power-down

During power-down, the $\overline{HSB}$ output is driven LOW as soon as V_{CC} crosses below V_{SWITCH} level and remains LOW until V_{CC} falls further below the V_{HDIS} level. Once V_{CC} falls below V_{HDIS} level, the $\overline{HSB}$ output driver gets disabled and the nvSRAM doesn't have any control on this pin and leaves $\overline{HSB}$ floating. If an external pull-up resistor is connected to the $\overline{HSB}$ pin, then it will keep the voltage at V_{CC} or V_{CCQ} (through which the $\overline{HSB}$ pin is pulled to) and continues to track this voltage. The $\overline{HSB}$ pin behavior during a power-up, power-down, and brownout condition is shown in Figure 2. The definition of each parameter shown in this figure is provided in Table 1.

Figure 2. $\overline{HSB}$ Behavior during AutoStore or Power-Up RECALL



Note
1. If no SRAM write cycle has been initiated after the nonvolatile STORE or software RECALL operation, then toggling the hardware STORE ($\overline{HSB}$) LOW will not initiate the nonvolatile STORE in the memory cell.
2. During the power-up / power-down cycle, the $\overline{HSB}$ output glitches when an external pull-up resistor is connected to this pin.

Table 1. AutoStore or Power-up RECALL

Parameters	Description	Note
$t_{HRECALL}$	Power-Up RECALL duration	Parameter values are not specified in this table. Refer to the device datasheet for these parameter values.
t_{STORE}	STORE cycle duration	
t_{DELAY}	Time allowed to complete SRAM write cycle	
V_{SWITCH}	Low-voltage trigger level	
$t_{VCCRISE}$	V_{CC} rise time	
V_{HDIS}	$\overline{HSB}$ output disable voltage	
t_{LZHSB}	$\overline{HSB}$ to output active time	
t_{HHHD}	$\overline{HSB}$ HIGH active time	

Initiating a Hardware STORE

A hardware STORE is initiated by driving the $\overline{HSB}$ pin LOW. If the $\overline{HSB}$ is driven LOW while a SRAM write is still in progress, the hardware STORE is internally delayed by a period of t_{DELAY}. This ensures that the write operation is completed before the hardware STORE operation is initiated. The SRAM write cycle requested after the $\overline{HSB}$ goes LOW is inhibited until the $\overline{HSB}$ returns HIGH. Pulling the $\overline{HSB}$ pin LOW externally, irrespective of the Write Latch is set or not, inhibits all reads and writes in the nvSRAM until the $\overline{HSB}$ returns HIGH.

Figure 3 shows the hardware ($\overline{HSB}$) STORE behavior when Write Latch is set and Figure 4 shows the hardware ($\overline{HSB}$) STORE behavior when Write Latch is not set.

Initiating Hardware Store in Serial Parts

In the serial (SPI and I^2C) nvSRAM devices, write to the SRAM happens after the last data bit (D0 bit of the data byte) is received. Therefore, a hardware STORE operation, initiated through the $\overline{HSB}$ pin before the completion of the last byte write cycle, will discard the storing of the last byte written. The $\overline{HSB}$ STORE operation should be initiated only after a minimum of one clock cycle after the last data bit (D0) is received to guarantee that the last byte is successfully written in the nvSRAM.

Figure 3. Hardware STORE Cycle (Write Latch Set)

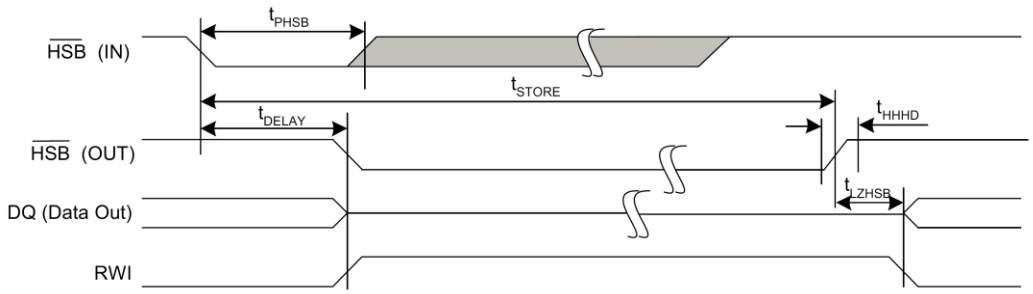
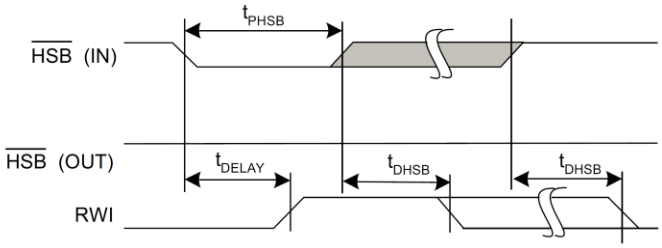


Figure 4. Hardware STORE Cycle (Write Latch Not Set)



Note: When the $\overline{HSB}$ output driver is disabled, the $\overline{HSB}$ pin is driven HIGH to the V_{CC} /V_{CCQ} by an internal weak pull-up resistor (~100 kΩ). All accesses to the SRAM are inhibited as long as $\overline{HSB}$ (Input) is driven LOW externally.

Table 2. Hardware STORE Cycle

Parameters	Description	Note
t_{DHSB}	$\overline{HSB}$ to output active time when Write Latch is not set	Parameter values are not specified in this table. Please refer the device datasheet for these parameter values.
t_{PHSB}	Hardware STORE pulse width	

Summary

This application note explains the $\overline{HSB}$ pin internal architecture and its functionalities. The device behavior during different applications scenario is also discussed in details. Following this application note, you should be able to control the $\overline{HSB}$ pin functionally appropriately in your system.

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Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1830597	UNC	12/12/2007	New application note.
*A	3155331	ZSK	01/27/2011	Added description on t_{DELAY} and t_{HHHD} timing parameter. Modified Figure 1 to add more details on $\overline{\text{HSB}}$ pin internal architecture Added sections to describe $\overline{\text{HSB}}$ behavior during power-up and power-down. Added Figure 2 to showcase $\overline{\text{HSB}}$ behavior during power-up/down and brownout situations. Added Figure 3 and Figure 4 to demonstrate the hardware ($\overline{\text{HSB}}$) STORE behavior. Formatted according to the new Cypress Application Note spec.
*B	3160226	ZSK	02/02/2011	Corrected the wrong application note number that was mentioned in the header from “AN61546” to “AN43380”.
*C	3756101	ZSK	09/25/2012	Contents re-arranged and rephrased. No change in any figures, tables or technical details. Applied new application note format.
*D	4277877	ZSK	02/11/2014	Sunset Review. Removed obsolete application note AN6023 reference. Removed the description on connecting $\overline{\text{HSB}}$ pins of multiple nvSRAM devices together (ganging of the $\overline{\text{HSB}}$ pins). Removed notes Note 3 and Note 4 on t_{SS} which are not related to the $\overline{\text{HSB}}$ operation.

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