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Spec No: 001-42961

Spec Title: AN42961 - USING A USB SWITCH WITH WEST BRIDGE(R) ANTIOCH(TM)

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AN42961

Using a USB Switch with West Bridge® Antioch™

Author: Sonia Gandhi
Associated Project: No
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Software Version: None
Related Application Notes: AN1168

To get the latest version of this application note, or the associated project file, please visit http://www.cypress.com/go/AN42961.

The West Bridge® Antioch™ device is a USB and mass storage peripheral controller that is a perfect fit for handset applications. The baseband or applications processors in handset systems may need to use an integrated full-speed USB transceiver at times, and switch to the West Bridge Antioch device for high-speed USB operations. This requires the use of a USB switch. This application note discusses the implications of adding a USB switch with West Bridge Antioch and provides the PCB layout recommendations to avoid degradation of signal integrity.

Contents

Introduction

The West Bridge Antioch device (CYWB0124AB) is a peripheral controller supporting high-speed USB and mass storage access. This controller provides access from a processor interface and a high-speed USB (HS-USB) interface to the following peripherals:

- SD
- MMC/MMC+
- CE-ATA
- NAND

The West Bridge Antioch device supports interleaving accesses between the processor interface, the HS-USB, and the peripherals. Therefore, an external processor and an external USB host can transfer data to each other and to the mass storage peripherals simultaneously.

The West Bridge Antioch device is a perfect fit for handset applications. The baseband or applications processors in handset systems may need to use an integrated full-speed USB transceiver at times, and switch to the West Bridge Antioch device for high-speed USB operations. This requires a USB switch. This application note discusses the implications of adding a USB switch with West Bridge Antioch, and provides PCB layout recommendations to avoid degradation of signal integrity. For details on the USB switches used for internal system testing at Cypress, contact Cypress.

The recommendations in this application note must be followed with those in the application note "*High-speed USB PCB Layout Recommendations*" (AN1168).

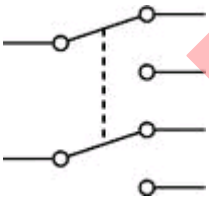
Architecture using USB Switch

Handset systems employ a USB switch to select between the full-speed USB transceiver of the baseband processor and the West Bridge Antioch high-speed USB controller.

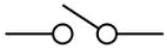
In such cases, the USB connector's D+ and D- are connected to the D+ and D- signals of the USB switch.

Two different types of switches are used in USB applications:

1) Double Pole Double Throw (DPDT) that use the following internal configuration:



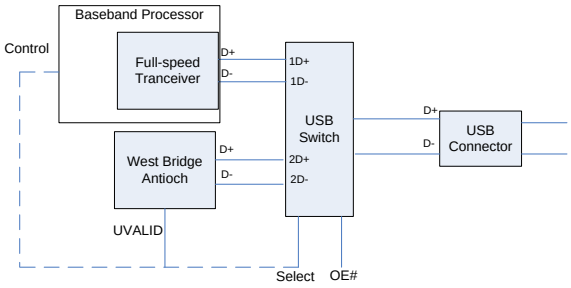
2) Single Pole Single Throw (SPST) that use the simpler configuration:



If the switch is a DPDT, one input source is connected to the D+ and D- lines of West Bridge Antioch, while the other input source is connected to the D+ and D- of the full-speed transceiver of the baseband processor. In general, Cypress recommends the SPST switch for the reasons demonstrated in this application note.

Figure 1 shows the DPDT switch architecture.

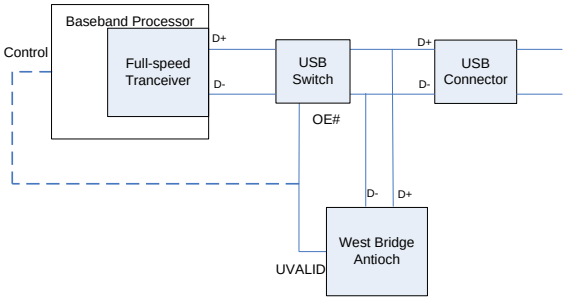
Figure 1. Architecture using a DPDT Switch



If the switch is SPST, the West Bridge Antioch device is connected at the output port of the switch and connected directly to the D+ and D- lines of the USB connector. The input port of the switch is connected to the transceiver of the baseband or applications processor. When the integrated transceiver is in use, the USB switch is enabled and West Bridge Antioch tristates its D+ and D- lines.

The SPST switch architecture is shown in Figure 2.

Figure 2. Architecture Using an SPST Switch



Signal Integrity Considerations

The high-speed USB D+ and D- signals operate at 480 Mbps. These signals need to be USB full-speed compatible and, as a result, also operate at 12 Mbps. These requirements and other electrical requirements of the USB specification call for cautious PCB layout practices. These requirements are enumerated in detail in the application note, "*High-speed USB PCB Layout Recommendations*" (AN1168), and some highlights are listed here.

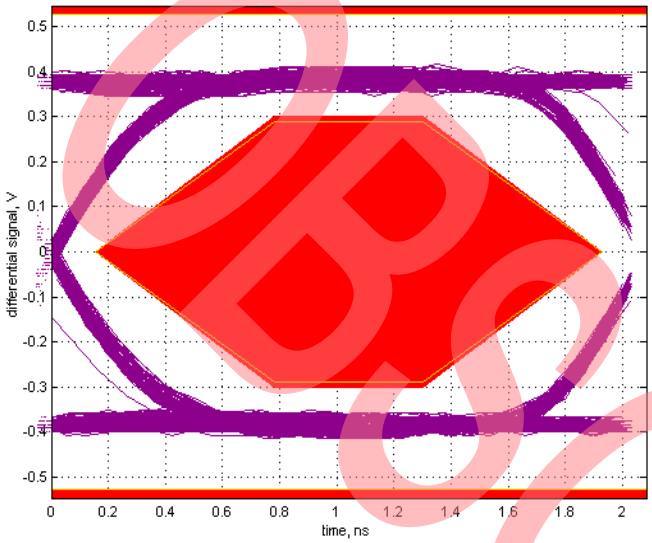
Controlled differential impedance of the D+ and D– traces is important in high-speed USB PCB design. The impedance of the D+ and D- traces affects signal eye pattern, end of packet (EOP) width, jitter, and crossover voltage measurements.

Introducing a USB switch on the D+ and D- traces may lead to impedance mismatch and can cause transmission line reflections. To avoid signal integrity failures, a USB switch must be placed as close as possible to the West Bridge Antioch device.

The West Bridge Antioch device by itself (without a USB switch on the D+ and D- traces), easily passes the signal integrity test under the USB specification requirement.

Figure 3 shows the eye diagram result of West Bridge Antioch by itself (without a USB switch on the D+ and D- traces). This is used as a benchmark in this application note, to judge the quality of the eye diagrams shown in the following sections.

Figure 3. Eye Diagram for Antioch without a USB Switch



Layout Examples and Resulting Eye Diagrams

As explained in the previous section, place the USB switch as close as possible to the West Bridge Antioch device to minimize signal reflections. The switch must be closer to the West Bridge Antioch device rather than the USB connector. The following three cases explain how signal integrity is affected by the distance of the USB switch from West Bridge Antioch.

Case 1

In this board layout example, the USB switch is placed closer to the USB connector rather than to the West Bridge Antioch device. Figure 4 shows the layout and Figure 5 shows the resulting eye diagram. In this case, the signal integrity test fails.

The board layout when using Fairchild's FSUSB20 DPDT switch is shown in Figure 4, with the following specifications:

- Distance from Antioch to switch = 1.7 inches
- Distance from USB switch to USB connector = 0.6 inches

Figure 4. Layout

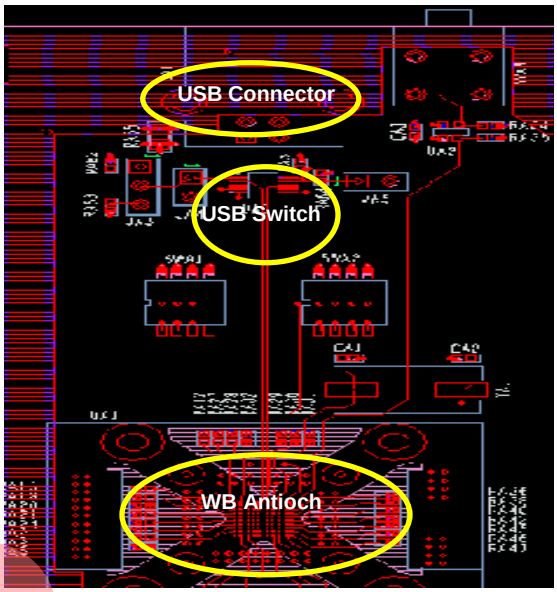
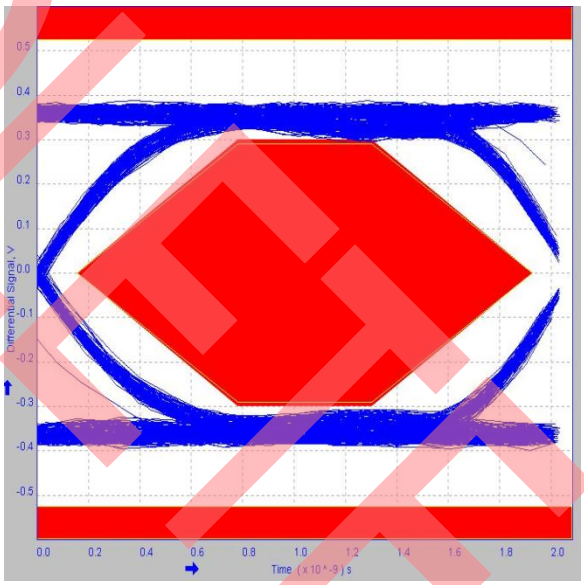


Figure 5. Eye Diagram Result for Layout in Figure 4



Case 2

In this board layout example, the USB switch is placed closer to the West Bridge Antioch device. Wherever you place the West Bridge Antioch device in a socket on the board, this socket itself poses certain layout restrictions. Figure 6 shows the layout and Figure 7 shows the resulting eye diagram. In this case, the signal integrity test passes marginally.

The board layout when using Fairchild's FSUSB30 DPDT switch is shown in Figure 6, with the following specifications:

- Distance from Antioch to switch = 0.4 inches
- Distance from USB switch to USB connector = 0.65 inches

Figure 6. Layout

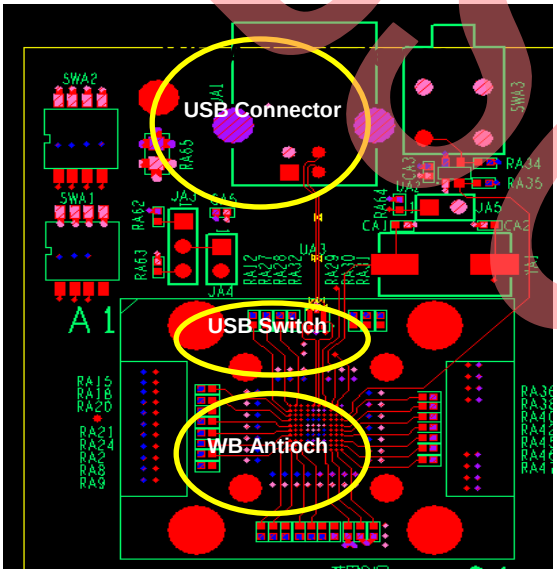
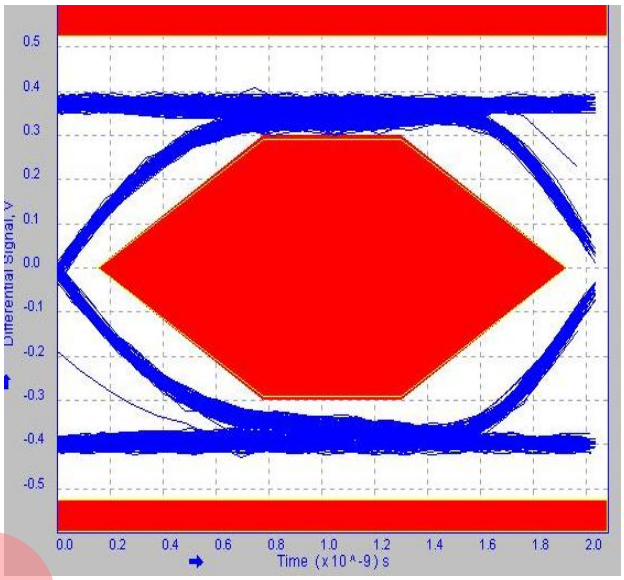


Figure 7. Eye Diagram Result for Layout in Figure 6



Case 3

In this layout example, the USB switch is placed as close as possible to the West Bridge Antioch device. Here, the Antioch is not in a socket, but directly on the board. This results in improved signal integrity as seen in Figure 9.

The board layout when using Fairchild's FSUSB40 DPDT switch is shown in Figure 8, with the following specifications:

- Distance from Antioch to switch = 0.17 inches
- Distance from USB switch to USB connector = 0.65 inches

Figure 8. Layout

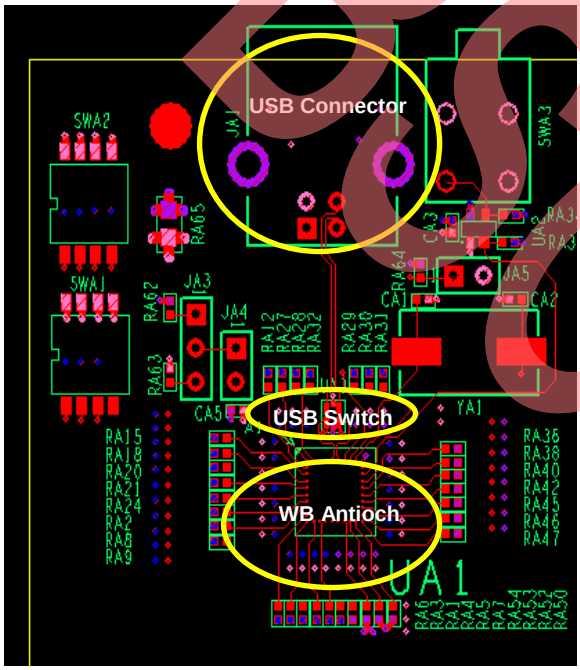
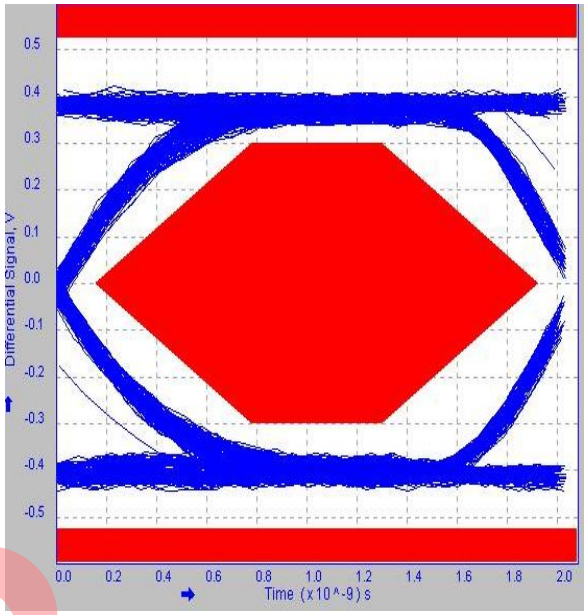


Figure 9. Eye Diagram Result for Layout in Figure 8



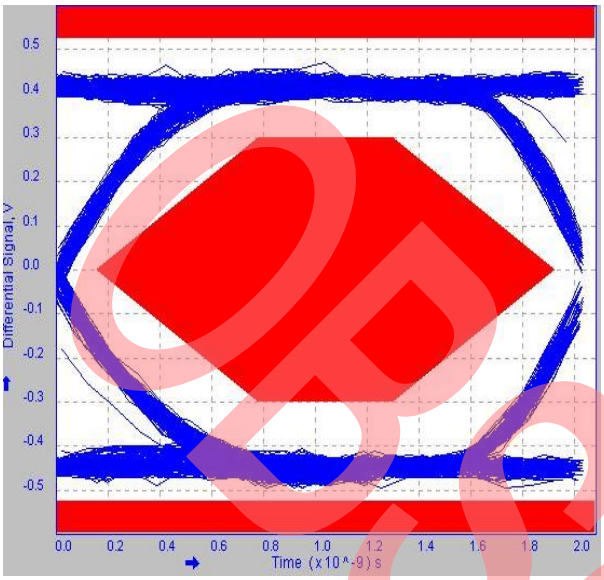
Signal Integrity Result with an SPST Switch

The results of the previous three cases are derived using a DPDT switch from Fairchild Semiconductor (FSUSB40/30).

Figure 10 shows the eye diagram when using a SPST switch from the same manufacturer (FSUSB31). Compared to the eye diagram in Figure 9, this has less jitter and provides more margin. Using this SPST switch provides the benefit of higher margin for the USB receiver sensitivity test. This provides greater flexibility in case other components such as chokes or filters need to be added on the D+ and D- lines.

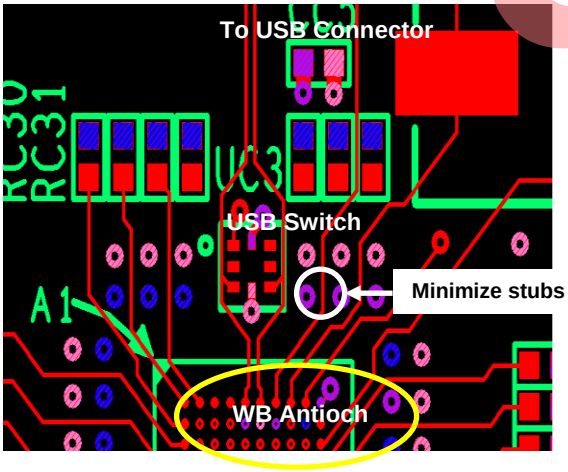
As a result, it is advisable to use a SPST switch with West Bridge Antioch.

Figure 10. Eye Diagram Result When Using an SPST Switch from Fairchild Semiconductor (FSUSB31)



When using a SPST switch, care must be taken to minimize stubs. Figure 11 shows an optimal layout to minimize stubs when laying out an SPST switch.

Figure 11. Optimal Layout to Minimize Stubs When Using an SPST Switch



All results mentioned in the previous sections are obtained by using switches from Fairchild Semiconductor. West Bridge Antioch has also been tested and found to pass the USB Signal Integrity test with switches from other manufacturers such as Pericom Semiconductor.

Figure 12 shows the eye diagram obtained when West Bridge Antioch is used with a DPDT switch from Pericom Semiconductor (PI3USB10LP-A).

Figure 12. Eye Diagram Result When Using a Switch from Pericom Semiconductor (PI3USB10LP-A)

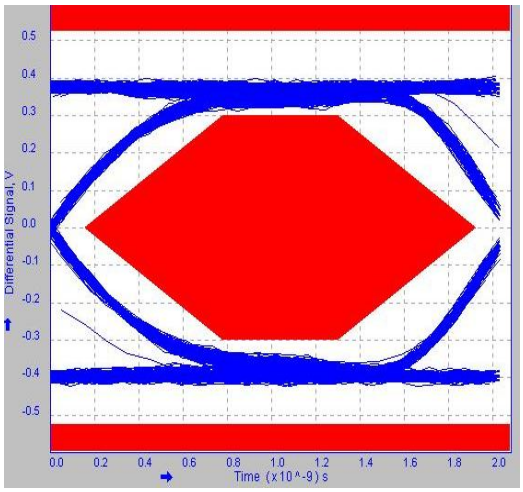


Table 1 shows a summary of the signal integrity and receiver sensitivity test results for different switches.

Table 1. Summary of Test Results

Manufacturer	Part Number	Type	Eye Diagram	Receiver Sensitivity Margin to 200 mV spec
Fairchild	FSUSB31	SPST	Pass	40 mV
Fairchild	FSUSB40	DPDT	Pass	30 mV
Pericom	PI3USB10LP-A	DPDT	Pass	35 mV

For more information on Fairchild Semiconductor's USB switch products, see: http://www.fairchildsemi.com/tree/signal-path-ics/switches/usb-switches/.

For more information on Pericom's switch products, see http://www.pericom.com/products/switch.

Additional Resources

- West Bridge® Antioch™ Advance Datasheet
- Fairchild Semiconductor FSUSB31 Product Folder
- Fairchild Semiconductor FSUSB40 Product Folder
- Pericom PI3USB10LP-A Data Sheet

Summary

West Bridge Antioch may be used successfully with a USB switch. Necessary precautions must be taken with respect to PCB design. The recommendations in this application note must be followed with other essential guidelines found in the application note *High-speed USB PCB Layout Recommendations*.

West Bridge Antioch has been tested at the system level with several USB switches. For further details, contact the applications team at Cypress or your local sales representative.

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**	1759065	ODC	11/19/2007	New application note.
*A	3103989	ODC	12/07/2010	Updated the following sections: Architecture using USB Switch and Signal Integrity Considerations. Updated links to associated application note and internal cross-references. Updated to new template.
*B	3171947	OSG	02/12/2011	Updated links to third-party products. Added “Additional Resources”.
*C	3469004	DBIR	12/19/2011	Updated to new template.
*D	4218523	DBIR	12/12/2013	Updated to new template. Completing Sunset Review.
*E	5588918	DBIR	01/24/2017	Obsolete document. Updated to new template. Completing Sunset Review.

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