THIS SPEC IS OBSOLETE

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Spec Title: Light Dimmer with CapSense® Brightness Control – AN42832

Sunset Owner: BVI

Replaced By: None

Light Dimmer With CapSense® Brightness Control

AN42832

Author: Petro Koblyuk
Associated Project: Yes
Associated Part Family: CY8C21x34, CY8C24x94
Software Version: PSoC® Designer™ 5.1
Associated Application Notes: AN2302, AN2394, AN13943

Abstract

To get lighting that is pleasant and comfortable to the eyes, you must be able to regulate the incandescent lamp brightness. This application note describes how the Light Dimmer helps you design an easy-to-use controller for incandescent lamp brightness. You can adjust the lamp brightness level by touching the CapSense® slider. The dimmer includes an LED bar graph to display the actual brightness as additional feature.

Introduction

Modern lighting controls have mechanisms that allow you to adjust the brightness to create comfortable and pleasant room lighting. Popular devices use a potentiometer with triac phase control technique for regulating lamp brightness. The proposed dimmer uses a touch sensitive control that enables you to control brightness easily and conveniently.

The design demonstrates how a PSoC® device is able to do more than offer CapSense as a design aid. A single chip is used for capacitance sensing, lamp power phase control, AC frequency calibration for worldwide use, and for multiplexed LED bargraph driving for night slight backlight.

Table 1 shows the technical specification of the Light Dimmer.

Table 1. Light Dimmer Specifications

Characteristic	Value
AC Supply	110 – 220 V, 47 – 63 Hz
Lamp Power	Depending on triac, 200 W for current design
CapSense Slider Overlay Thickness*	1 mm – 6 mm
Quantity of Brightness Levels	17

* Silicon glass, ABS, or plexiglass can be used for overlay. The slider segments dimensions must be adjusted according to the overlay thickness.

Power Phase Control

The light dimmer uses the principal of power phase control, which is easy to implement. The phase control operation principle lies in controlling triac turning on phase within AC supply period. Figure 1 shows the typical triac and lamp interconnection circuit. The delay variation between AC Zero Crossing signal and triac turning on time is used to control the amount of power provided to the lamp, as shown in Figure 2.

Figure 1. Typical Interconnection Circuit of Triac and Lamp

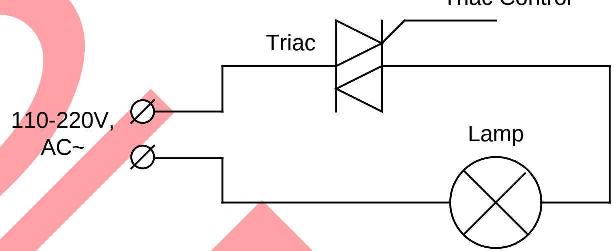
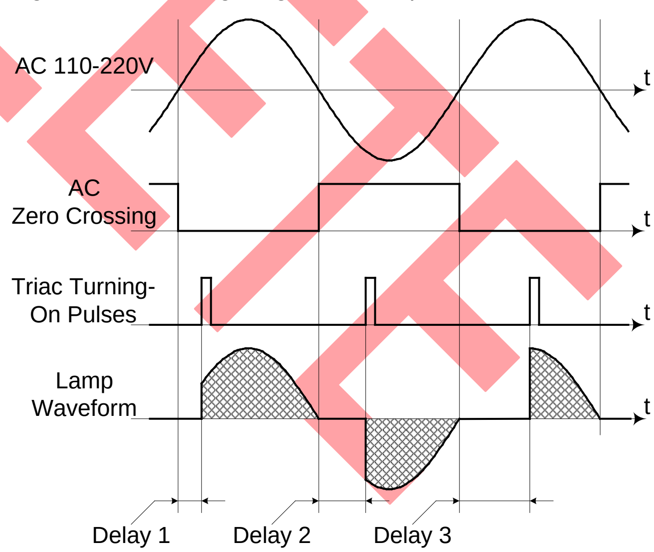


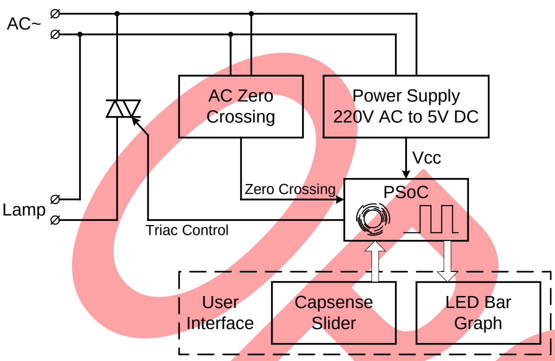
Figure 2. The Timing Diagram of Lamp Power Phase Control



Light Dimmer Block Diagram

The light dimmer consists of these blocks: AC zero crossing detector, PSoC's CPU core for general control, power supply, CapSense slider for load power control, and an LED bar graph, as shown in see Figure 3.

Figure 3. Light Dimmer Block Diagram



Dimmer Hardware

Figure 5 shows the light dimmer schematic. The $R_4 \ldots R_7$ resistors limit Q_2 base current, C_9 and $R_4 \ldots R_7$ form the LPF for zero-crossing detector false triggering prevention when noised AC signal is close to zero. The D_4 limits the reverse voltage applied to Q_2 base-emitter junction, R_{17} is zero-crossing detector pull-up. The zero cross detection operation is shown in Figure 4.

Figure 4. The Timing Diagram of "Zero Crossing" Signal

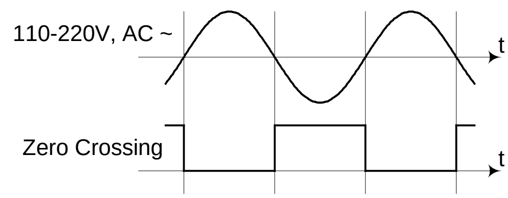
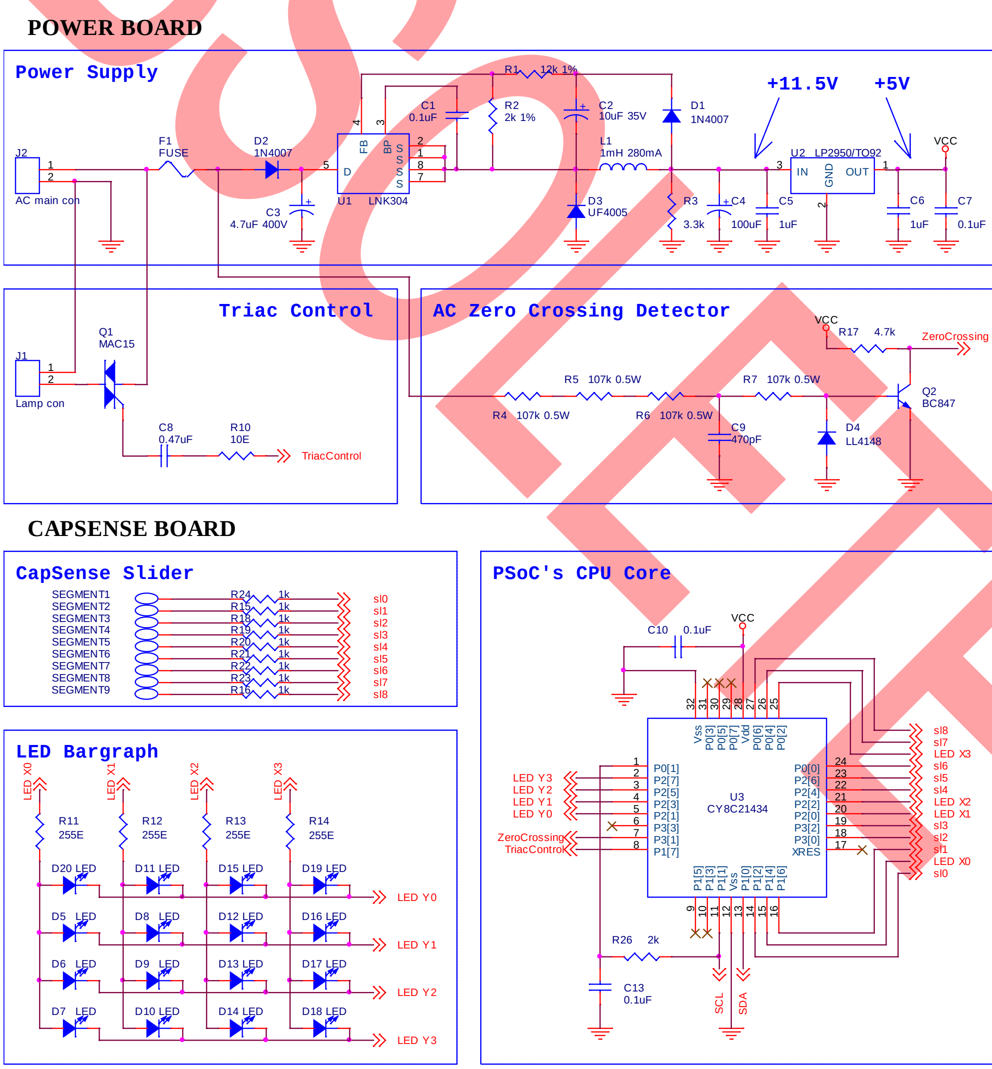


Figure 5. Light Dimmer Schematic



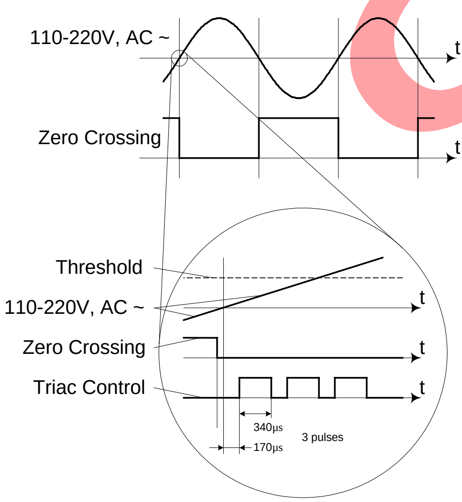
Power Supply

The dimmer power supply is implemented using the transformer-free switching DC-DC regulator, type LNK304 from Power Integrations [1]. The F_1 self recovered fuse serves two functions, it protects from possible over currents, and its resistance (about 8 Ohms) limits the C_3 inrush current at power on. The values of R_1-R_2 divider define the U_1 regulator output voltage, which is about 11.5 V. The U_1 output voltage varies with input voltage change and load current variations. CapSense use requires a stable PSoC power supply [2]. That is why the additional U_2 linear regulator is used to form the clear 5 V supply.

Triac Control

Triac is driven by short pulses to optimize power consumption. These pulses are generated by PSoC and are differentiated by C_8R_{10} network. Triac is turned on by series from three pulses, as shown in Figure 6. At full brightness triac turning on time is slightly delayed from the zero crossing event to guarantee reaching the minimum triac turning on voltage. This design provides stable operation if AC mains signal is noised.

Figure 6. The Timing Diagram of Triac Control



Note In Figure 6 the "Triac Control" signal is at minimal delay, that is, at the maximum brightness level.

Dimmer Firmware

Triac Control

The controllable delay between the zero crossing signal and triac turning on is used for lamp brightness control. The delay is generated by PWM8 user module for low-jitter operation. Both edges of the zero crossing signal are used for interrupt triggering. The interrupt handler that restarts the PWM with appropriate period value depends on the required delay. Initially PWM generates the first pulse with delay conditioned by the expected brightness level. Once the delay interval expires, the PWM registers are reloaded for generation series triac turning on pulses with 340 µs pulse duration and 170 µs interval between them. After three pulses the generation PWM disables itself and is reenabled by the following zero crossing interrupt.

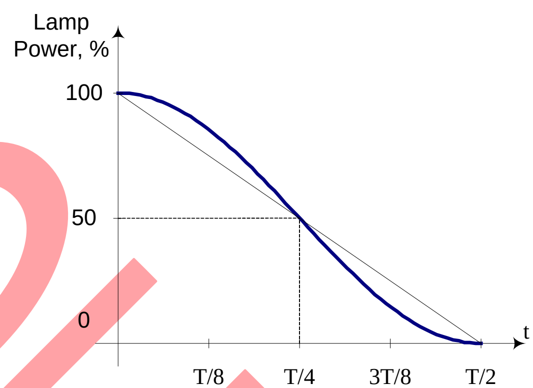
LED Bar Graph Control

The dimmer uses multiplexed LED control to drive 16 LED using only eight PSoC's pins. LEDs control occurs in four phases. In each phase only one appropriate LED row is turned on. The row switching time base is formed by CSD sensor scanning time, taking into account that scanning time is constant. The LED control state machine switches each row after each slider segment scanning for getting high refresh rate (about 250 Hz). This also prevents visible bar graph flickering. In each LED scanning cycle all LEDs are turned on for 3 µs using the software delay routine to provide low intensity night backlight for all LEDs.

Lamp Light Intensity Linear Control

The incandescent lamp power is not linearly proportional to the triac turning on delay (see Figure 7) due to sinusoidal AC mains current waveform nature.

Figure 7. Lamp Power Versus Triac Turning on Delay

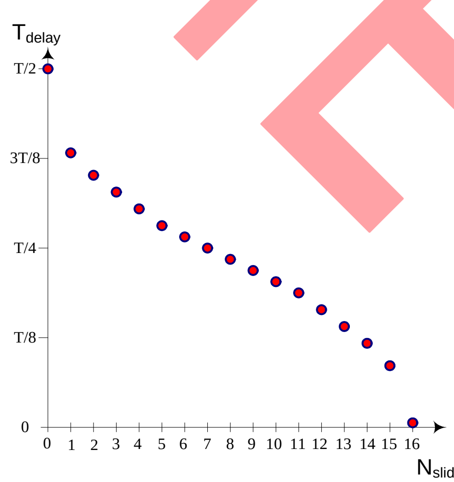


Note In Figure 7 the "T" is equal to AC mains period.

The human eye has logarithmic visible brightness vs. lamp brightness; also, the lamp visible brightness is a non-linear function of applied voltage RMS value via variation lamp resistance due to lamp coil temperature change.

To provide linear visual lamp brightness change, a non-linear lookup table (*baConst* array in C code) is used. This table has 17 entries and Figure 8 shows a lookup table graph. You can adapt this table to meet your needs.

Figure 8. Triac Turning on Delay Versus Slider Position



AC Mains Frequency Calibration

There are several frequency AC standards in the world, some countries use 50 Hz frequency, other 60 Hz. For the dimmer operation to work worldwide with no manual adjustments, an additional calibration procedure is implemented. This procedure measures the actual AC mains frequency and calculates the scale coefficient to transform the lookup table array for the actual triac turning on delay values. The calibration procedure is initiated once the dimmer powers up.

Calibration takes three stages. In the first stage the duration of AC half period is measured using a CSD UM counter block. The 32 measurements are taken, and the average value is calculated. For this, a CSD is manually reconfigured by re-routing counter enable signal from the comparator bus to zero-cross detector output.

In the second stage the scale coefficient is calculated in relation to the measured period (T_C) to the expected period (T_{C50}) for 50 Hz AC:

$$K = \frac{T_C}{T_{C50}} \qquad \text{Equation 1}$$

In the third stage the triac turning on delay table (*baConst*) is scaled by coefficient *K*.

Dimmer Mechanical Construction

The dimmer consists of two boards. All SMT components are placed on the first board. The first board has the LED array, the CapSense slider, and the reverse mount LEDs that are placed in the slider segments.

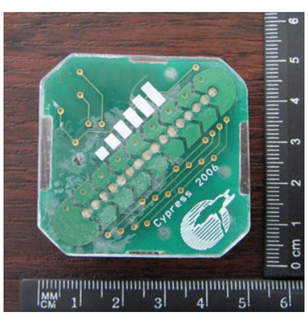
The power supply, zero crossing detector, triac and screw power and lamp connectors are placed on the second board. The all through hole components are located on this board as well.

The boards are connected using two connectors located on opposite sides of the board. The PCB Gerber files provided in the supporting archive, together with PSoC project, can be used for PCB routing reference.

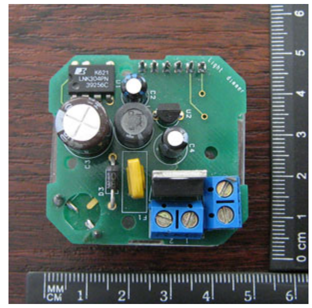
Figure 9 shows various views of the light dimmer.

Figure 9. Light Dimmer Photos

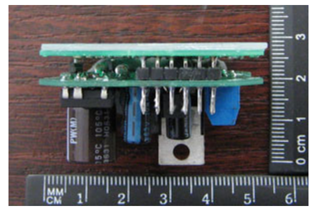
a) Front View



b) Back View



c) Side View



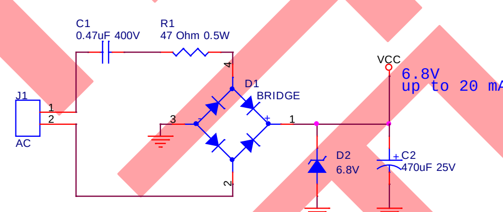
Safety Warnings

The light dimmer does not have galvanic isolation from the AC mains line. Make certain that the plastic overlay is of 1 mm or more thickness to prevent electric shock. Never touch the PCB or dimmer components when supply voltage is applied. Use the isolation transformer or galvanically isolated scope probes to debug and test the device.

Possible Modifications

You may want to optimize the dimmer price at the cost of sensitive applications. The most expensive part is the DC-DC converter switching. To reduce the BOM amount, redesign the power supply by using the simplest capacitive current source, see

Figure 10. Simplified Power Supply



In this case reduce the total current consumption to 25 mA by supplying smaller currents to the LED array and reduction the LED amount. Select the C_1 capacitor value according to AC voltage (110 or 220 V), the provided value was intended for 220 V supply.

Note To successfully pass the EMC tests an AC Mains filter may be required if the triac radiated noise is too large.

Alternative Dimmer Applications

Originally, the dimmer was designed for incandescent lamp control. With no modifications you can use the device to control universal motor speed in various applications, such as electric drills, pumps, air-conditioners, household appliances, etc. This is a good chance to replace the potentiometers by CapSense control.

Additional Resources

1. LNK304 datasheet
2. CSD UM datasheet

About the Author

Name:	Petro Koblyuk
Title:	Application engineer
Background:	Petro graduated from National University "Lviv Polytechnica" (Ukraine) in specialty 'computer systems' in 2001. Working in the Ukraine Solution Center since 2005.
Contact:	Petro.Koblyuk@cypressua.com

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1749763	XSG	12/10/2007	New application note
*A	3143991	ARVM	01/17/2011	Project update
*B	3185061	BVI	03/01/2011	Project update.
*C	3427167	BVI	11/01/2011	Obsolete spec

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone: 408-943-2600
Fax: 408-943-4730
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