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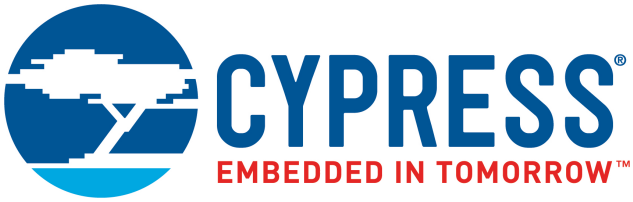

THIS SPEC IS OBSOLETE

Spec No: 001-42416

Spec Title: AN42416 - INTERFACING MOBL-USB(TM) TX2UL USB 2.0 ULPI PHY TO MARVELL MONAHANS LV APPLICATIONS PROCESSOR

Replaced by: None

AN42416

Interfacing MoBL-USB™ TX2UL USB 2.0 ULPI PHY to Marvell Monahans LV Applications Processor

Author: Dhanraj Rajput
Associated Project: No
Associated Part Family: CY7C68003
Software Version: None
Related Application Notes: AN42266

To get the latest version of this application note, or the associated project file, please visit http://www.cypress.com/go/AN42416.

There is an increasing demand in the mobile handset market for high speed USB (HSUSB) support. Mobile handset processors, including baseband and applications processors, have varying levels of HSUSB adoption. Some are unsupported, while others have integrated the serial interface engine (SIE). The Marvell Monahans LV processor (PXA31x) integrates the SIE and provides a ULPI (UTMI+ Low Pin Interface) port to interface with an external HSUSB ULPI transceiver. Cypress's MoBL-USB™ TX2UL is the ULPI transceiver of choice due to its optimized timing on the ULPI interface, tristate mode, and extremely tiny package size. AN42416 outlines all aspects of interfacing the MoBL-USB TX2UL to the Marvell Monahans LV applications processor.

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1 Introduction

Cypress's MoBL-USB TX2UL (CY7C68003) is a low power, high speed (HS) USB 2.0 ULPI transceiver. The TX2UL is specifically designed for mobile handset applications by offering tiny package options and ultra-low power consumption. TX2UL provides an industry standard ULPI USB interface that seamlessly interfaces to different baseband and applications processors in the market.

This application note discusses the following topics:

- TX2UL package options
- Hardware connections
- Power considerations
- Clocking considerations
- Oscillator and crystal configuration
- Operation modes

- GPIO sharing with tristate mode
- ULPI interface voltage, drive strength, and slew rate
- PCB layout recommendations

This application note is intended to be a supplement to the MoBL-USB TX2UL datasheet and all Marvell Monahans ecosystem documentation.

2 TX2UL Package Options

The Cypress MoBL-USB TX2UL device is available in two different package options: 24-pin QFN and 20-ball CSP. The 24-pin QFN package is 4 mm × 4 mm × 0.55 mm in size. The 20-ball CSP package is 2.2 mm × 1.8 mm × 0.55 mm, the smallest ULPI PHY in the market. The 20-ball CSP does not have the XO, VIO, VSSBATT, and NC pins, which are available only in the 24-pin QFN package. Consequently, the 20-ball CSP package does not support external crystals and the ULPI interface I/O voltage is limited to 1.8 V only.

3 Hardware Connections

The hardware connection between the Marvell Monahans LV applications processor and the Cypress MoBL-USB TX2UL is a simple, standard ULPI interface. While the Monahans has dedicated hardware pins for the ULPI control bus interface (STP/DIR/NXT), the designer selects which GPIOs on the Monahans functions as the rest of the ULPI control and data bus signals. There is a recommended user model in *Volume I: Monahans Processor Developers Manual: System and Timer Configuration Developers Manual*. See the Table 4-2 in this manual for a GPIO selection example. The sample schematics in Figure 1 show the hardware connections for the 24-pin QFN package; Figure 2 shows the 20-ball CSP with the Monahans LV applications processor.

Figure 1. Hardware Interface for Marvell Monahans LV and Cypress 24-Pin QFN TX2UL

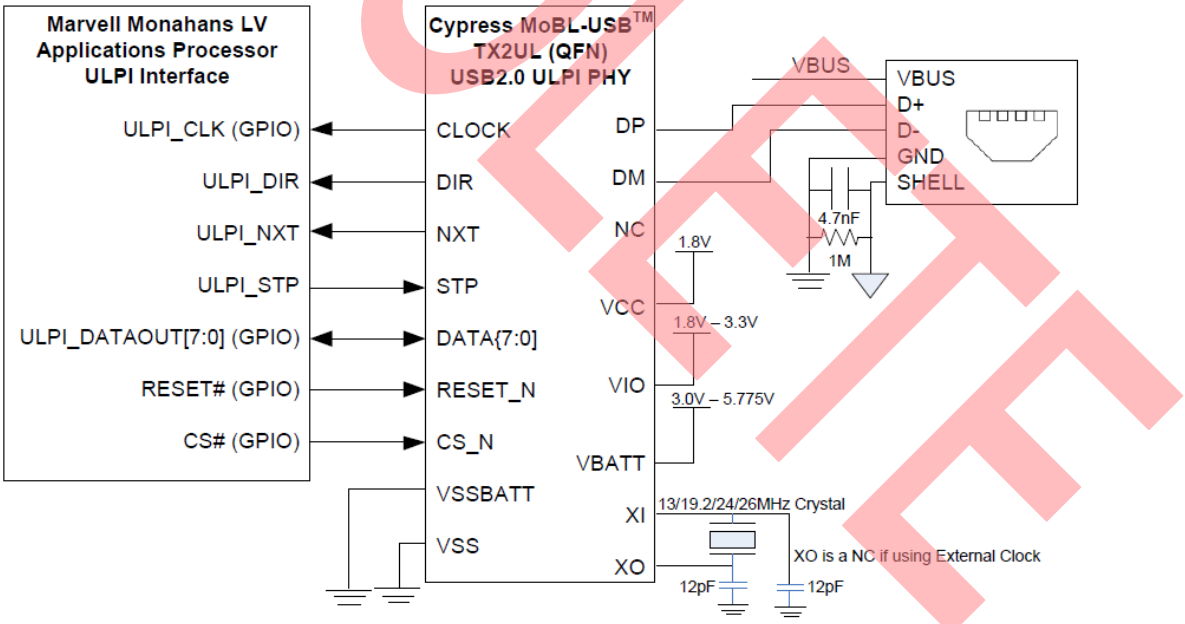
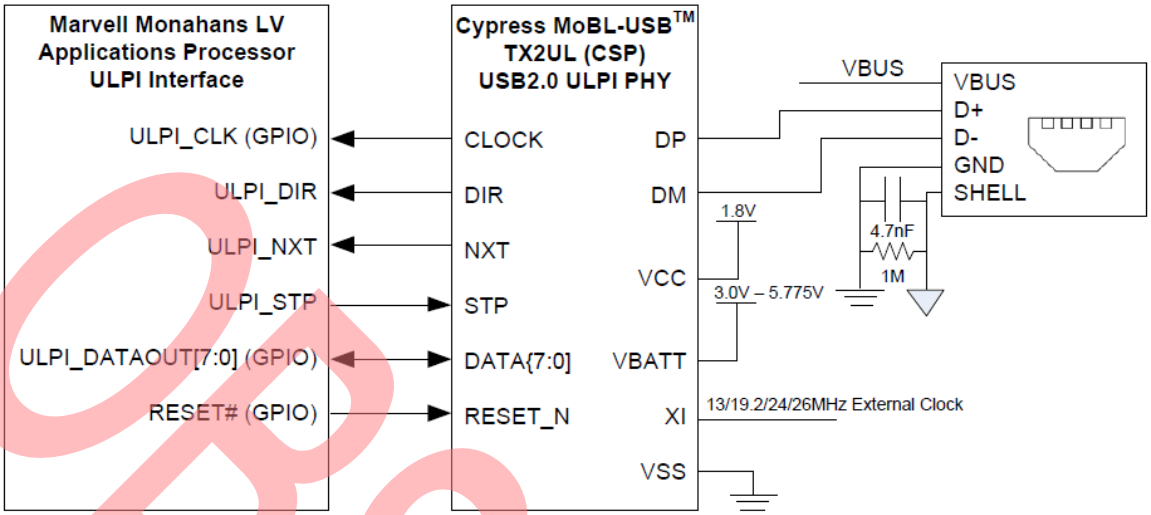


Figure 2. Hardware Interface for Marvell Monahans LV and Cypress 20-Pin CSP TX2UL



4 Power Considerations

The TX2UL in the 24-pin QFN package has three independent power domains—VCC, VIO, and VBATT. The TX2UL in the 20-ball CSP package has only two power domains, VCC and VBATT. VCC is the 1.8 V core power supply; VIO is the ULPI interface I/O voltage, which is flexible and is in the range 1.8 V to 3.3 V. The VBATT is the battery input supply that powers the 3.3 V regulator block and it ranges from 3.0 V to 5.775 V during actual operation. The internal 3.3 V voltage regulator block takes VBATT as an input and supplies it to the USBIO and XOSC blocks. If the supply voltage at VBATT is below 3.3 V, the regulator block switches the VBATT supply directly for the USBIO and XOSC blocks.

Note that all power supplies are independently sequenced without damaging the part. All supplies must be up and stable for the device to function properly (VCC, VIO, and BATT for the 24-pin QFN; VCC and VBATT for the 20-ball CSP). The analog block contains circuitry that senses the power supplies to determine when all supplies are valid. VCC and VIO both need to be on when VBATT is provided.

5 Clocking Considerations

Unlike the competition, TX2UL has the flexibility to accommodate an array of different clock input sources. TX2UL supports external crystals and clock inputs at the 13, 19.2, 24, and 26 MHz frequencies and the internal PLL applies the proper clock multiply option depending on the input frequency.

The TX2UL operates on one of two primary clock sources:

- LVCMOS square wave clock input driven on the XI pin.
  - XO pin must be left floating on the 24-pin QFN package.
  - This is the only clock input source on the 20-ball CSP package.
  - Clock signal amplitude is 1.8 V.
- Crystal generated sine wave clock on the XI/XO pins.
  - Only available in the 24-pin QFN package.

When using a clock input, make sure it meets the specifications provided in Table 1.

Table 1. External Clock Requirements

Parameter	Description	Specification		Unit
		Min	Max	
Vn	Supply voltage noise at frequencies < 50 MHz	–	20	mVp-p
PN_DC	Input phase Noise at DC	–	–75	dB
PN_1k	Input phase noise at 1 kHz Offset	–	–104	dB
PN_10k	Input phase noise at 10 kHz Offset	–	–120	dB
PN_100k	Input phase noise at 100 kHz Offset	–	–128	dB
PN_1M	Input phase noise at 1 MHz offset	–	–130	dB
	Duty cycle	30	70	%

When using a crystal input, make sure the crystal of choice meets the following specifications:

- Tolerance within (±) 100 ppm
- Parallel resonant
- Fundamental mode
- 750 mW drive level
- 12 pF (5% tolerance) load capacitors

The selection between input clock source and frequency on the XI pin is determined by the Chip Configuration register loaded through the RESET_N during Configuration mode. See the TX2UL datasheet for details.

6 Oscillator and Crystal Configuration

The TX2UL supports different frequencies of oscillators and crystals. To configure TX2UL with different clock source input, it must first be put into the Configuration mode. This mode is entered by pulling CS# to HIGH and RESET# to LOW for the duration of tSTATE. When TX2UL enters into the Configuration mode, the Marvell Monahans must generate pulses at the RESET# pin to configure TX2UL's clock source. The number of pulses determine what clock source is expected by TX2UL. When the configuration is completed, the CS# signal must be asserted LOW for tSTATE. Table 2 summarizes the configuration options. The TX2UL is defaulted to 26 MHz with single end clock input to XI.

Table 2. TX2UL Configuration Options

Number of Pulses at RESET# Pin During Configuration Mode	Configuration Description
0	26 MHz clock input on XI (default)
1	19.2 MHz clock input on XI
2	24 MHz clock input on XI
3	13 MHz clock input on XI
4	26 MHz crystal input on XI/XO
5	19.2 MHz crystal input on XI/XO
6	24 MHz crystal input on XI/XO
7	13 MHz crystal input on XI/XO

Figure 3. 24-Pin QFN Package Configuration Mode Entry Timing Diagram

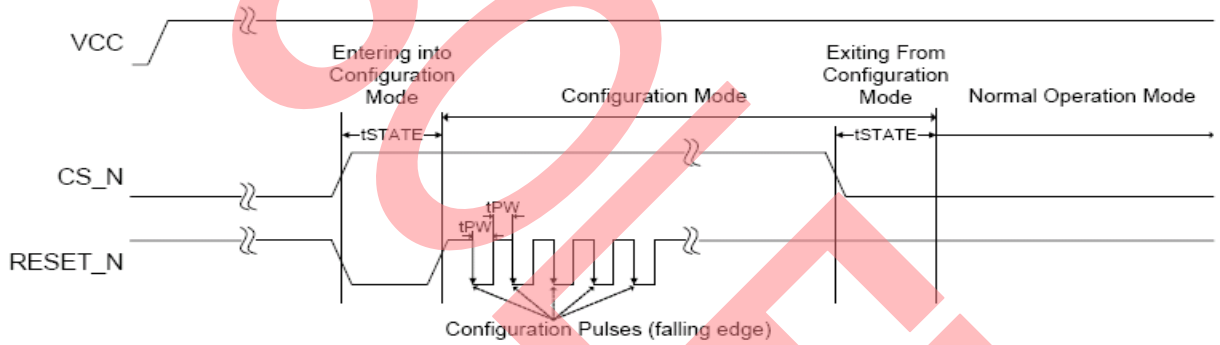
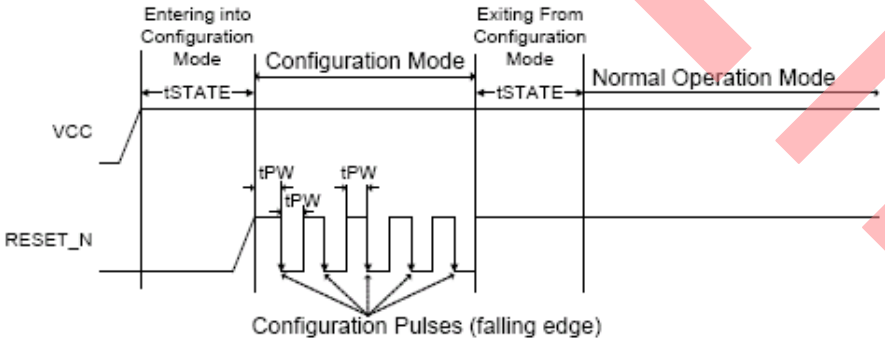


Figure 4. 20-Pin CSP Package Configuration Mode Entry Timing Diagram



7 Operation Modes

TX2UL has different operation modes, as listed in Table 3 and Table 4:

Table 3. 24-Pin QFN Package TX2UL Operation Modes

CS#	RESET#	Mode
0 (LOW)	0 (LOW)	Sleep mode
0 (LOW)	1 (HIGH)	Normal operation mode
0 (LOW)	1 (HIGH)	Enter into ULPI Low Power mode by setting SuspendM register bit (in function control register) to 0 during the normal operation mode
0 (LOW)	1 (HIGH)	Enter into Carkit UART pass through mode by setting Carkit mode register bit (in interface control register) to 1 during the normal operation mode
1 (HIGH)	0 (LOW)	Configuration mode
1 (HIGH)	1 (HIGH)	Tri-state ULPI interface output mode

Table 4. 20-Pin CSP Package TX2UL Operation Modes

RESET#	Mode
0 (LOW)	Sleep mode
1 (HIGH)	Normal operation mode
1 (HIGH)	Enter into ULPI low power mode by setting SuspendM register bit (in function control register) to 0 during the normal operation mode
1 (HIGH)	Enter into Carkit UART pass through mode by setting Carkit mode register bit (in interface control register) to 1 during the normal operation mode
0 (LOW) when Power On (VCC On)	Enter into configuration mode

For detailed descriptions, refer to the TX2UL datasheet. When changing the operation mode, it must first be changed to normal operation mode. For example, you cannot change from sleep mode directly to tristate ULPI interface output mode. First, you must transition from sleep mode to normal operation mode, then into tristate ULPI interface output mode.

8 GPIO Sharing with Tristate Mode

The need to support an increasing number of peripherals such as cameras, bluetooth, Wi-Fi, GPS modules, and memory expansion cards has increased the demands on a limited number of GPIOs. This is forcing mobile phone designers to share GPIOs between two functions that need not be used simultaneously. The problem here is to find a way to isolate one device from the data bus while the other is using it. Designers have resorted to the use tristate buffers, which add to the BOM cost and take up precious board real estate. These are two things that are unacceptable in mobile handset applications.

The MoBL-USB TX2UL in the 24-pin QFN package has a unique feature that allows ULPI IOs to be tristated when the device is put into the tristate ULPI interface output mode—one of the six modes supported by TX2UL. This feature effectively eliminates the need for costly buffers.

Figure 5 and Figure 6 show a simplified block diagram comparison of the solution with and without the tristate ULPI interface output mode.

The following must be taken into account when sharing GPIOs:

- If the device sharing GPIOs with the MoBL-USB TX2UL cannot tristate its I/Os, then buffer must still be used to isolate that device from the shared bus.
- No pins should be left floating when in tristate ULPI interface output mode, as it causes additional power consumption.

Figure 5. GPIO Sharing without Tristate ULPI Interface Output Mode

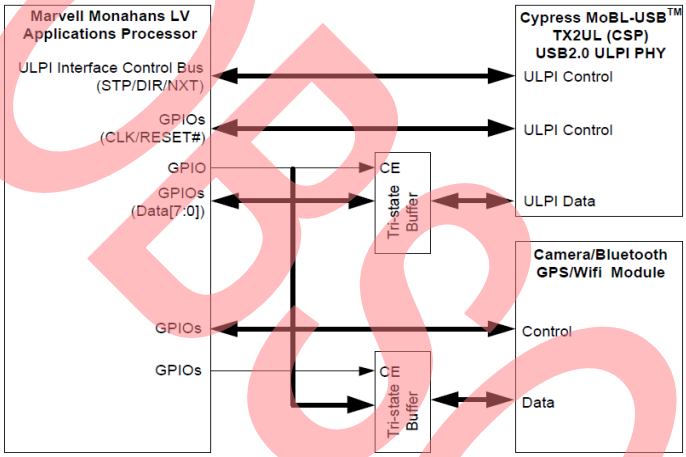
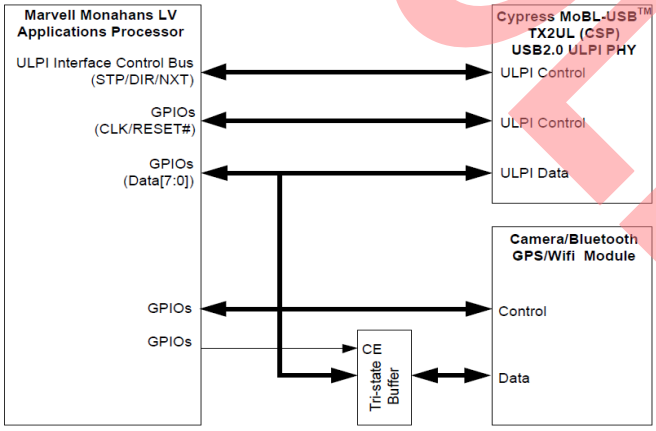


Figure 6. GPIO Sharing with Tristate ULPI Interface Output Mode



Note that the buffer in Figure 6 is only needed if the camera, bluetooth, GPS, or Wi-Fi module cannot tristate its data bus.

9 ULPI Interface Voltage Selection

The MoBL-USB TX2UL in the 24-pin QFN package has a flexible processor I/O interface, which supports 1.8 V to 3.3 V. The TX2UL in 20-ball CSP package supports the lowest I/O voltage of the range, 1.8 V. The Monahans LV applications processors specify a ULPI interface I/O voltage requirement of 1.8 V. Thus, both the QFN and CSP versions of TX2UL interface with the Monahans LV applications processor by using 1.8 V I/O voltages. Note that the RESET# and CS# signals are not a part of the standard ULPI signals. However, they must also be connected to the 1.8 V GPIO bank on the Monahans.

The I/O voltage of the TX2UL in the 24-pin QFN package depends on the voltage supplied to the VIO pin. The I/O voltage for a particular GPIO bank on the Monahans is selected via the associated VCCIO for that bank. Refer to the *Monahans Processor Electrical, Mechanical, and Thermal Specification (EMTS) Datasheet* for more information.

10 Drive Strength and Slew Rate

The GPIOs on the Monahans applications processor have selectable drive strength and slew rate. This feature optimizes the signal quality on the ULPI interface to avoid possible overshoots, depending on the trace impedance. The drive strength and slew rate are changed by setting bit [12:10] in the Multi Function Pin Register (MFPR) for each pin in the interface. Similarly, the drive strength and slew rate of the TX2UL device are selected by changing the Drive Strength and Slew Rate Configuration Register at x'31h.

11 PCB Layout Recommendations

There are two interfaces for which proper PCB layout is crucial:

- USB Interface
- ULPI Interface

There are many considerations when laying out the USB D+/D- interface to maintain signal integrity. Refer to the *High Speed USB PCB Layout Recommendations Application Note* for layout recommendations.

Due to the tight timing requirements on the ULPI interface, the layout of this interface is crucial to ensure that proper timing is met. The MoBL-USB TX2UL has ULPI interface timing that is designed to comply with the ULPI specification, which is optimized for interface to the Monahans applications processor. Table 5 summarizes the TX2UL timing parameters and compares them to the ULPI specification required by the Monahans.

For recommendations on the ULPI interface layout, refer to *Marvell Monahans Processor Design Guide*, which is available directly from Marvell.

Table 5. ULPI Interface Timing Parameters

Parameter	Description	MoBL-USB TX2UL		ULPI Specification 1.1		
		Min	Max	Min	Max	Unit
tCS	Setup time for control input	5.8	–	–	6.0	ns
tDS	Setup time for data input	5.8	–	–	6.0	ns
tCH	Hold time for control input	0	–	0	–	ns
tDH	Hold time for data input	0	–	0	–	ns
tCD	Output delay time for control output	7.6	9.0	–	9.0	ns
tDD	Output delay time for data output	7.6	9.0	–	9.0	ns

12 Summary

The MoBL-USB™ TX2UL is the ULPI transceiver of choice when interfacing to the Marvell Monahans LV applications processor. It has optimized timing on the ULPI interface allowing ease of layout. Its tristate mode provides the unique ability to share the bus with other devices, eliminating the need for costly external tristate buffers.

This application note, in conjunction with the TX2UL Usage Model application note, MoBL-USB TX2UL datasheet, and the Marvell Monahans ecosystems documentation, provides all of the information needed to ensure a smooth design cycle.

13 Referenced Documents

- Cypress: MoBL-USB™ TX2UL Datasheet.
- Cypress: Guide to a Successful EZ-USB® FX2LP™ Hardware Design.
- Marvell: PXA300 and PXA310 Processor: Vol. I: System and Timer Configuration Development Manual.
- Marvell: PXA300 and PXA310 Processor: Vol. IV: Developer Manual.
- Marvell: Marvell Monahans Processor Design Guide.

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**	2499466	DBIR	05/18/2008	New Spec.
*A	3132935	DBIR	01/18/2011	Marketing part updated from TX2LP18 to TX2UL throughout the document.
*B	3235331	DBIR	04/20/2011	No material changes. Added “About the Author” section.
*C	3610064	DBIR	05/07/2012	Updated to new template. Completing Sunset Review.
*D	4806021	DBIR	06/25/2015	Updated Hardware Connections: Updated hyperlink of “Volume I: Monahans Processor Developers Manual: System and Timer Configuration Developers Manual”. Updated Referenced Documents: Updated hyperlinks of all referenced documents. Updated to new template. Completing Sunset Review.
*E	5834756	RUPA	07/27/2017	Updated Cypress logo and Copyright information.
*F	6079597	HPPC	02/23/2018	Obsolete document

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