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Spec No: 001-42266

Spec Title: AN42266 - INITIALIZING TX2UL

Replaced by: None

Initializing TX2UL

Author: Ganesh Subramaniam
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Associated Part Family: CY7C68003
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With its low power consumption and small package options, the Cypress MoBL-USB™ TX2UL transceiver offers an ideal design for mobile applications. The TX2UL provides configuration and control registers that comply with the *UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1*. This application note describes how to configure these registers.

Introduction

TX2UL supports the immediate register set. It provides 11 control and configuration registers that allow the processor to access the ULPI bus with ULPI protocol. Table 1 shows the TX2UL register map.

Table 1. TX2UL Register Map

Field Name	Size (bits)	Address			
		Rd	Wr	Set	Clr
Vendor ID Low Register	8	00'h			
Vendor ID High Register	8	01'h			
Product ID Low Register	8	02'h			
Product ID High Register	8	03'h			
Function Control Register	8	04–06'h	04'h	05'h	06'h
Interface Control Register	8	07–09'h	07'h	08'h	09'h
Debug Register	8	15'h			
Scratch Register	8	16–18'h	16'h	17'h	18'h
Carkit Control Register	8	19–1B'h	19'h	1A'h	1B'h
Drive Strength and Slew Rate Configuration Register	8	31'h	31'h		
USB Interface Control Register	8	35'h	35'h		

Initializing Registers

During enumeration, three registers are initialized from their reset default value: Function Control Register (04–06'h), Interface Control Register (07–09'h), and USB Interface Control Register (53'h). Table 2, Table 3, and Table 4 show the description and reset default values of these three registers.

Table 2. Function Control Register (Address: 04h–06h [read], 04h [write], 05h [set], 06h [clear])

Bit	Field Name	Description	Access	Reset Value
1:0	XcvrSelect	Selects the required transceiver speed. 00'b: Enable HS transceiver. 01'b: Enable FS transceiver. 10'b: Not available. 11'b: Enable FS transceiver for LS packets.	rd/wr/s/c	01'b
2	TermSelect	Controls the internal 1.5 K pull-up resistor and 45 Ω HS terminations.	rd/wr/s/c	0'b
4:3	OpMode	Selects the required bit encoding style during transmit. 00'b: Normal operation. 01'b: Non-driving. 10'b: Disable bit stuff and NRZI encoding. 11'b: Do not automatically add SYNC and EOP when transmitting. It is used only for HS packets.	rd/wr/s/c	00'b
5	Reset	Active high transceiver reset. After the link sets this bit, TX2UL asserts DIR and resets the ULPI core. When the reset is complete, DIR is deasserted and automatically clears this bit. After deasserting DIR, TX2UL reasserts DIR and sends an RX CMD update to the link. The link waits for DIR to deassert before using the ULPI bus. It does not reset the ULPI interface or ULPI register set.	rd/wr/s/c	0'b
6	SuspendM	Active low; puts TX2UL into low power mode. TX2UL powers down all blocks except for the full-speed receiver and ULPI interface pins. TX2UL sets this bit to "1" when it exits low power mode. 0'b: Enter into low power mode. 1'b: Normal operation mode.	rd/wr/s/c	1'b
7	Reserved		rd	X

Table 3. Interface Control Register (Address: 07h - 09h [read], 07h [write], 08h [set], 09h [clear])

Bit	Field Name	Description	Access	Reset Value
1:0	Reserved		rd	xx'b
2	CarkitMode	Changes the ULPI interface to the carkit interface that supports UART pass through mode. This bit is cleared when it exits from carkit UART pass through mode. 0'b: Disable serial carkit mode. 1'b: Enable serial carkit mode.	rd/wr/s/c	0'b
6:3	Reserved		rd	xxxx'b
7	Interface Protect Disable	Controls the circuit built into TX2UL to protect the ULPI interface when the link tristates STP and DATA [7:0]. Any pull-ups or pull-downs employed by this feature are disabled. 0'b: Enable the Interface Protect Circuit. 1'b: Disable the Interface Protect Circuit.	rd/wr/s/c	0'b

Table 4. USB Interface Control Register (Address: 35h [read], 35h [write])

Bit	Field Name	Description	Access	Reset Value
1:0	Reserved		rd	00'b
2	UsbEnable	Controls the USB interface. 0'b: Disable the USB interface. 1'b: Enable the USB interface.	rd/wr	0'b
7:3	Reserved		rd	00000'b

After reset or power-on reset, use the ULPI RegWrite command to initialize the TX3 in full speed mode and enable the USB interface:

1. Write 45'h to the Function Control Register (04'h).
2. Write 00'h to Interface Control Register (07'h).
3. Write 04'h to USB Interface Control Register (35'h).

Figure 1, Figure 2, and Figure 3 show the ULPI protocol used to access these registers.

Figure 1. Write 45'h to Function Control Register

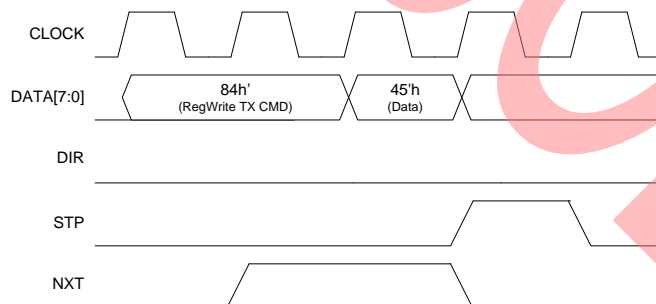


Figure 2. Write 00'h to Interface Control Register

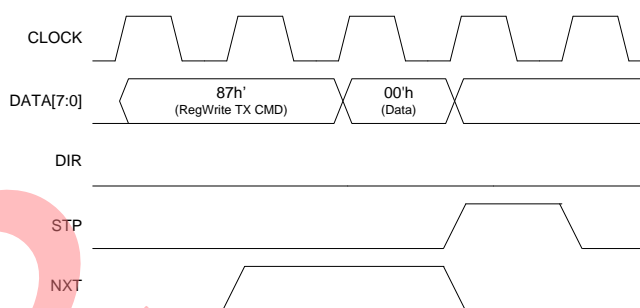
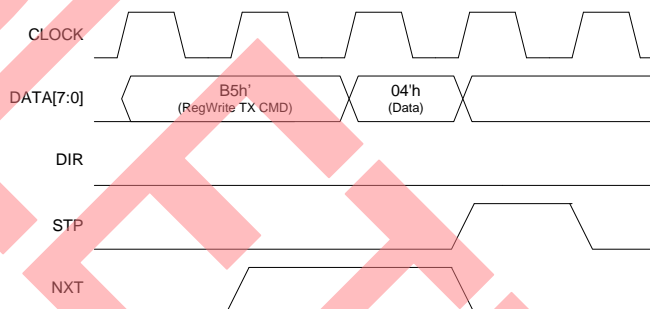


Figure 3. Write 04'h to USB Interface Control Register

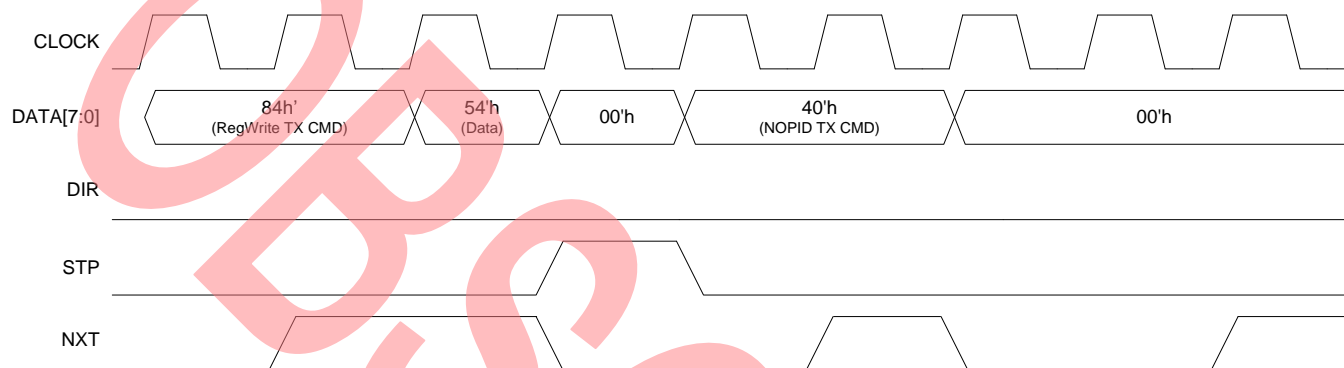


Enabling Chirp Signaling

When TX2UL connects to the host (for example, when a USB cable is plugged into the host hub), the host initiates a USB reset sequence. TX2UL sends the updated LineState in a Receive Command (RX CMD) byte to the processor. When the processor detects the USB reset (by RX CMD byte), TX2UL initiates chirp signaling.

To enable chirp signaling on TX2UL, the processor must write 54'h to the Function Control Register (04'h) and then initiate a NOPID transmit command with 00'h data as shown in Figure 4. For more information on this process, see *UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1*.

Figure 4. Processor Writes 54'h to TX2UL Function Control Register and NOPID Transmit Command



When the processor detects the host response with an alternating sequence of K's and J's, it sets the OpMode bits back to normal operation (clear bit[4:3]) in the Function Control Register. Then, the processor clears TermSelect (bit-3) in the Function Control Register as shown in Figure 5 and Figure 6.

Figure 5. Clear bit[4:3] of TX2UL Function Control Register

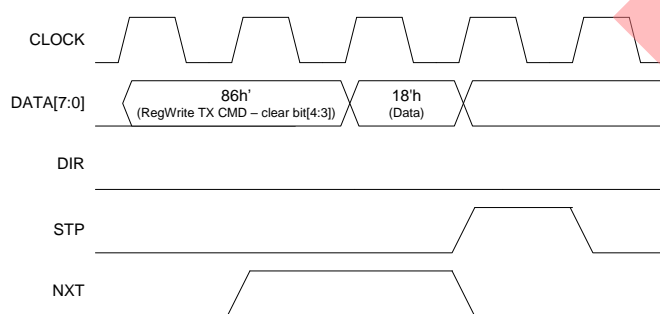
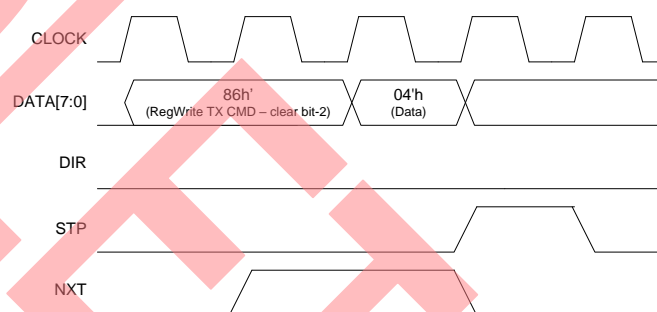


Figure 6. Clear bit-2 of TX2UL Function Control Register



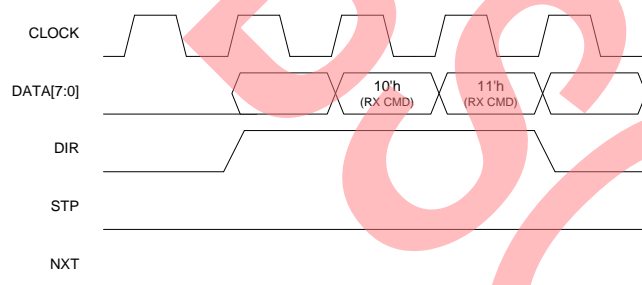
Enumeration

The process of enumeration occurs with the host reading the peripheral descriptors. For more information on this process, see *USB 2.0 Specification*. For more information on the data exchange between the device and host, see *EZ-USB® Technical Reference Manual*.

State transitions on the bus are communicated to the processor by receive commands (RX CMD) from the TX2UL. For more information on the Receive Command byte, see *UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1*.

Table 4 shows an example of an RX CMD from TX2UL. The first command (10'h) indicates RxActive, and the second command (11'h) indicates RxActive and LineState[0] going high.

Figure 7. TX2UL Sends RX CMD Bytes with 10'h and 11'h



Summary

After a reset or power-on reset, three registers provided by the TX2UL are initialized. After enumeration is complete, the processor starts to transfer traffic to the host through the TX2UL high speed USB transceiver.

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Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1678604	DBIR	11/01/2007	New Application Note
*A	3118366	DBIR	12/22/2010	Changed TX3LP to TX2UL. Updated to new template.
*B	3356905	DBIR	08/29/2011	No technical updates.
*C	4518342	DBIR	09/29/2014	Updated to new template. Completing Sunset Review.
*D	5877651	AESATMP9	09/08/2017	Updated logo and copyright.
*E	5956749	DBIR	11/03/2017	Making the AN obsolete

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