AN4065

QDR®-II, QDR-II+, DDR-II, and DDR-II+ Design Guide

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Associated Project: No
Related Application Notes: None

Cypress Quad Data Rate™ (QDR®)-II, QDR-II+, DDR-II, and DDR-II+ SRAMs address the high-bandwidth requirements for networking and data storage applications that provide up to 80 GBps data transfer rate. The purpose of this application note is to assist system designers in using the QDR-II, QDR-II+, DDR-II, and DDR-II+ SRAM devices. It includes guidelines on clocking and termination techniques for the QDR-II, QDR-II+, DDR-II, and DDR-II+ SRAM devices.

Contents

Introduction

QDR-II, QDR-II+, DDR-II, and DDR-II+ are designed to be the SRAMs of choice for networking applications with high data-rate requirements. DDR-II/DDR-II+ transfer data on both the rising and falling clock edges using a common data bus interface. QDR-II/QDR-II+ utilize two separate dedicated double data rate bus interfaces. Using the double data rate feature in both QDR-II/QDR-II+ and DDR-II/DDR-II+ SRAM devices results in higher bandwidth compared to other single data-rate SRAM devices, in which data transfers on single clock edge only. For further information on difference between QDRII/II+ and DDRII/II+, refer to the application note AN6017.

QDR-II and QDR-II+ Functionality

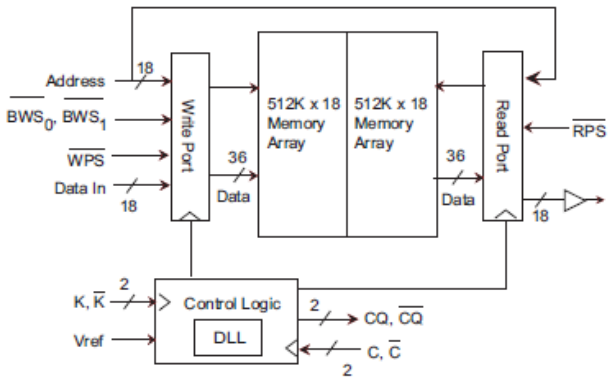
The QDR-II architecture consists of two separate ports (a READ port and a WRITE port) to access the memory array. Each port can be accessed through a common address bus and control inputs for each port. The QDR-II/QDR-II+ SRAMs use complementary input clocks (K and K#) to latch the address, control, and write data inputs.

Control signals include RPS# (Read Port Select), WPS# (Write Port Select), and BWSx# (Byte Write Select). RPS# is asserted to initiate a read operation. WPS# is asserted to initiate a write operation. BWSx# is used in conjunction with WPS# to perform byte write operations (only certain bytes are written). QDR-II/QDR-II+ SRAMs are offered in both burst of two and burst of four options. Burst of two implies two words of data are transferred per address, and burst of four implies four words of data are transferred per address. The address rate and write data placement differ between the two burst options.

For the burst of two option, the read address is provided on the rising edge of the K clock and the write address is provided on the rising edge of the K# clock. The write data is provided on the same clock edge as that of the write

address. For QDR-II, the read data is driven out after a 1.5-clock cycle latency, whereas for QDR-II+, the read data is driven out after 2.0 clock cycles or 2.5 clock cycles depending on the respective device option used. Figure 1 shows the block diagram for QDR-II burst of two.

Figure 1. QDR-II Burst of 2 Device (1 M x 18)



For the burst of four option, both the read and write address is provided on the rising edge of the K clock. The write data is provided with 1-clock cycle latency. For QDR-II, the read data is driven out after a 1.5-clock cycle latency, whereas for QDR-II+, the read data is driven out after 2.0 clock cycles or 2.5 clock cycles depending on the respective device option used.

QDR-II has a pair of optional input clocks (C and C#) that control the output data registers and determine when read data is clocked out of the device. These clocks are used in systems that have multiple SRAMs connected to a common controller. Figure 2 and Figure 3 show the block diagram for QDR-II burst of four and QDR-II+ burst of four respectively.

Figure 2. QDR-II Burst of Four Device (2 M x 18)

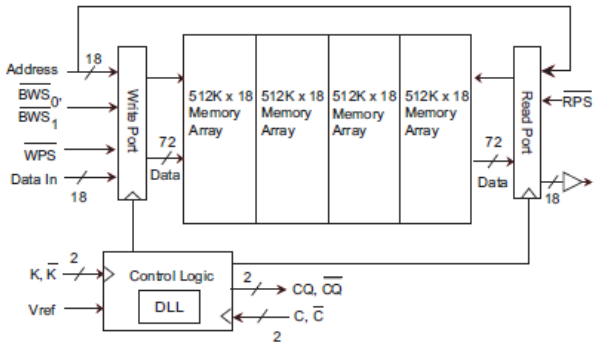
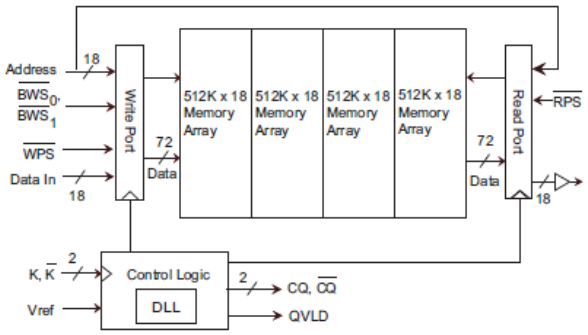


Figure 3. QDR-II+ Burst of Four Device (2 M x 18)



QDR-II+ devices are available in two flavors: one with read cycle latency of two cycles, and the other with read cycle latency of 2.5 clock cycles. QDR-II+ devices do not have the C/C# input clocks, but instead provide QVLD and ODT control signals. The QVLD (Valid Output Indicator) signal (which can be optionally used by the memory controller) is provided to simplify data capture on high-speed systems. QVLD is asserted one-half cycle before valid data arrives for each read data transfer. QDR-II+ devices are offered with or without an On-Die Termination (ODT) option. The ODT input provides range control (HIGH or LOW termination resistances) for devices that support this. For further information on ODT, refer to the application note AN42468.

Figure 4 and Figure 5 show example timing diagrams for QDR-II/II+ for bursts of two and four.

Figure 4. QDR-II/II+ Burst of Two Timing Showing Read Latency of Two

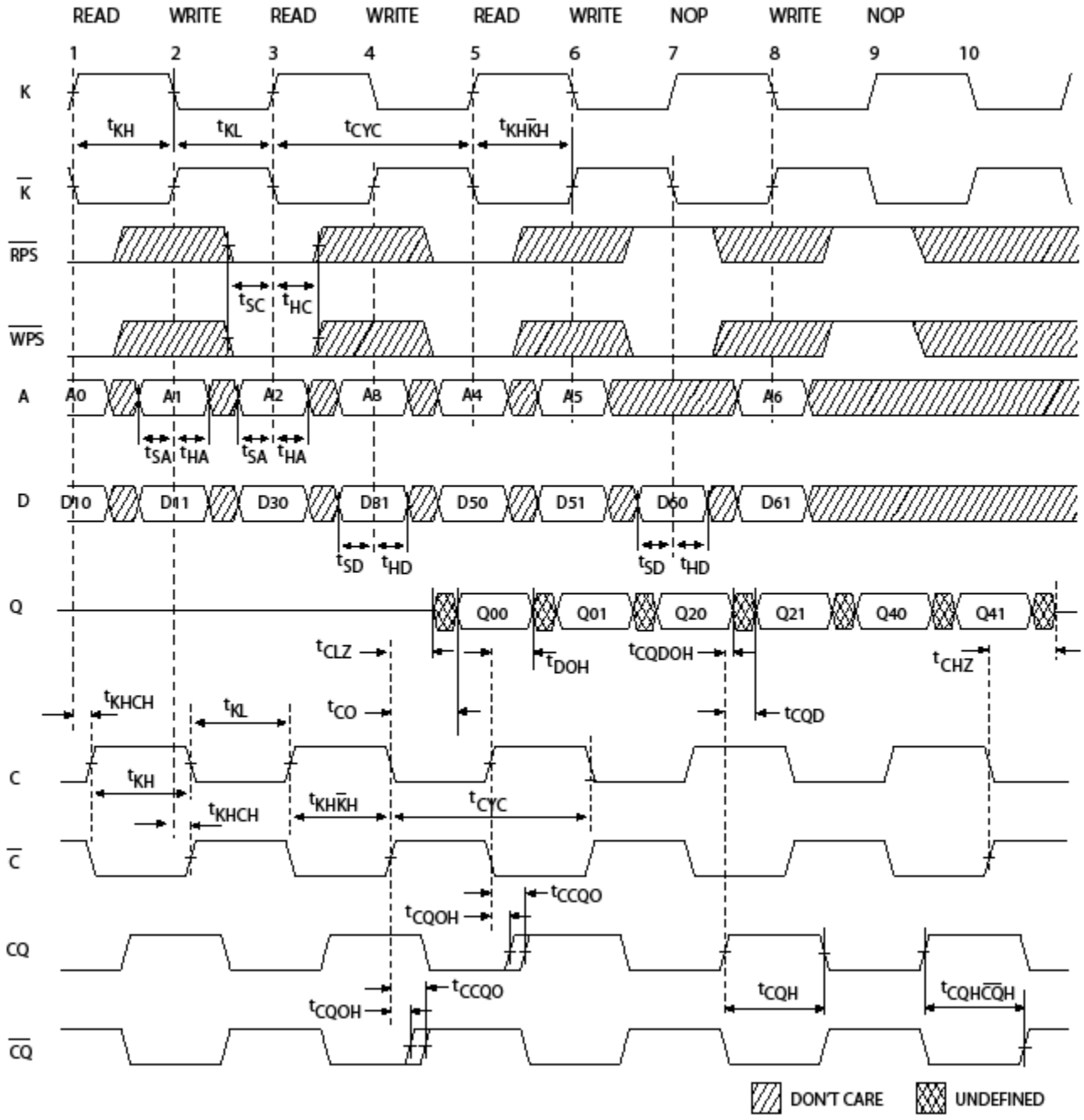
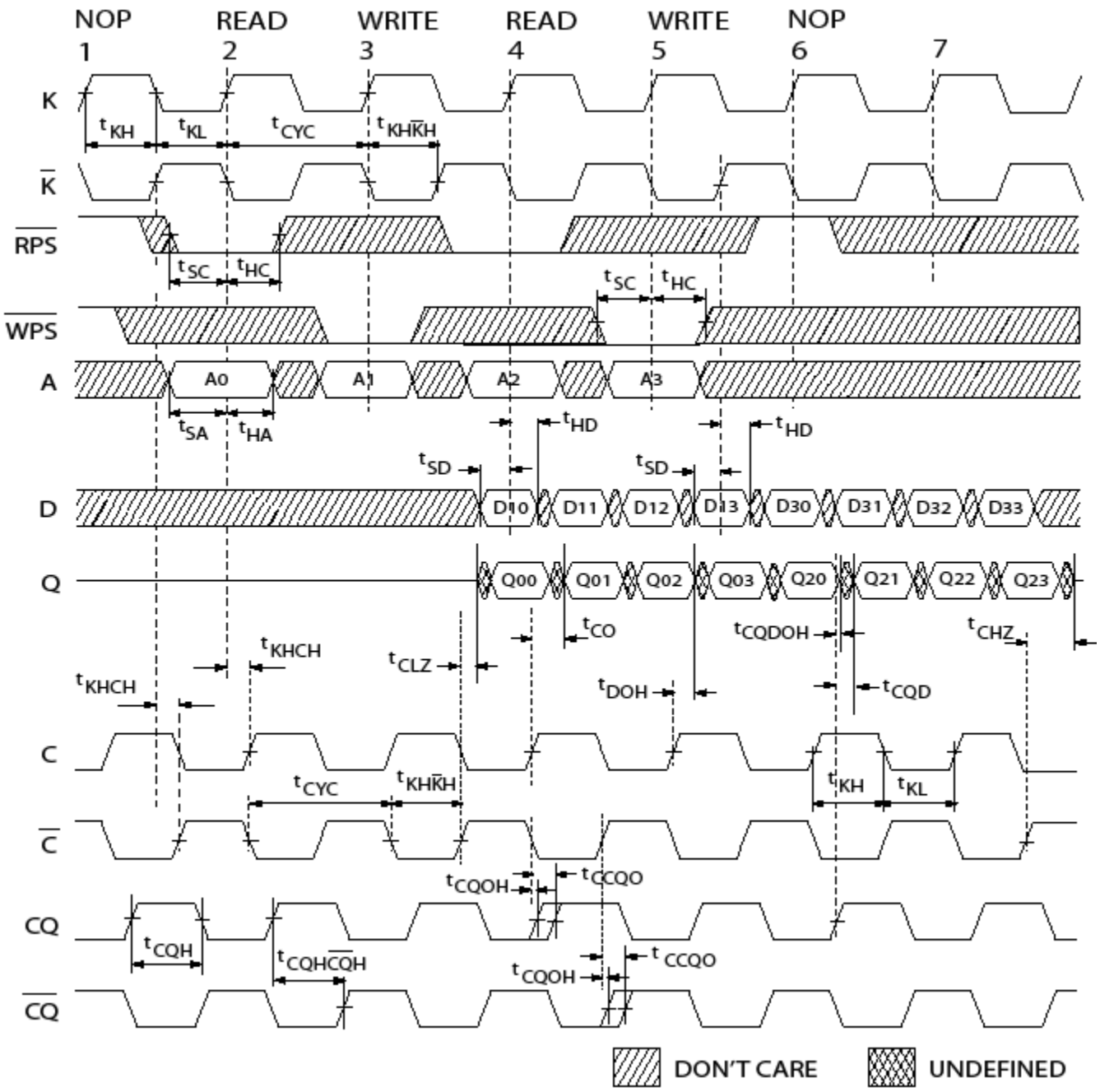


Figure 5. QDR-II/II+ Burst of Four Timing Showing Latency of Two



DDR-II and DDR-II+ Functionality

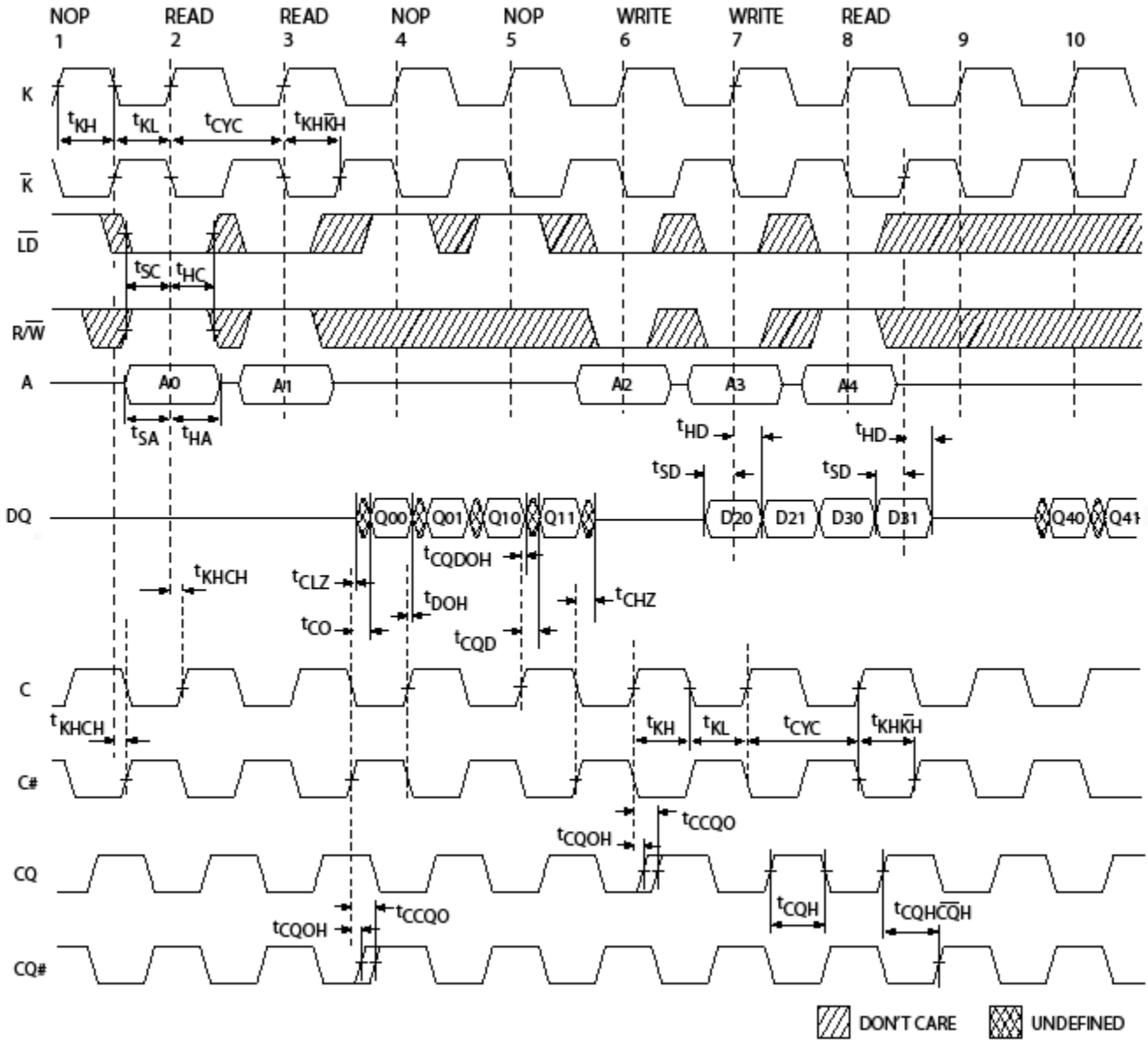
The DDR-II architecture is similar to that of QDR-II/QDR-II+ except that there is only one common data I/O port to access the memory array. Like QDR-II/QDR-II+, DDR-II/DDR-II+ SRAMs use complementary input clocks (K and K#) to latch the address, control, and write data inputs.

Control signals include R/W# (Read/Write Select), LD# (Load Select) and BWSx# (Byte Write Select). LD# is asserted to initiate a memory access. R/W# is asserted concurrently with LD# to indicate a read or write operation.

Also, BWSx# is used to perform byte select write operations. DDR-II/DDR-II+ SRAMs are offered in both burst of two and burst of four options. The address rate is different between the two burst options.

For the burst of two, the read address or the write address is provided on the rising edge of K clock. The write data is provided with 1-clock cycle latency. The DDR-II read data is driven out after a 1.5-clock cycle latency, whereas the DDR-II+ read data is driven out after 2.0 clock cycles or 2.5 clock cycles depending on the respective device option used. Figure 6 shows an example timing diagrams for DDR-II/II+ for bursts of two.

Figure 6. DDR II/II+ Burst of Two Timing Showing Latency of Two



For the burst of four option, the read or write address is provided on every other rising edge of the K clock. The write data is provided with a 1-clock cycle latency. DDR-II read data is driven out after a 1.5-clock cycle latency whereas DDR-II+ read data is driven out after 2.0 clock cycles or 2.5 clock cycles depending on the respective device option used.

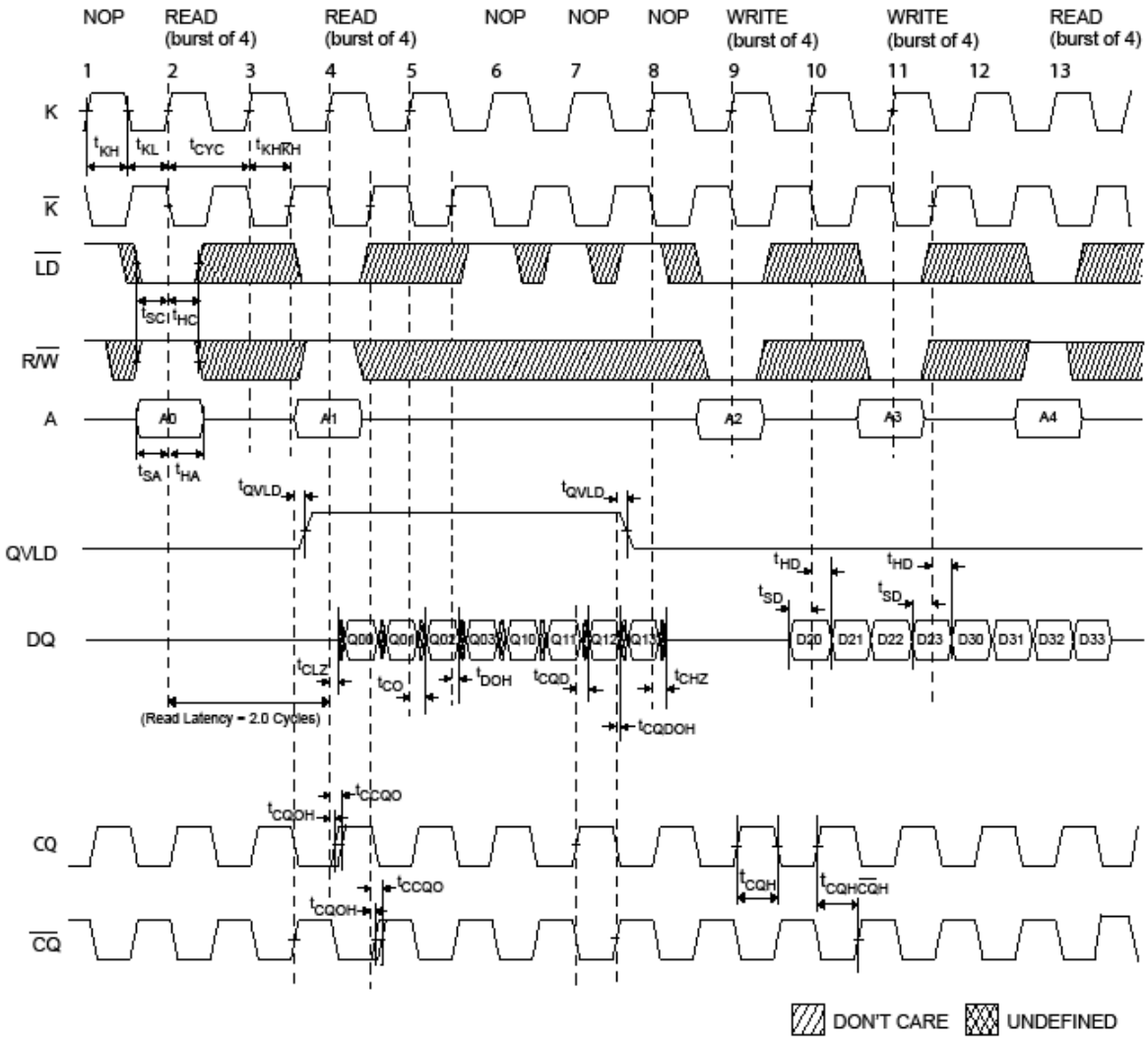
DDR-II has a pair of optional input clocks (C/C#) that control the output data registers and determine when read data is clocked out of the device. These clocks are used in systems that have multiple SRAMs connected to a common controller.

DDR-II+ devices are available in two flavors: one with read cycle latency of two cycles and the other with read cycle latency of 2.5 clock cycles. DDR-II+ devices do not have the C/C# input clocks, but instead provide QVLD and ODT control signals. The QVLD signal is used to simplify data capture on high-speed systems, which is asserted one-half cycle before valid data arrives for each read data transfer. DDR-II+ devices are offered with or without an on-die termination (ODT) option. The ODT input provides range control (HIGH or LOW termination resistances) for devices that support this.

For further information on ODT usage, refer to the Cypress Application Note AN42468. For further information on differences between QDR and DDR devices, refer to the Cypress Application Note AN6017.

Figure 7 shows an example timing diagrams for DDR-II/II+ for bursts of four.

Figure 7. DDR II/II+ Burst of Four Timing Showing Latency of Two



For detailed functional information with timing diagrams on QDR-II/II+ and DDR-II/II+, refer to the respective datasheets at www.cypress.com.

Feature Set Explanation – QDR-II, QDR-II+, DDR-II, and DDR-II+

Output Impedance Control

All QDR-II, QDR-II+, DDR-II, and DDR-II+ devices provide an option for users to control the drive strength of the output drivers. This is accomplished by using the ZQ pin. The output impedance of the QDR-II or QDR-II+ device can be varied between 35 Ω to 70 Ω. This allows you to match the driver impedance to that of the system boards. To use this method of impedance control, connect a resistor whose value is five times the required impedance at the ZQ pin. The ZQ circuit provides a pull-up and pull-down tolerance of ±15% (between 175 Ω and 350 Ω, with V_{DDQ} = 1.5 V). Alternately, this pin can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected. The output impedance is adjusted every 1024 or 2048 cycles (for QDR-II or QDR-II+ respectively) upon power-up to account for drifts in supply voltage and temperature.

Clocking Overview and Strategies

All QDR-II, QDR-II+, DDR-II, and DDR-II+ devices require an input clock pair, K and K#. Only the rising edges are used by the SRAM. The K# rising edge must ideally occur exactly one half clock cycle after the K rising edge. This balances the output data so that each data word has the same data valid time. If this is not the case, the output data valid window will not be symmetrical (Figure 8).

All QDR-II and DDR-II devices have an output data clock pair, C and C#. These clocks can be optionally used to control when the output data emerges from the device. This is very useful in systems in which multiple SRAMs are located at different physical distances from the bus master. All output data can be aligned using C and C# such that the whole result can be captured and easily synchronized at the bus master simultaneously. If not needed, C and C# must be strapped HIGH. If the C and C# clocks are used, the duty cycle factor shown in Figure 8 applies to these clocks as well.

All QDR-II, QDR-II+, DDR-II, and DDR-II+ devices have optional-use output echo clocks CQ and CQ#. These outputs are timed exactly like the output data Q signals and can be used as valid data indicators. The echo clocks are source-synchronous with the data and must be delayed to capture data at the receiver.

In summary, for QDR-II and DDR-II devices input signals at the SRAM are latched using the K and K# clocks.

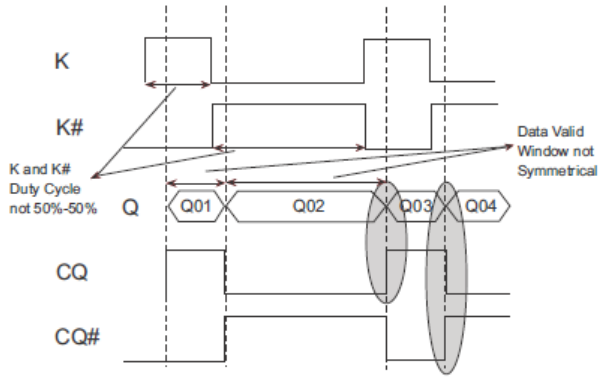
The output signals from the SRAM are latched at the receiving controller (ASIC/FPGA) by one of the following clocks:

- Using Input clocks K and K# for read data capture from SRAM (Not recommended for frequencies above 167 MHz)
- Using Input clocks K, K#, C, C# for read data capture from SRAM (Not recommended for frequencies above 200 MHz)
- Using CQ and CQ# for read data capture from SRAM and routed to the controller. (Recommended for all frequencies specified)

For QDR-II+ and DDR-II+ devices input signals at the SRAM are latched using the K and K# clocks. The output signals from the SRAM are latched at the receiving controller (ASIC/FPGA) by one of the following clocks:

- Using Input clocks K, K#, C, C# for read data capture from SRAM (Not recommended for frequencies above 200 MHz)
- Using CQ and CQ# provided by SRAM and routed to the controller

Figure 8. QDR-II and QDR-II+ K and K# Duty Cycle Effect (Single Clock Mode)



Refer to the Clocking Strategy 1: Using Input Clock K/K#, Clocking Strategy 2: Using Input Clocks K/K#, C/C#, and Clocking Strategy3: Using Echo Clocks CQ and CQ# sections to get more details on when and how to select the clock pair that can be used for latching data at the receiving controller (ASIC/FPGA).

Clock Startup

When initializing the system, two voltages are applied, V_{DD} (Core Supply) and V_{DDQ} (I/O Supply). Additionally, an external DOFF# enables and resets the PLL circuit internal to the SRAM. DOFF# should be tied HIGH if it is not used. The use of this signal is optional, however, it is highly recommended to follow the Power-up Sequence, which uses the DOFF# input control (Method 2 below).

This presents the following 2 startup methods:

Method 1: Power-up Sequence – with DOFF# always tied HIGH

1. Apply V_{DD} before V_{DDQ} or at the same time as V_{DDQ}.
2. Apply V_{DDQ} before V_{REF} or at the same time as V_{REF}
3. Wait for the input clock K/K# to stabilizes
4. Wait an additional 20 µs before starting memory operations

Method 2: Power-up Sequence – using the DOFF# control input

1. Start with DOFF# LOW.
2. Apply V_{DD} before V_{DDQ} or at the same time as V_{DDQ}.
3. Apply V_{DDQ} before V_{REF} or at the same time as V_{REF}
4. Drive DOFF# High only when the input clock K/K# has stabilized
5. Wait an additional 20 µs before starting memory operations

Clocking Strategy 1: Using Input Clock K/K#

In this strategy, K/K# are used as input clocks and read data capture clocks. The K/K# clock at the controller is used for latching the data driven out by the SRAM at the ASIC/FPGA. This method can only be used for frequencies up to 167 MHz.

For example, for QDR-II, Figure 9 shows the system diagram for the K/K# clock implementation. Moreover, for QDR-II, Figure 10 shows the resulting timing waveform for the K and K# clock usage assuming using a 133 MHz system clock. Figure 10 assumes two key parameters:

1. Internal Delay from controller clock generation to the output of the ASIC pins (ASIC buffer delay) is 2.0 ns.
2. Flight time from the ASIC to SRAM is 0.5 ns.

The t_{CO} for the SRAM is 0.50 ns (133 MHz) obtained from the datasheet. For the example to work, the ASIC must be able to capture input data with only 0.25 ns of input setup time. If this is not possible, gate delays can be added from the clock to the capture register to allow for more input setup time.

Figure 9. QDR-II With K and K# Clocks

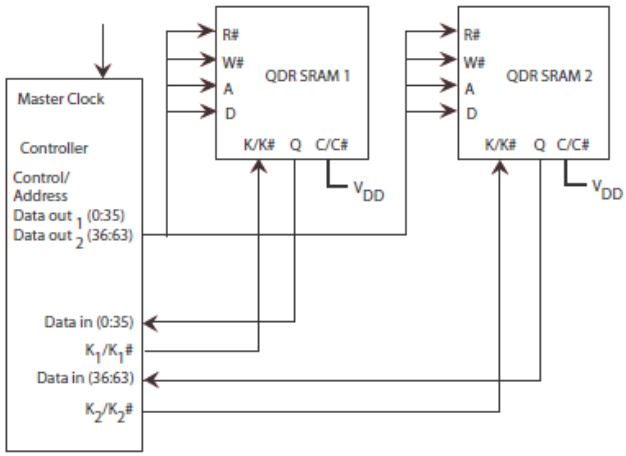
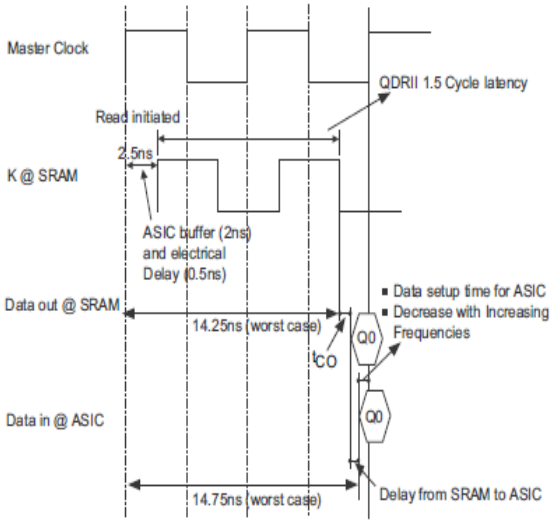


Figure 10. QDR-II Timing Waveform With K and K# Usage



Clocking Strategy 2: Using Input Clocks K/K#, C/C#

In this strategy, K/K# is used as input clocks and C/C# as read data capture clocks. The C/C# clock at the controller is used for latching the data driven out by the SRAM at the ASIC/FPGA. This method can only be used for frequencies up to 200 MHz.

C/C# clocks can be added to the circuit to make the output data from all SRAMs reach the ASIC at the same time. Figure 11 shows a system diagram for the C/C# clock implementation. As indicated in Figure 12, to ensure data arrives at the controller at the same time from both the SRAMs, the following conditions should be met:

1. Flight time of C/C# between SRAM1 and SRAM2 + Flight time of Q between SRAM1 and ASIC = Flight time of Q between SRAM2 and ASIC.
2. C/C# clocks are routed to the farthest SRAM first (SRAM2 in the example) and then connected to nearest SRAMs later.

The above two points ensures that all the data from both the SRAMs arrive at the ASIC at the same time. This is an example of a recommended implementation of the C/C# clock usage.

Figure 12 assumes three key parameters:

1. Internal delay from controller clock generation to the output of the ASIC pins (ASIC buffer delay) is 2.0 ns.
2. Flight time from the ASIC to SRAM1 is 0.5 ns.
3. Flight time from the SRAM1 to SRAM2 is 0.5 ns.

The t_{CO} for the SRAM is 0.50 ns (166 MHz) obtained from the data sheet. For the example to work, the ASIC must be able to capture input data with 1.25 ns of input setup time.

Figure 11. QDR-II Using C/C# Clocks

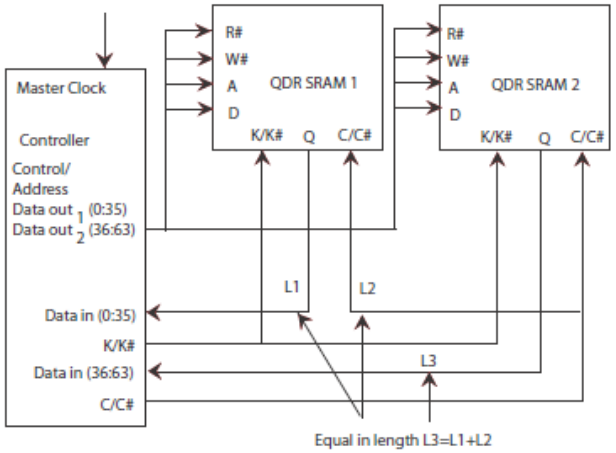
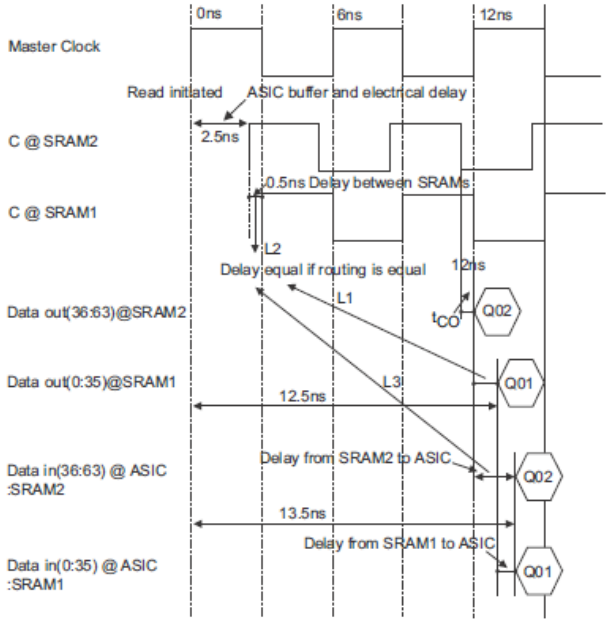


Figure 12. QDR-II Timing Waveform for C/C# Usage



Clocking Strategy 3: Using Echo Clocks CQ and CQ#

For QDR-II/II+, another scheme to capture high-frequency data employs K/K# and the echo clocks CQ/CQ#. The echo clocks are free-running clocks.

Using this method has one big advantage compared to other clocking methods used in the past. Any jitter introduced on the K clocks is not transferred to the CQ/CQ# edges because the echo clocks are regenerated within the SRAM using an internal SRAM PLL. The echo clocks are source-synchronous and edge-aligned at all times. Any jitter introduced by the internal SRAM PLL will affect both the echo clock and read data equally, and jitter effects are eliminated. In order for a System to work optimally, the trace lengths between the echo clocks (CQ/CQ#) need to be matched to the Data traces.

When the read data is sent from the SRAM, the echo clocks CQ/CQ# are edge-aligned with the data outputs. The receiving FPGA (or ASIC) will internally need to shift (delay) the echo clocks (CQ/CQ#) by 90 degrees in order to center-align the echo clocks with respect to the incoming read data.

For example, Figure 13 shows the system diagram for QDR-II+ implementation. The method for delaying echo clocks is to use the PLL within the FPGA or ASIC.

The same timing also applies to QDR-II as well.

Figure 13. QDR-II Using CQ/CQ# Clocks

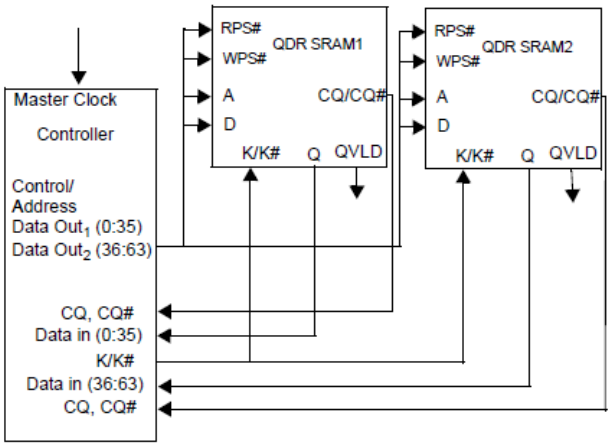
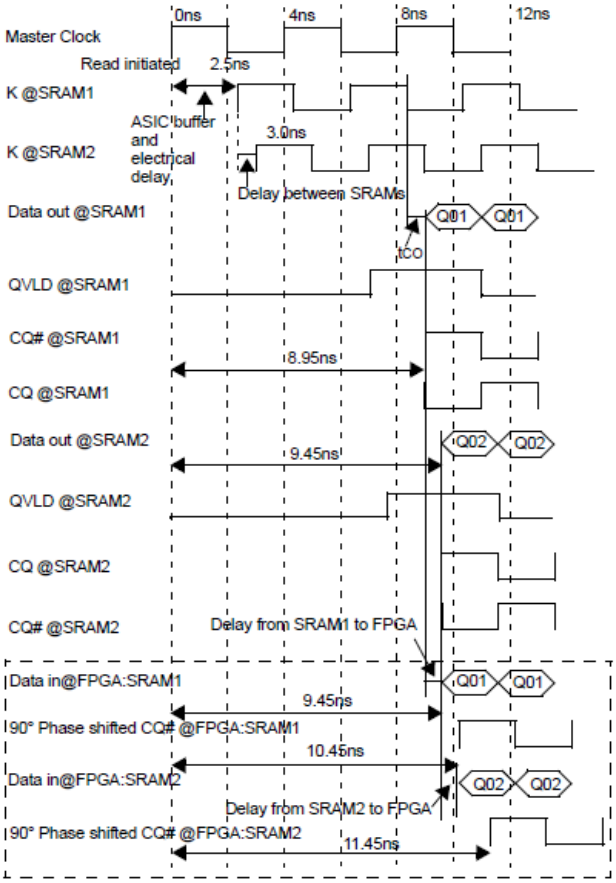


Figure 14 shows the timing using the echo (CQ/CQ#) clocks assuming a 250-MHz clock.

Figure 14. QDR-II+ Timing Information for CQ/CQ# Clocks



Summary of Clocking Strategies

Table 1. Clocking Strategies Summary

Clocking Strategies	Usage	Applicable SRAMs	Limitations	Frequency Range
Using K and K#	Data in/out	QDR-II, DDR II	Setup time for ASIC decreases at high frequencies	< 167 MHz
Using C and C#	Data out	QDR-II, DDR II	Flight path delay needs to be compensated	< 200 MHz
Using CQ and CQ#	Data out	QDR-II/II+.DDR-II/II+	None	All frequency ranges

From the above table, clocking strategies that use K/K# and C/C# for the read data path are limited in frequency of operation to 167 MHz and 200 MHz respectively. Clocking strategies that use CQ/CQ#, however, can run the entire frequency range specified in the QDR II/II+ and DDR II/II+ data sheets. For frequencies greater than 200 MHz, the echo clocks (CQ/CQ#) must be used for Read Data capture. Cypress recommends using the echo clocks strategy for all memory controller implementations across all QDR-II/II+ and DDR-II/II+ devices.

Signal Integrity and Layout Guidelines

For the most optimal performance of the QDR-II/II+ parts, follow these guidelines on a PC Board that uses these parts:

- All Data, Address and Clock lines must be matched closely within ±10 ps within each bus type and between buses. Alternatively, in terms of length, the matching translates to +/-60 mils using 160 ps per inch of trace length. Also Clock lines should be kept away from other signal and Clock lines to a minimum of 5x the trace width or larger if space allows.
- Cypress Packages are routed to obtain all traces to 50 Ω ± 10%. All traces must be routed to have 50-Ω impedance and should have no impedance discontinuities.
- All traces must be routed similarly as possible to have the same number of vias, traverse through the same layers, avoid bends, and other impedance mismatches.
- All traces must be simulated to ensure similar and low insertion loss. Consider putting more ground vias in the proximity of signal vias to reduce insertion losses.
- Consider using a series resistor to match total driver side impedance to 50 Ω.
- Ensure variation of V_{REF} is within ±2% by decoupling V_{REF} to V_{DDQ} and V_{SS}.
- Place termination resistors close to power sources.

Refer to the JEDEC document JESD 8-6, HSTL guidelines for noise margins to ensure that all noise simulations do not exceed noise margin, and to use the right values of decoupling capacitors to reduce the noise levels to a minimum.

Termination Schemes

Mismatched impedance causes signals to reflect back and forth along the transmission lines, which can cause ringing and jeopardize system reliability. The ringing reduces the dynamic range of the receiver (because of threshold shifts) and can cause false triggering. To eliminate reflections originating at the source, the impedance of the source (Z_S) must closely match the impedance of the trace (Z_O). To eliminate reflections originating at the load the impedance of the load (Z_L) must closely match the impedance of the trace (Z_O). This section discusses various signal termination schemes and provides input as to which one to use for unidirectional and bidirectional interfaces.

As indicated in the JEDEC Specifications (JESD 8-6), the following are the different termination schemes for HSTL QDR-II/II+, DDR-II/II+ SRAM devices:

1. Matching source impedance with transmission-line impedance – absorbs reflections at the source
2. Active Pull-up Termination to V_{TT} at the Load (HSTL Class-I) - absorbs reflections at the load
3. Series resistance on both ends of the transmission line (bidirectional I/Os only), e.g., DDR-II CIO device
4. Active Pull-up Termination (HSTL Class-II) to V_{TT} on both ends of transmission line (bidirectional I/Os only)

Each of the above termination schemes are discussed in detail. All of the following simulations are performed with QDR-II Driver buffer, V_{DDQ} = 1.5 V, a QDR-II receiver buffer and 2-inch trace length. All terminations are at $V_{DDQ}/2$. Simulations are provided to show differences between the termination schemes. The slew rate of the output swings shown for the different schemes depends upon load conditions and on the device and its revision used.

Matching Source Impedance to TX Line Impedance

QDR-I, QDR-II, QDR-II+, DDR-I, DDR-II, and DDR-II+ have an impedance-matching feature with which the impedance of the output driver can be set by tying a resistor value to ZQ (resistor value tied to ZQ is five times the value of the impedance desired). Figure 15 shows a termination scheme where the source impedance of the driver matches that of the transmission line impedance.

Figure 16 shows the Hyperlynx simulation results (using IBIS models) of the scheme shown in Figure 15. The output is measured at the receiver end. The trace length is 2 inch with a frequency of 250 MHz. The output does overshoot and undershoot close to -200 mV up to 1.68 V respectively. The simulations were done at the fast process corner. This scheme does not have any termination at the receiver end. Figure 17 shows the Eye diagram for this source impedance matched case. The bit rate is 0.5 Gbps and PRBS pattern was used to generate the Eye diagram. The eye height is 1.22 V and eye width is 1.962 ns.

Figure 15. Source Impedance Matching Scheme

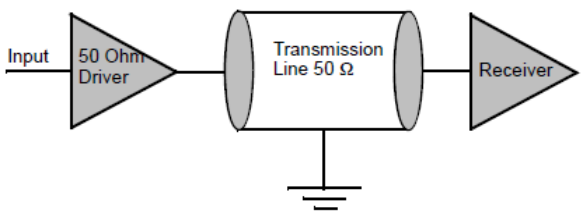


Figure 16. Simulation Results With Source Impedance Matched, Output Measured at Receiver End, 2-inch Trace Length

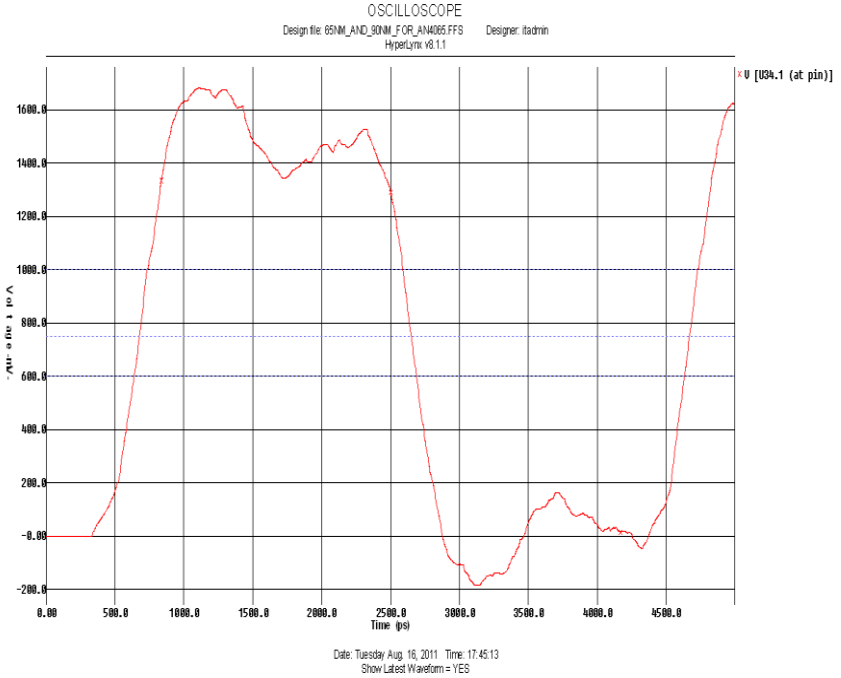
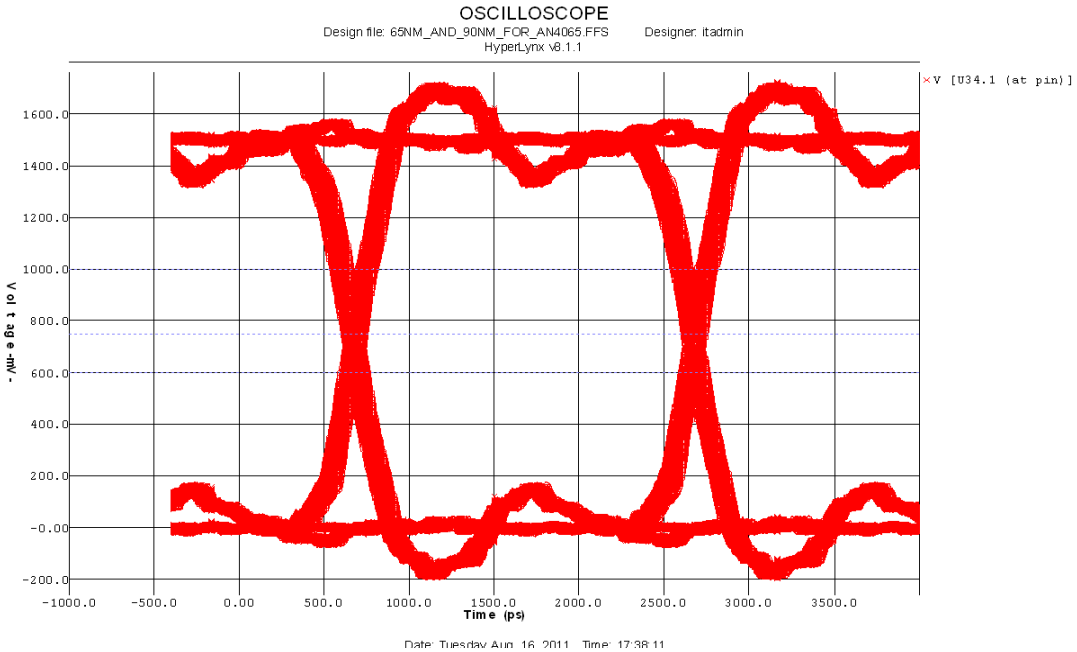


Figure 17. Eye Diagram for Source Impedance Matched Case



Active Pull-up Termination to V_{TT} at the Load

Figure 18 shows an active pull-up termination scheme, where the terminating resistor (R1 = Z_O) is tied to a termination voltage (V_{TT}). In this scheme, the voltage (V_{TT}) is selected so that the output drivers can draw current from the high- and low-level signals. However, this scheme requires a separate voltage source that can sink and source currents to match the output transfer rates.

Figure 19 shows the Hyperlynx simulation results of this termination scheme. The trace length is 2 inch with a frequency of 250 MHz. The output has a voltage swing from 318 mV to 1.2 V. Figure 20 shows the Eye diagram for the corresponding termination scheme with 1% Gaussian noise added. The eye height is 0.75 V, and eye width is 2 ns. The reflections compared to the source terminated case are minimal.

There have been cases where the value of R1 has been increased to increase the voltage swing at the load. If the source impedance is matched, then the reflections are absorbed at the source-end. The load-end shows an increase in the voltage swing due to the presence of a reflection coefficient, which is in turn present because of impedance mismatch at the load.

Figure 21 shows the termination scheme using 150 Ω. Figure 22 shows the simulation results with R1 = 150 Ω. The voltage swing with 150 is from -100 mV to 1.42 V. Although the recommendation is to have R1 = 50 Ω, R1 can be increased to obtain higher voltage swing provided the source impedance is matched. If the source impedance is not matched, the reflections come back to the load-end and the signal integrity is poor.

Figure 18. Active Pull-Up Termination Scheme Using 50 Ω

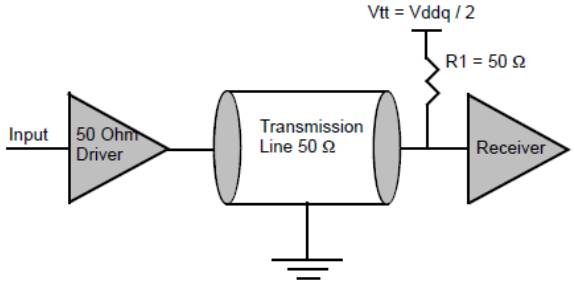


Figure 19. Simulation Results for R1 = 50 Ω Active Pull-Up Termination. Output Measured at Receiver End

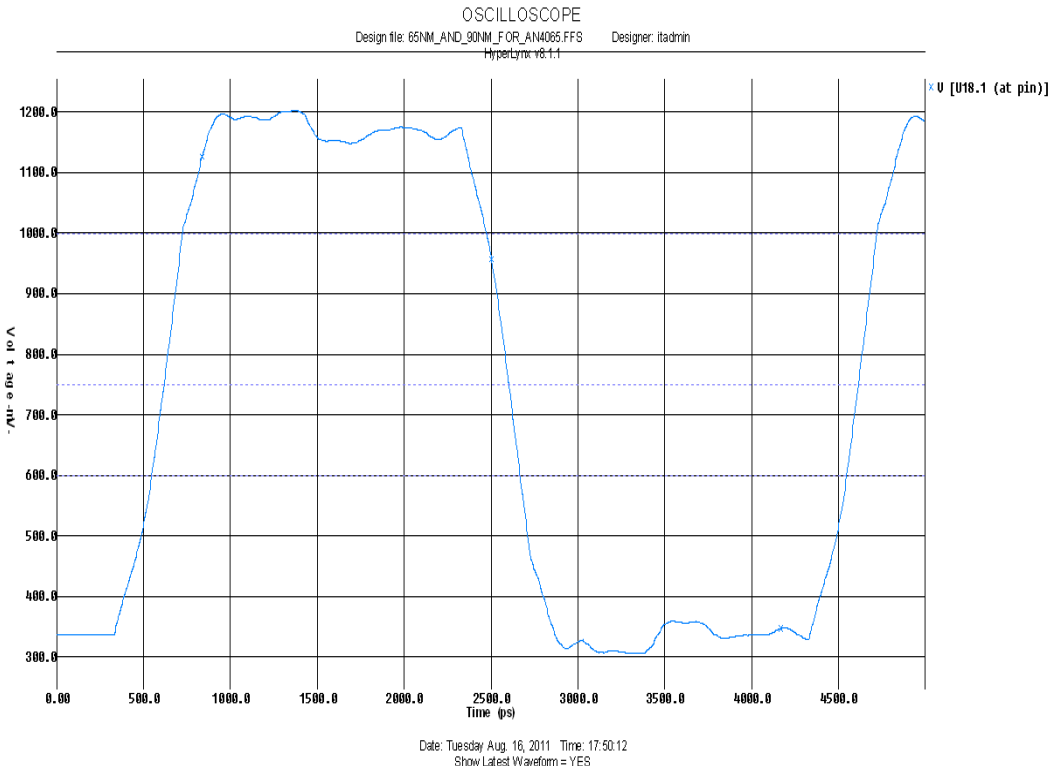


Figure 20. Eye Diagram for R1 = 50 Ω Active Pull-Up Termination Case

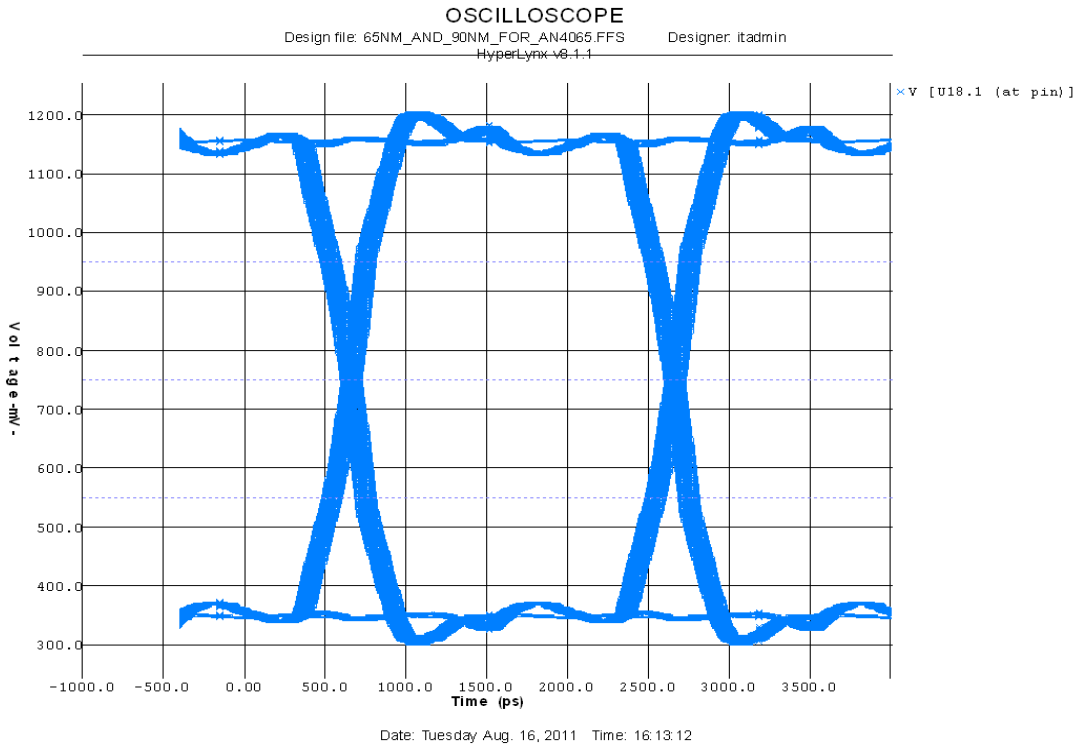


Figure 21. Active Pull-Up Termination Scheme Using 150 Ω

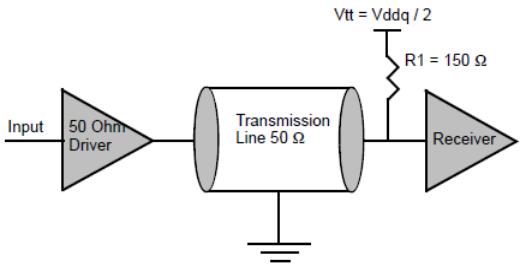


Figure 22. Simulation Results for R1 = 150 Ω Active Pull-Up Termination. Output Measured at the Receiver End (2-inch Trace length)

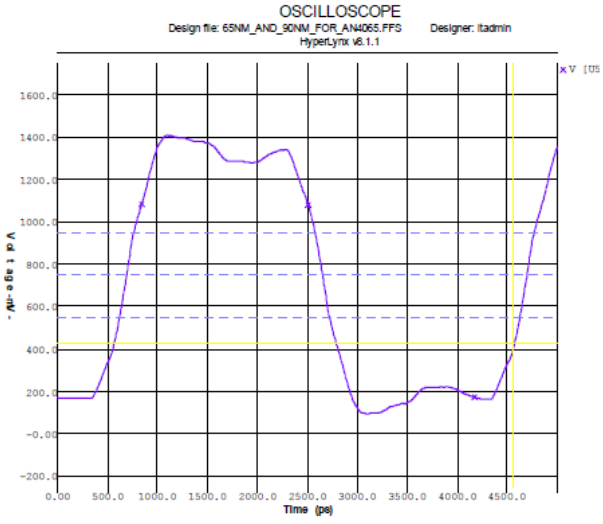


Figure 23. Simulation Result From Active Pull-Up Termination Scheme Using 50 Ω

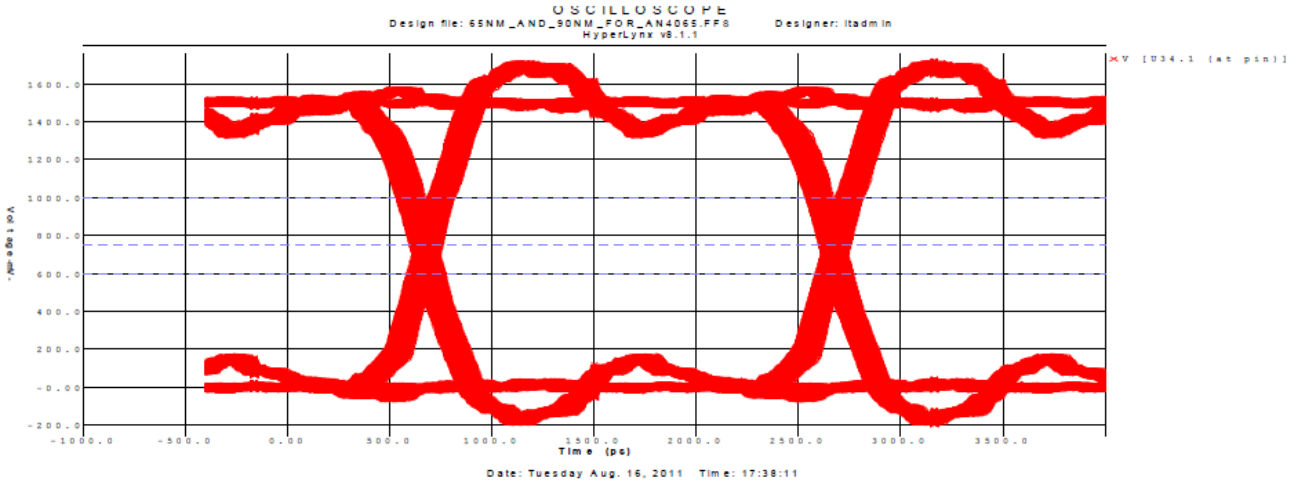


Figure 24. Measurement Results from Pull-Up Termination

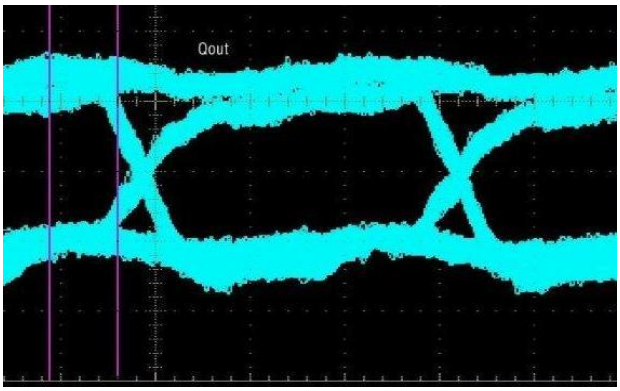


Figure 23 shows the simulation carried out from the topology shown in Figure 21 that has a single pull-up termination at the receiver end. Figure 24 shows the results from measurement of the board that has the same termination topology. The single pull-up receiver termination is the most recommended termination for the HSTL standard.

A special case of the Active Pull-up Termination scheme is when a stub is introduced after the termination resistor. Depending on the board layout, the stub cannot be avoided in some cases.

Series Resistance on Both Ends (Bidirectional I/Os Only)

In a series resistance termination scheme, the termination resistor matches the impedance at the signal source instead of matching the impedance at each load. Figure 25 shows a series resistance termination scheme, terminated on both ends for bidirectional I/Os. The sum of Rs and the impedance of the output driver must be equal to Z_O. By setting the output driver to minimum impedance mode, you can add a series resistor to match the signal source to the line impedance. The advantage of series resistance termination is that it consumes less power. However, the disadvantage is that the rise time degrades because of the increased RC time constant. Setting the driver to the minimum impedance mode on the DDR-I/DDR-II devices gives the user the highest drive strength possible.

Figure 26 shows the simulation results for the termination scheme shown in Figure 25. The simulation has been done with Rs = 50 Ω at the load end. The voltage swing for this scheme is from 130 mV to 1.38 V. The waveforms may not reach rail for high frequencies, because of the RC time constant being larger in this scheme.

Figure 25. Series Resistance Termination

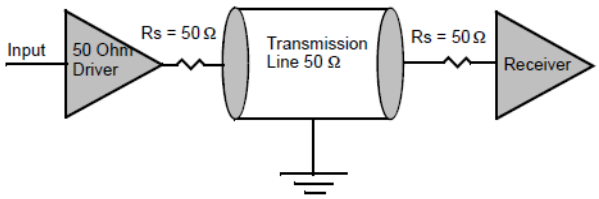


Figure 26. Using 50-Ω Series Resistances on Both Ends

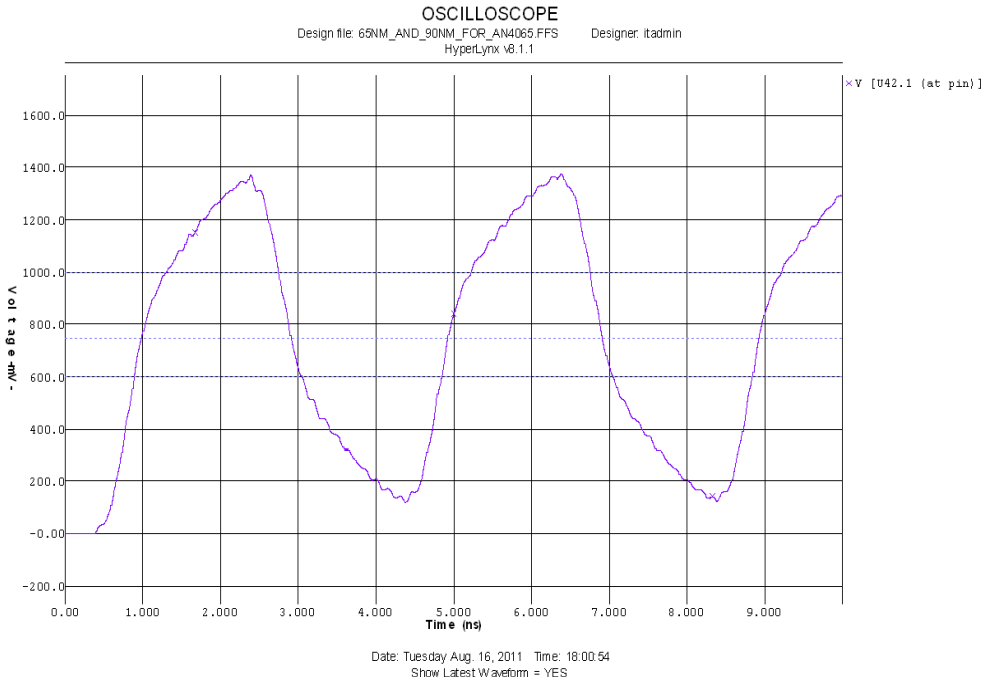
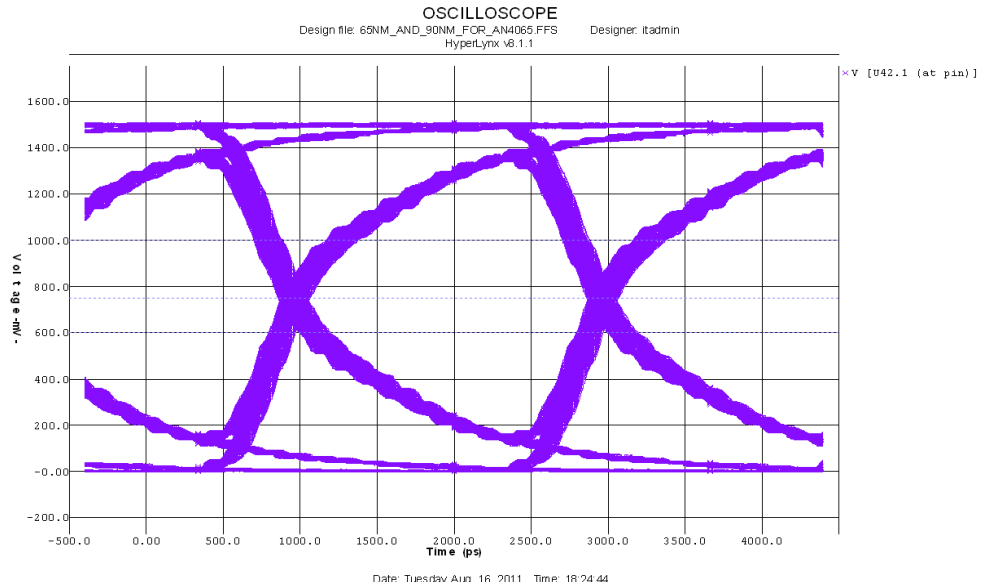


Figure 25 shows the eye diagram for the series resistor termination scheme shown in Figure 25. The eye width is 1.66 V, and the eye height is 931 mV.

Figure 27. Eye Diagram for Series Resistors Termination Case



Active Pull-up Termination to V_{TT} On Both Ends (Bidirectional I/Os Only)

Figure 28 shows an active pull-up termination scheme, where the terminating resistor (R1 = Z_O) is tied to a termination voltage (V_{TT}). This is same as the active pull-up termination scheme shown in Figure 18, the only difference being the active pull-up is present on both ends. The active pull-up on the source end shown in Figure 28 is actually load termination when the bus turns around (this scheme is for bidirectional buses). Figure 29 shows the same scheme using 150-Ω resistors on both ends.

Figure 30 shows the simulation results with R1 = 50 Ω and 150 Ω. The concept of 150-Ω usage explained in the active pull-up termination scheme holds true for this example also. As seen in the simulation waveform, the 150 Ω has higher swing compared to 50-Ω termination. If the source end cannot have 50-Ω driver, then it is best to have a 50-Ω termination at the load.

Figure 28. Active Pull-Up Termination Scheme for Bidirectional I/Os using 50 Ω

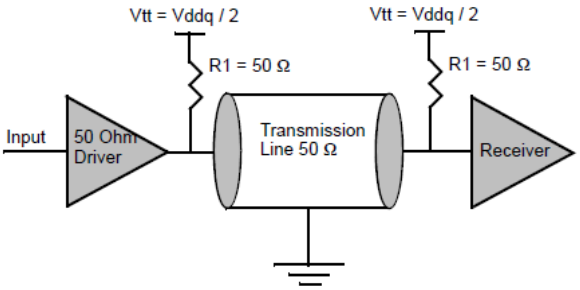


Figure 29. Active Pull-Up Termination Scheme using 150 Ω

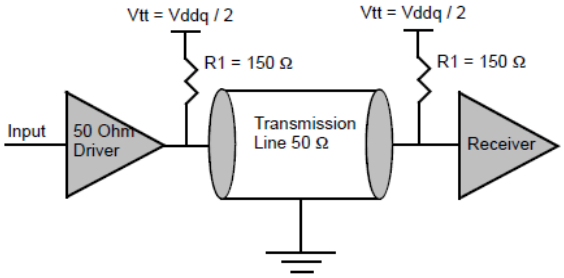
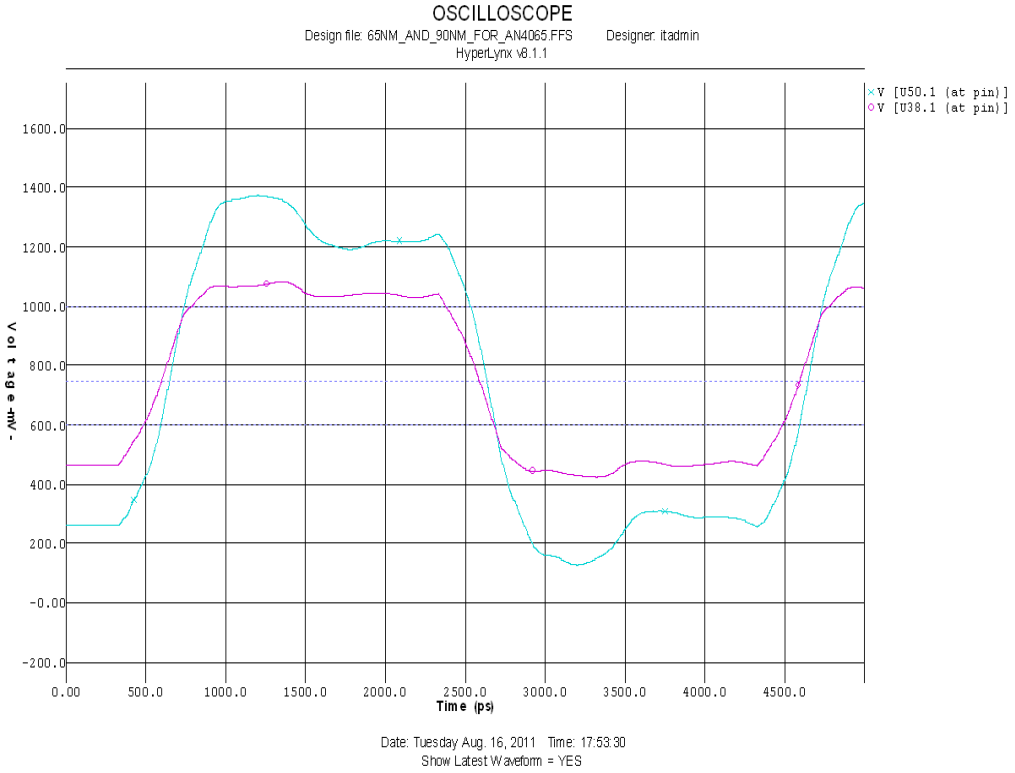


Figure 30. Simulation Results With R1 = 50 Ω and 150 Ω, Output Measured at Receiver End, 2-inch Trace Length



As seen in Figure 30, the voltage swing for the Active Pull-up termination using 50 Ω is from 425 mV to 1.1 V, and for the Active Pull-up termination of 150 Ω is from 130 mV to 1.38 V.

One more method that can be followed (bidirectional I/Os) for short trace lengths is to have a single active pull-up termination in the middle of the transmission line. This is efficient only if the trace length on both sides of the termination is small enough that the traces do not act as a transmission line any more.

Termination Schemes for Multi-Receiver Topologies

Previous sections covered single driver and single receiver topologies. Many customers have a need to use multiple memories as receiver with a single driver such as a memory controller. This section examines the schemes and guidelines for multiple receivers. In the case of two memories being driven by a single controller as shown in Figure 31. A single trace driven by the memory controller splits into two, it is recommended that the trace impedance of 100 Ω each be used, including the termination of 100 Ω for each receiver.

Figure 32 below shows the waveform for one of the receivers.

Figure 31. Active Pull-Up Scheme for Two Receivers

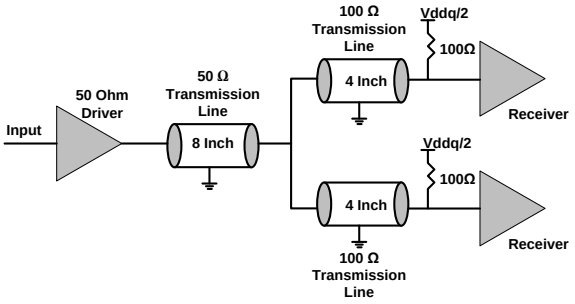
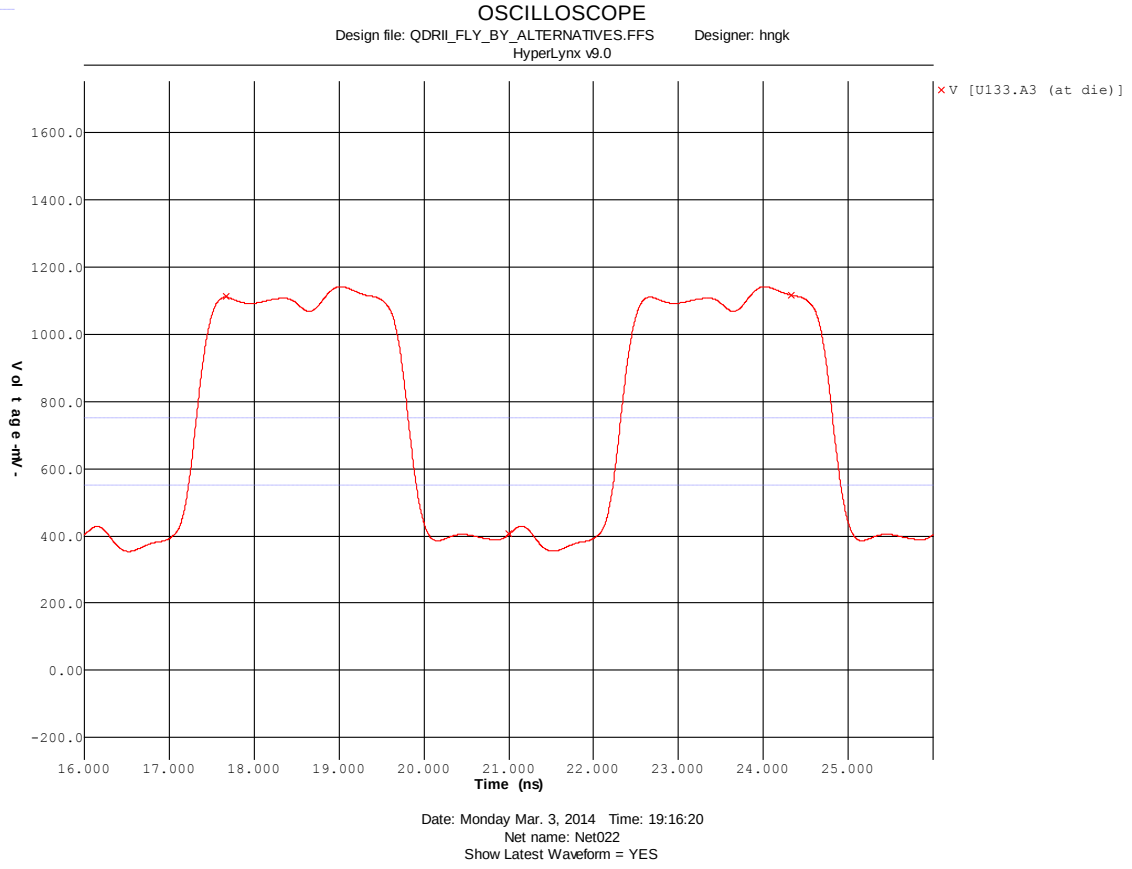


Figure 32. Simulation Results for Active Pull-Up Schemes for Two Receivers



Both waveforms at the receiver inputs will be identical because the lengths and impedances are matched.

A commonly used subset of this topology is the clam-shell topology, where the receivers are placed on top of either side of the board. This entails reducing the distance of the traces after the split and the need to use 100-Ω traces is not critical as long as the traces are short. Simulations must be done on the trace topology with the right driver and receiver models and to ensure the right trace impedances are used.

The split case and multi-receivers topologies are further explored in the following examples.

Figure 33 shows a basic “fly-by” termination scheme, simplified to have all receivers with no distance between the receivers. This is an ideal situation and is discussed for completeness. It does not matter where the termination is placed because at the receiver, there is only a single node.

Figure 33. Fly-By Topology: All Receivers Grouped Together

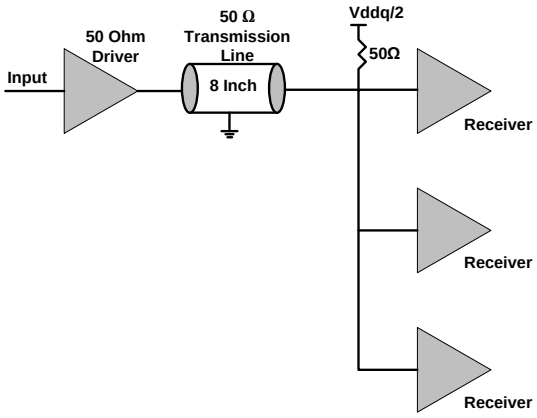


Figure 34 shows the waveform to be close to ideal, when a single termination is used for all the receivers.

Figure 34. Simulation Results for Fly-By Topology: All Receivers Grouped Together

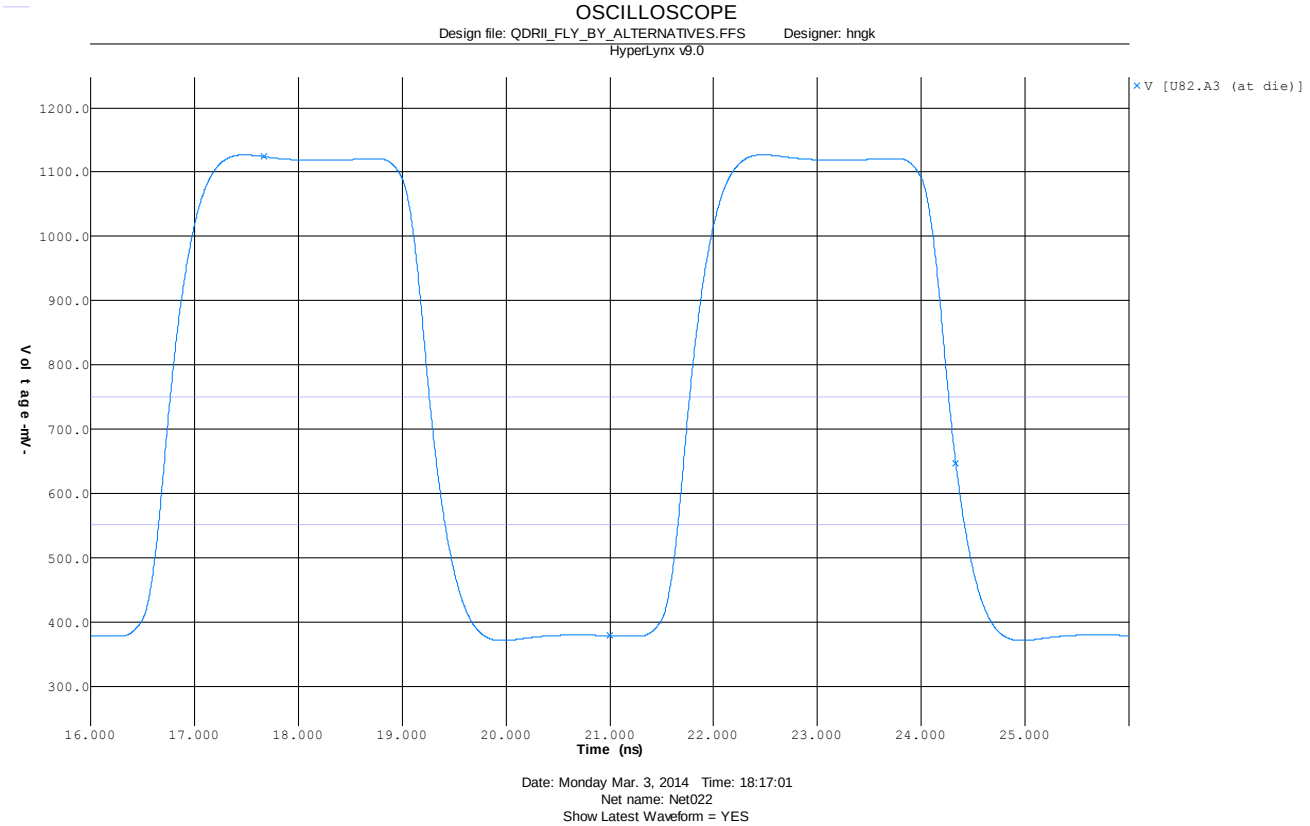


Figure 35 shows a more realistic fly-by topology where the distance between the receivers is 250 mils.

Figure 35. Fly-By Topology: 250-mil Separation Between Receivers

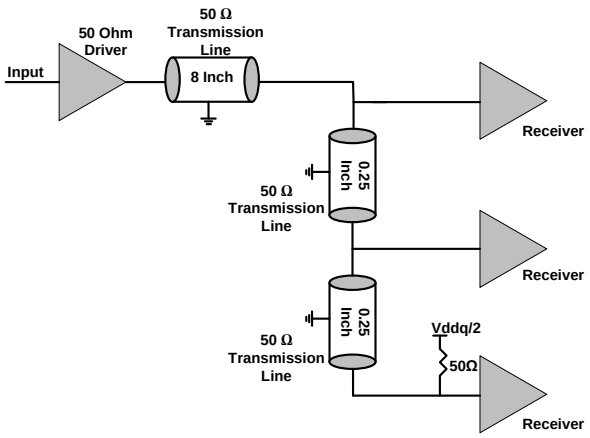


Figure 36 shows receiver waveforms. The first one is closest to the driver and the other which is slightly delayed is farthest away. The closest receiver sees some reflection at its input. While the reflection is not significant, increasing the number of receivers while maintaining the same trace distance of 250 mils between receivers will further degrade the waveform. One way to address this is by reducing the transmission line distance from 250 mils to say, 150 mils (150 mils is chosen as an example).

The effect of reducing the trace distance from 250 mils to 150 mils for the same 3-receiver topology is seen in Figure 37. The input to the first receiver shows no reflection.

Figure 36. Simulation Results for Fly-By Topology: 250-mil Separation Between Receivers

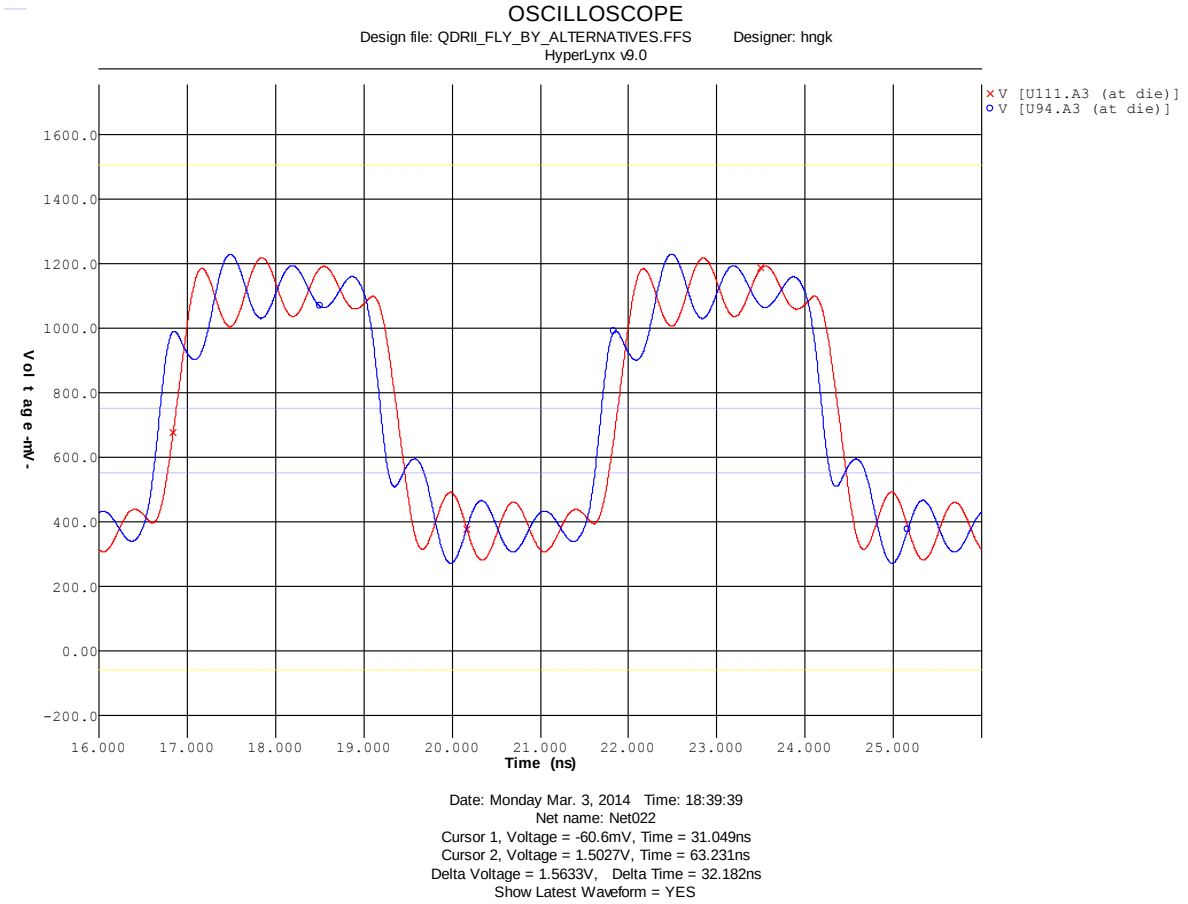
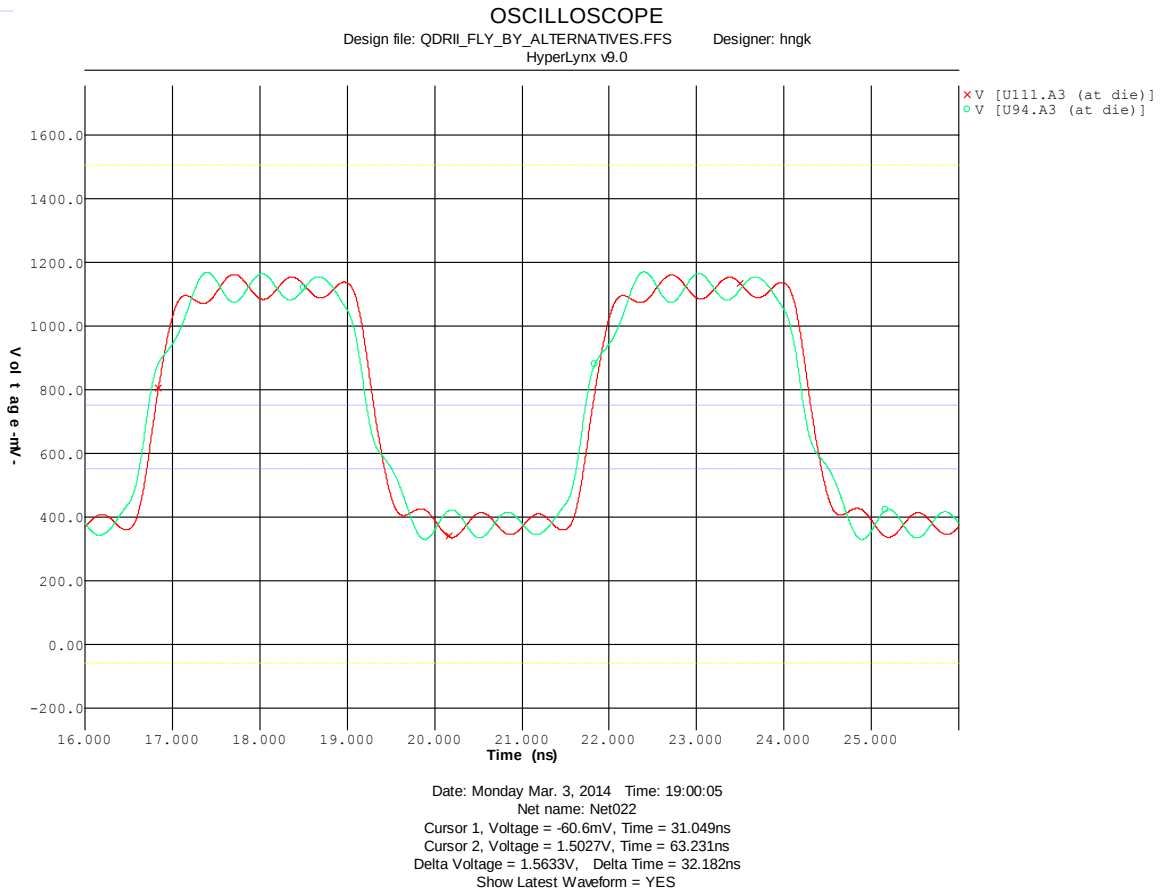


Figure 37. Simulation Results for Fly-By Topology: 150-mil Separation Between Receivers



In general, using more memories (receivers) to extend the topology shown in Figure 35 will cause waveform degradation unless the distances are reduced with more receivers.

Reference Schematic Design

This segment provides reference schematics for QDR-DDR II/II+/Xtreme devices. You can use these schematics, which are derived from an internal characterization board, as examples for your designs. However, you must perform signal integrity simulations before doing so.

Reference Schematic for QDR-DDR II/II+/Xtreme SRAMs (From the Internal Characterization Board)

Figure 38. QDR II/II+/II+Xtreme-DDR II/II+/II+Xtreme (Non-ODT) Reference Schematic—Part 1

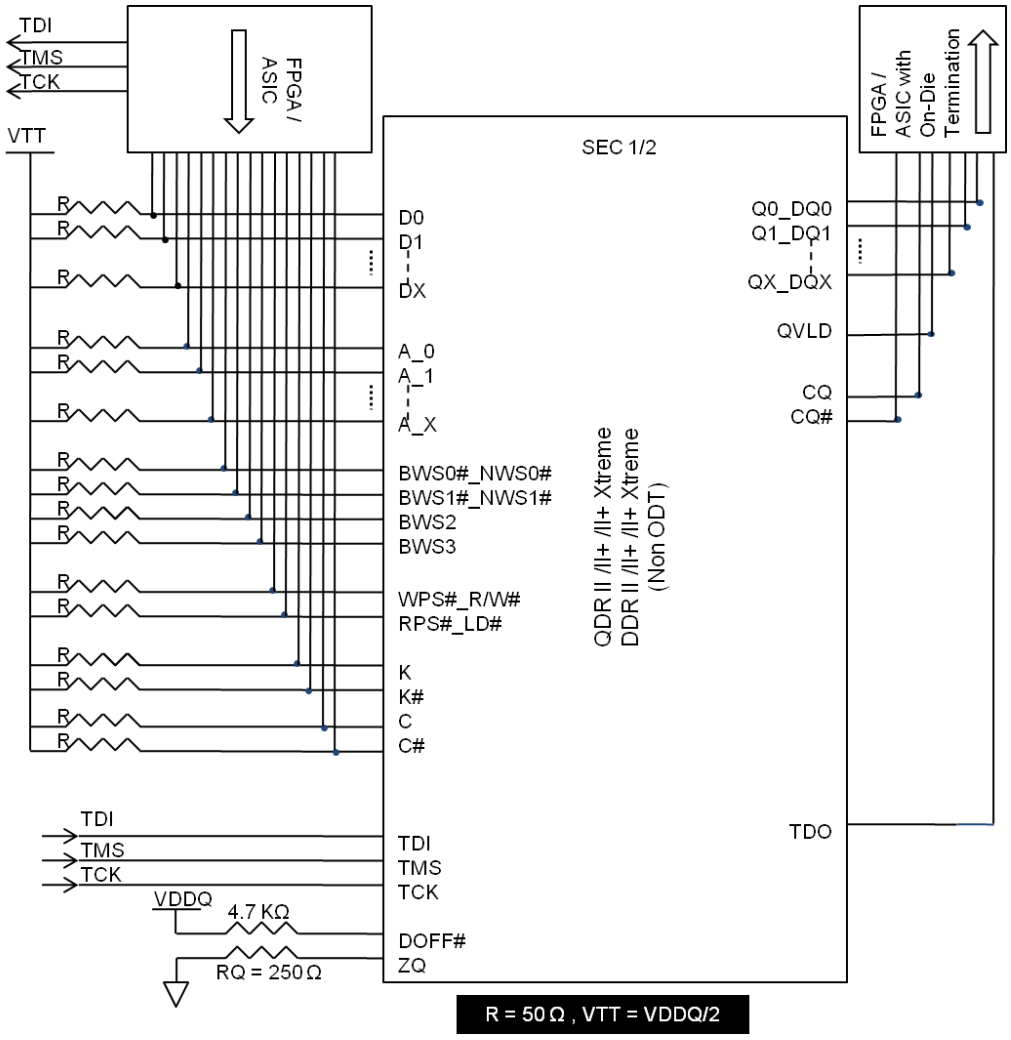


Figure 39. QDR II/II+/II+Xtreme-DDR II/II+/II+Xtreme (ODT) Reference Schematic—Part 2

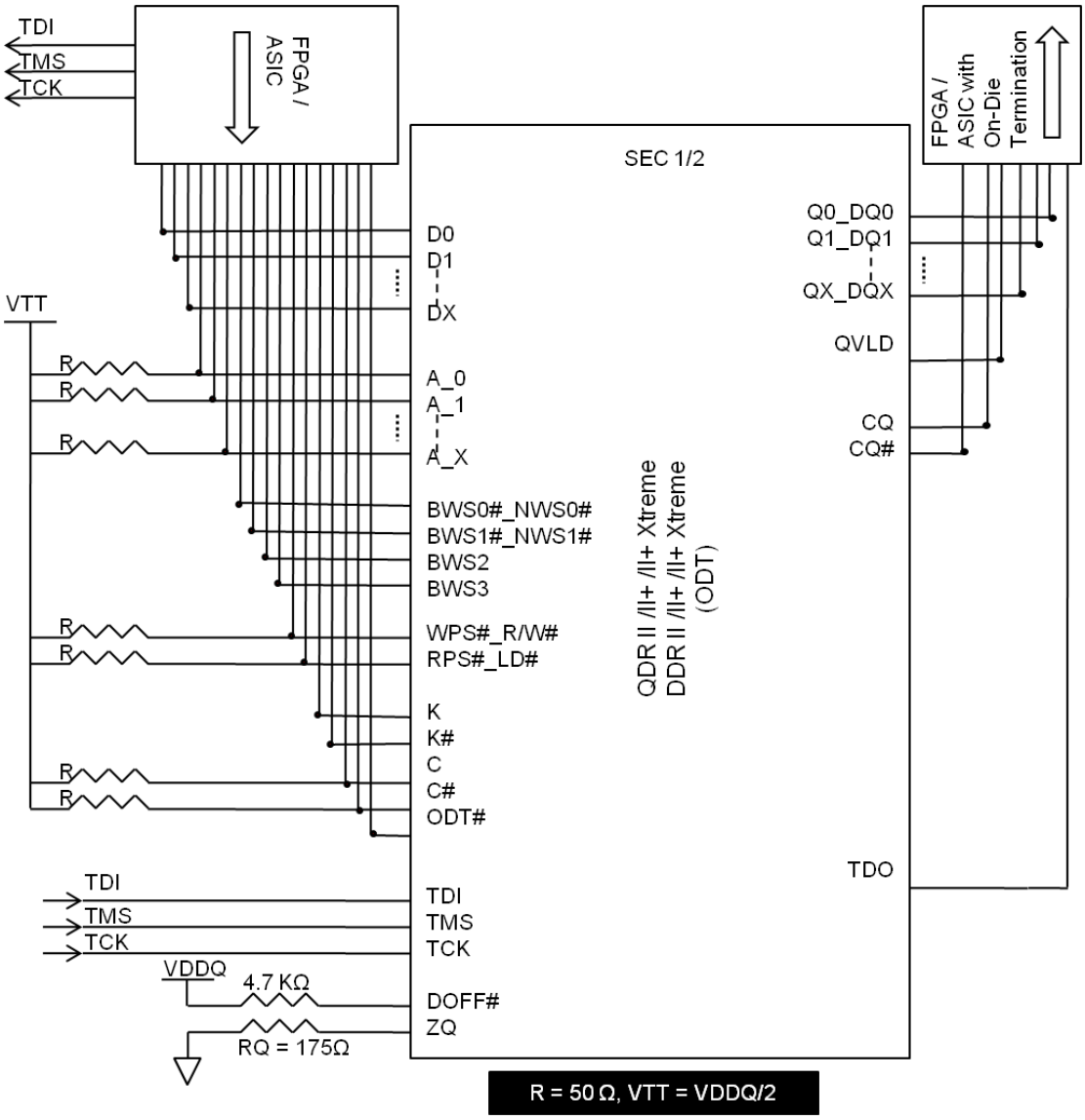
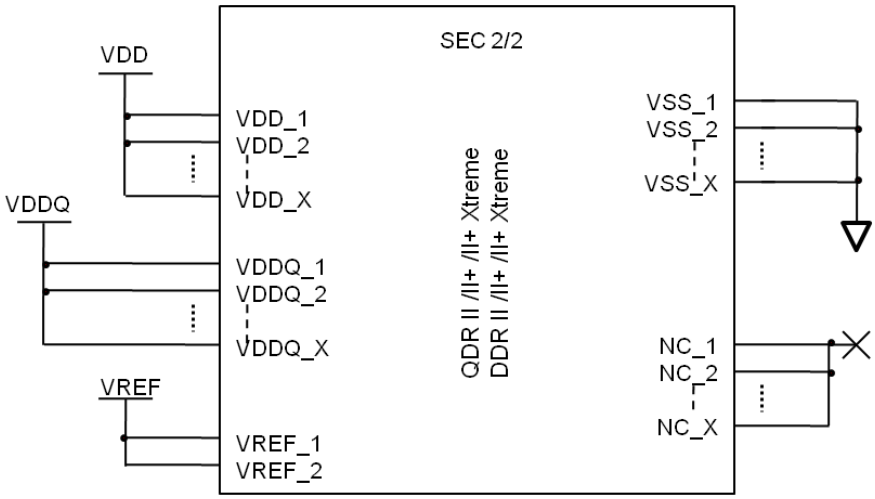


Figure 40. QDR II/II+/II+Xtreme-DDR II/II+/II+Xtreme (Supply Pins) Reference Schematic



Assumptions

- The reference schematics provided in this section are from an internal characterization board. Cypress recommends that you perform signal integrity simulations with specific board conditions before finalizing your design.
- Figure 38 and Figure 39 are the reference schematics for all non on-die termination (ODT) and ODT QDR-DDR II/II+/Xtreme SRAMs respectively. For example, if the part is an x18 device, then the data pin notation $D_{[x:0]}$ will be interpreted as $D_{[17:0]}$.
- QDR II+/II+Xtreme-DDR II+/II+Xtreme devices do not have the input clocks C and C#.
- Non-ODT QDR II+/II+Xtreme-DDR II/II+/II+Xtreme devices do not contain the ODT pin.
- ODT devices have an ODT feature for Data inputs ($D_{[x:0]}$), Byte Write Selects ($BWS_{[x:0]}$), and Input Clocks (K and K#). Therefore, there is no termination for the $D_{[x:0]}$, $BWS_{[x:0]}$, K, and K# pins shown in Figure 39.
- The Data output ($Q_{[x:0]}$) and Echo Clock (CQ/CQ#) signals drive the FPGA/ASIC without termination, considering the inputs of the FPGA/ASIC that supports ODT. In the case of FPGA/ASIC without ODT, Cypress recommends that you terminate (pull-up to V_{TT}) the Data output ($Q_{[x:0]}$) and Echo clock (CQ/CQ#) signals to reduce signal integrity issues.
- The value of the termination resistor (R) is 50 Ω because most designs have a trace characteristic impedance of 50 Ω. The termination resistor value must be equal to the characteristic impedance of the trace.
- Connect an external resistor, RQ, between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of RQ must be five times the value of the intended line impedance driven by the SRAM. As a result, the value of RQ is 250 Ω to match the output impedance of 50 Ω in Figure 38. The acceptable range of RQ that guarantees impedance matching with a tolerance of ±15% is between 175 Ω and 350 Ω, with V_{DDQ} = 1.5 V. The output impedance is adjusted every 1024 cycles upon power-up to account for drifts in supply voltage and temperature.
- The RQ is 175 Ω in Figure 39, considering the input impedance and ODT value of memory is 50 Ω, the ODT pin is LOW, and the output impedance is 35 Ω. If the output impedance needs to be 50 Ω, then Cypress recommends using a 15 Ω resistor in series with the output driver to match the trace impedance of 50 Ω. The other recommendation is to keep RQ equals to 250 Ω then the output driver impedance of memory is 50 Ω and with ODT pin low, the ODT value of memory is 75 Ω. In this case, the reflection co-efficient is positive with trace impedance of 50 Ω and customer does not need to use external resistors to match the impedance.
- Keep the termination resistors close to the device to reduce the stub length and, thereby, reduce reflections.

Decoupling Capacitor Recommendations for Power Supply Pins

- Decoupling capacitors on power-supply pins play a significant role in filtering noise in the power supply.
- Cypress recommends placing the decoupling capacitors close to the memory devices for best results.
- The decoupling capacitance for V_{DD}, V_{REF}, and V_{TT} can be identified using power integrity simulation tools. The selection of decoupling capacitors depends on board and device properties. Therefore, Cypress recommends performing power integrity simulation for high-speed systems before selecting the decoupling capacitor values for the respective power nets. The following decoupling capacitor recommendations are from an internal characterization board for your reference only:

Figure 41. Decoupling Capacitor Recommendation for V_{DD}

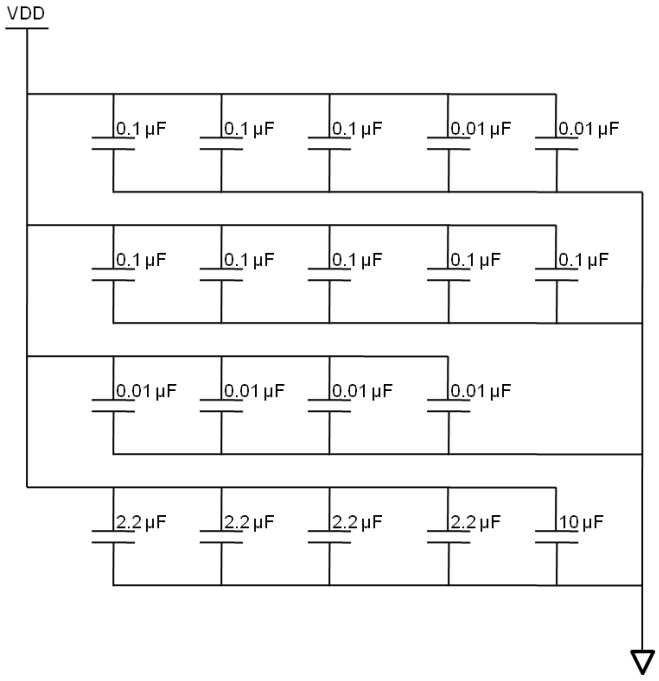


Figure 42. Decoupling Capacitor Recommendation for V_{DDQ}

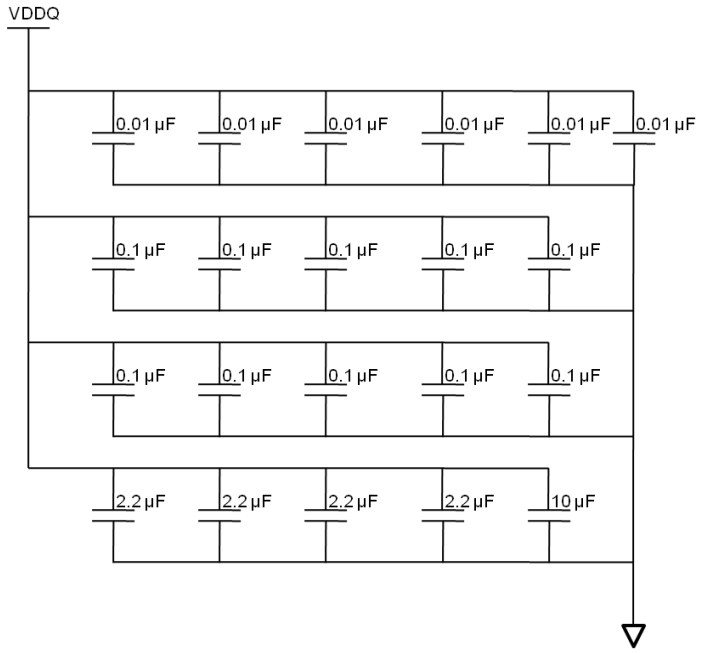


Figure 43. Decoupling Capacitor Recommendation for V_{TT}

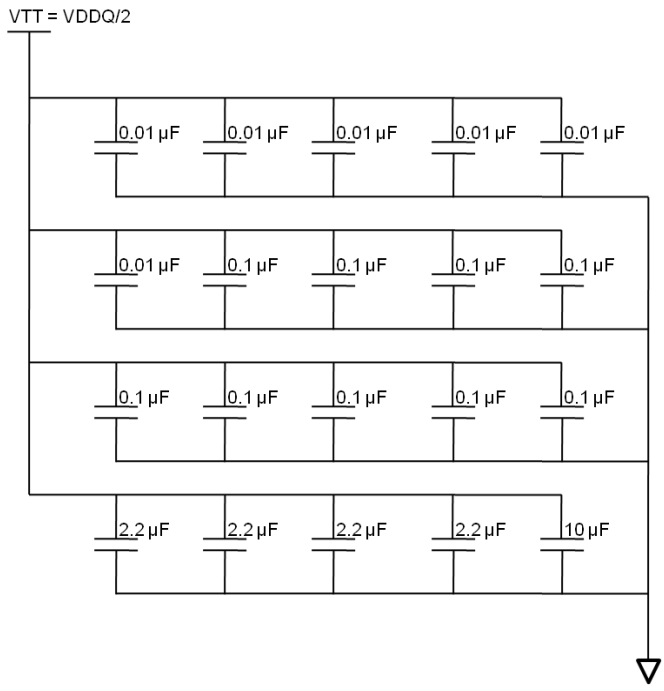
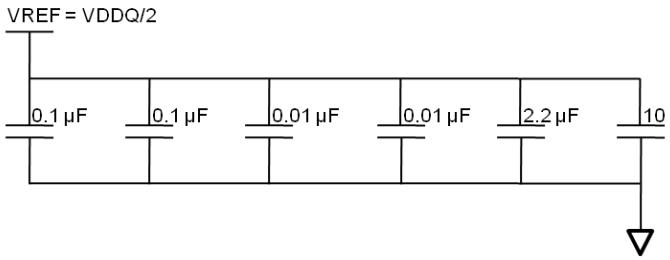


Figure 44. Decoupling Capacitor Recommendation for V_{REF}



If you face any issue while creating your design or if you want Cypress to review a schematic, create a technical support case at www.cypress.com.

Summary

As seen in this application note, high-speed bus design requires detailed analysis to ensure that the system works properly. Rigorous simulations with extracted layout, the right driver and receiver models are essential to ensure that the system works reliably as specified.

Document History

Document Title: QDR®-II, QDR-II+, DDR-II, and DDR-II+ Design Guide - AN4065

Document Number: 001-15486

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1051122	SFV	05/15/2007	New Application Note.
*A	1776708	VIDB	12/05/2007	Updated in new template. No Technical updates.
*B	3111380	VIDB	12/15/2010	No change in content.
*C	3338056	VIDB	08/05/2011	Updated Introduction. Updated Functional Description (Updated QDR-II and QDR-II+ Functionality and DDR-II and DDR-II+ Functionality). Updated Feature Set Explanation – QDR-II, QDR-II+, DDR-II, and DDR-II+ (Renamed “Clocking Strategies” as “Clocking Overview and Strategies” and updated the same section, updated Clock Startup, renamed “QDR-II and QDRII+ – Using Master Clock @ Controller (Input Clock K and K#)” as “Clocking Strategy 1: Using Input Clock K/K#” and updated the same section, renamed “QDR-II – Using Master Clock @ Controller (Input Clocks K, K#, C, C#)” as “ Clocking Strategy 2: Using Input Clocks K/K#, C/C#” and updated the same section, renamed “QDR-II and QDR-II+ – Using CQ and CQ# Provided by SRAM and Routed to the Controller” as “Clocking Strategy 3: Using Echo Clocks CQ and CQ#” and updated the same section, updated Summary of Clocking Strategies). Updated Signal Integrity and Layout Guidelines (Updated Matching Source Impedance to TX Line Impedance, updated Series Resistance on Both Ends (Bidirectional I/Os Only), and Active Pull-up Termination to V_{TT} On Both Ends (Bidirectional I/Os Only)). Updated in new template.
*D	3345310	VIDB	08/15/2011	Updated Termination Schemes (Updated Active Pull-up Termination to V_{TT} at the Load and Active Pull-up Termination to V_{TT} On Both Ends (Bidirectional I/Os Only).
*E	3558817	GOPA	03/23/2012	Added Signal Integrity and Layout Guidelines. Updated Termination Schemes (Updated Matching Source Impedance to TX Line Impedance, updated Active Pull-up Termination to V_{TT} at the Load, updated Series Resistance on Both Ends (Bidirectional I/Os Only)). Updated in new template.
*F	3739016	PRIT	09/12/2012	Replaced ‘Symmetrical Parallel Termination’ with ‘Active Pull-up Termination’ in section Active Pull-up Termination to VTT at the Load and Active Pull-up Termination to VTT On Both Ends (Bidirectional I/Os Only). Improved the clarity of the figures.
*G	4227355	PRIT	12/20/2013	Updated in new template. Completing Sunset Review.
*H	4316762	PRIT	03/21/2014	Added Termination Schemes for Multi-Receiver Topologies Added Reference Schematic Design
*I	4479402	DEVM	08/20/2014	Updated the “Assumptions” section of Reference Schematic Design Updated Decoupling Capacitor recommendations for Power Supply Pins

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