

# Generating a Power-Fail Interrupt using the F-RAM Processor Companion

## About this document

### Scope and purpose

AN400 describes the implementation of an early power-fail warning using the general-purpose comparator on the F-RAM Integrated Processor Companion. This warning signal can be used to drive a microcontroller interrupt input.

### Intended audience

It is intended for the users of F-RAM processor companions FM33xxx, FM31xxx.

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## 1 Overview

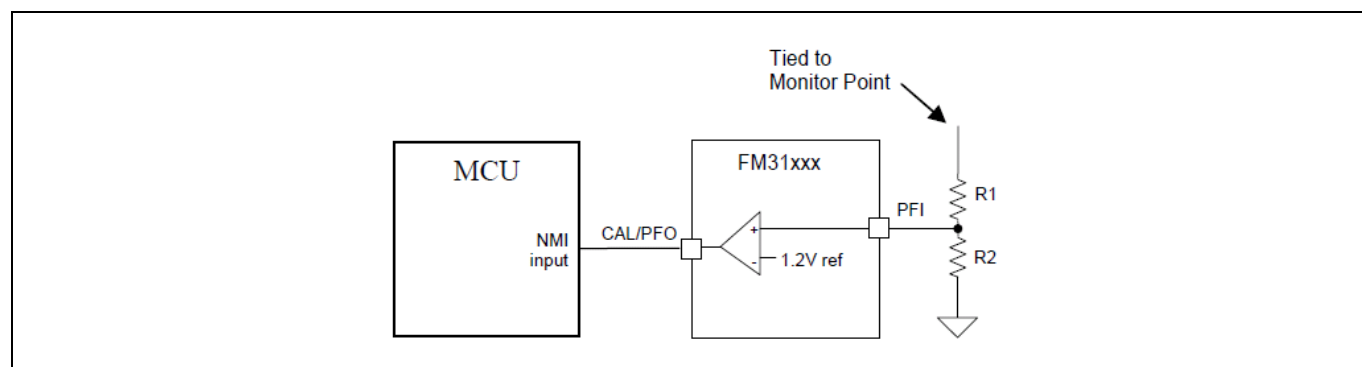
The F-RAM integrated Processor Companion features a general-purpose comparator that can be used to generate an early power-fail interrupt (PFI). This warning signal can drive a microcontroller interrupt input and must occur before  $V_{DD}$  drops too low to save all critical data to the nonvolatile RAM. The Processor Companion's early power-fail interrupt can also be used as a warning to the system to stop conducting critical activity during a brownout condition.

### 1.1 Power Supply Monitoring

The power supply can be monitored using the F-RAM Processor Companion family of products. The FM31xxx family is an I<sup>2</sup>C interface product and the FM33xxx family is an SPI interface product. As shown in **Figure 1**, an analog comparator compares the PFI input pin to an onboard reference voltage. When the PFI input voltage drops below the reference threshold, the comparator will drive the PFO output pin (ACS pin on FM33xxx and CAL/PFO pin on FM31xxx) to a LOW state. This early power-fail warning can be used as a system interrupt for a host microcontroller. This application note shows two implementations using this comparator. The FM31xxx family is used in this document.

*Note: The FM33xxx comparator is similar to FM31xxx, except for a change in the comparator reference voltage. The reference voltage in the FM33xxx is 1.5 V, while it is 1.2 V in the FM31xxx comparator.*

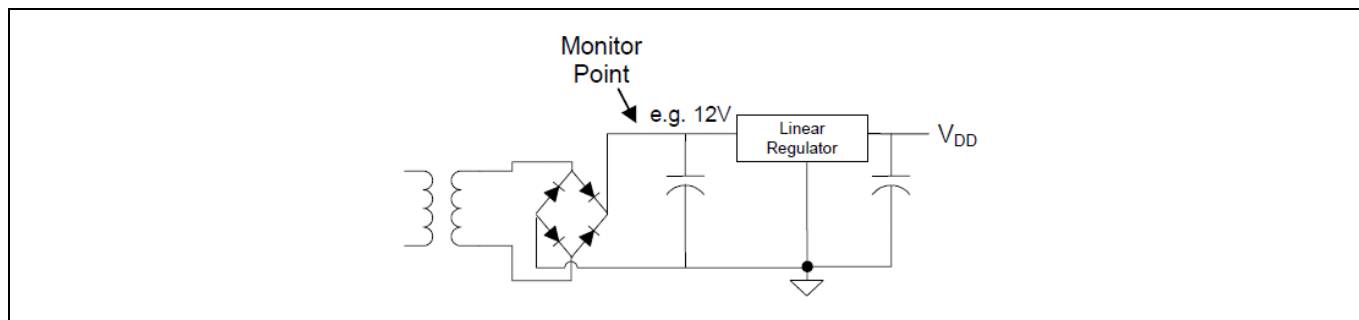
In a typical system, the comparator's output is tied to the non-maskable interrupt (NMI) input of a microcontroller as shown in **Figure 1**. The comparator provides a single input (PFI pin) for monitoring voltage. The other comparator input is tied to an on-board 1.2-V precision reference (1.5 V in FM33xxx). Since the comparator is non-inverting, the output will drive to a low state when the PFI input drops below 1.2 V. To use this function as a PFI, the PFI input should be connected to the power supply voltage to be monitored through a voltage divider.



**Figure 1** System Hookup and Monitor Point

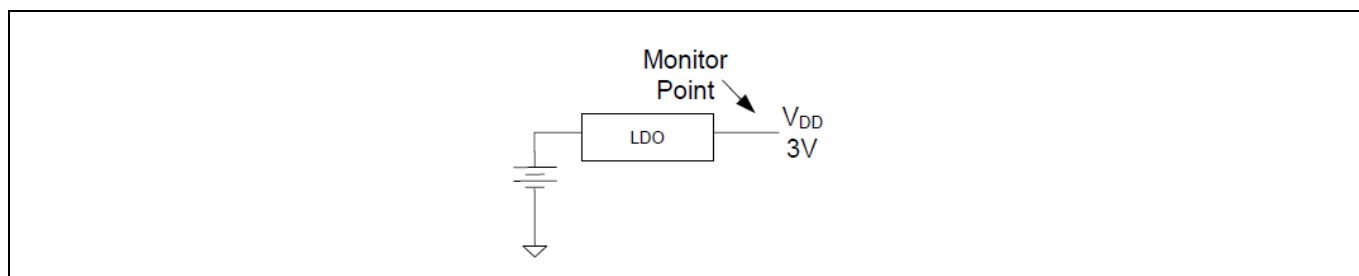
**First Method:** AC line-operated systems use voltage-regulated power to provide a stable voltage to guarantee circuit operation. The regulator is always preceded by an unregulated power supply. As the unregulated voltage varies, the regulated voltage remains stable – to a point. Hence, during a power failure or system shutdown, the unregulated supply voltage will begin to drop before the regulated output ( $V_{DD}$ ) is affected. Therefore, by generating an NMI when the unregulated power supply voltage drops below a threshold, the processor and the memory subsystem know that power will be lost well before the regulator drops out. A common line-operated power supply that is well suited to this type of application is shown in **Figure 2**.

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**Figure 2** Line-Operated Power Supply

**Second Method:** A regulated LDO output ( $V_{DD}$ ) can be monitored for a drop below a selected threshold so that the interrupt occurs at a higher voltage than the processor reset trip point. A typical battery-based power supply that is suited to this approach is shown in [Figure 3](#).



**Figure 3** Battery-based Power Supply

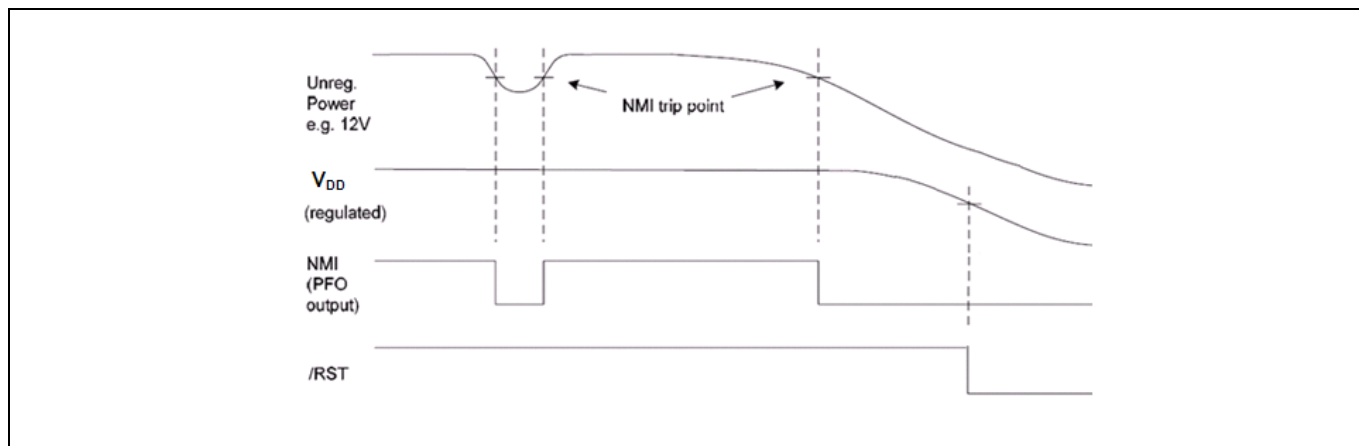
In the first method, the interrupt is generated in response to a voltage drop on the regulator's unregulated side, that is, 12 V in the example application given in [Figure 2](#). This will occur well before the regulated output ( $V_{DD}$ ) drops. In the second method, the power supply is a primary battery with a low dropout (LDO) regulator. The LDO output may begin to drop soon after the battery voltage falls, so it can more accurately monitor  $V_{DD}$  directly. Most LDO regulators exhibit a linear relationship between  $V_{IN}$  and  $V_{OUT}$  when  $V_{IN}$  drops below  $V_{OUT}$ .

The early power-fail comparator can support either approach, but the first method provides a warning much earlier.

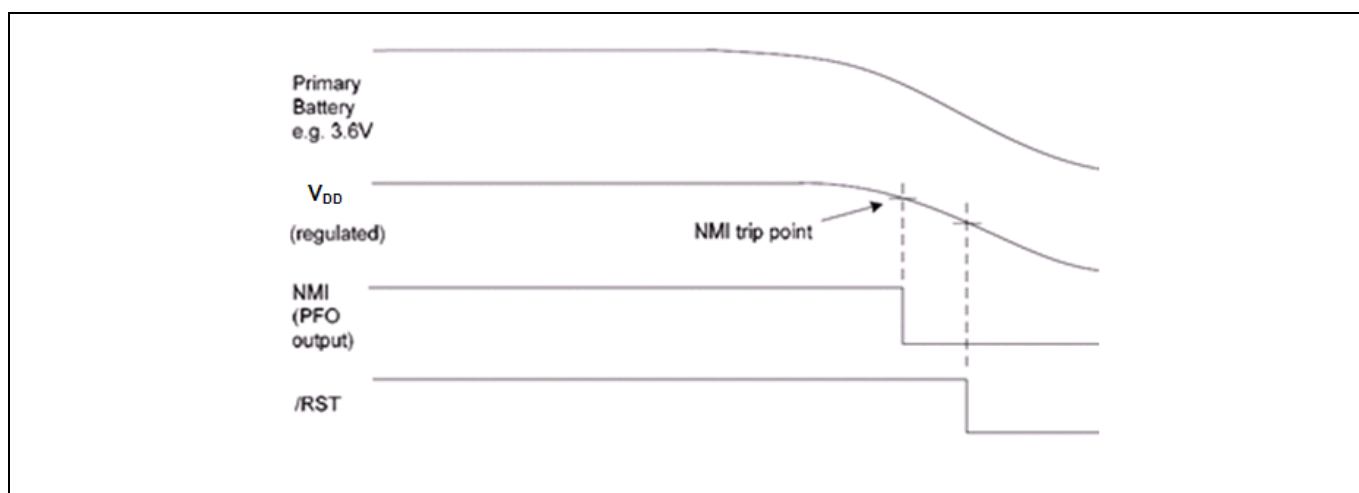
In the case of monitoring an unregulated power supply (first method), power loss due to a brownout condition and complete power down are shown in [Figure 4](#). An interrupt is generated well before  $V_{DD}$  drops because the monitored voltage occurs at an earlier point in the power supply. In the case of a primary battery (second method) shown in [Figure 5](#),  $V_{DD}$  is directly monitored and there is no brownout case.

To trigger the NMI, as shown in [Figure 4](#), the NMI trip point must be carefully chosen. The goal is to generate an NMI signal as soon as possible when power drops, but not generate an NMI within the normal tolerance or ripple of the power supply, yet not so late that the voltage regulator starts to drop out.

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**Figure 4** Power-down Events for Line-Operated Supply



**Figure 5** Power-down Events for Battery Supply

**Example:** A 12-V power supply with a  $\pm 10\%$  tolerance is allowed a 10.8-V output level; therefore, the PFO pin should be set to trip no higher than 10.3 V to provide an additional 0.5-V margin. A lower limit on the supply trip point is the minimum  $V_{IN}$  specification for the linear regulator. A LDO regulator requires very little headroom whereas a conventional linear regulator needs more input voltage. For example, a 5-V linear regulator may have a dropout specification of 2 V, meaning that  $V_{OUT}$ , or system  $V_{DD}$ , will begin to drop when the input voltage reaches 7 V. Therefore, in this example, the PFO trip point should be set between 10.3 V and 7 V.

The power supply sense circuit is a simple voltage divider, tied to the unregulated supply with the tap point connected to the PFI pin, which is the input to the on-chip comparator. The resistor values are chosen to generate an NMI when the divided voltage on the PFI input goes below the 1.2-V comparator reference (1.5 V for FM33xxx). The trip point is defined by a simple resistor divider ratio.

*Note:* Ensure the PFI pin voltage level cannot exceed  $V_{DD} (min)$ .

The equation is:

$$V_{TRIP} \times \frac{R2}{R1 + R2} = 1.2 \text{ V}$$

For example, if the power supply is  $12 \text{ V} \pm 10\%$ , the regulated output  $V_{DD}$  is  $5 \text{ V} \pm 10\%$ , and the desired NMI trip point  $V_{TRIP}$  is 9 V, then the divider ratio  $R2 / (R1 + R2)$  is 0.133.

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Note: Resistors R1 and R2 are labeled in [Figure 1](#).

$$\text{We know, } 0.133 = \frac{R2}{R1 + R2}$$

$$\text{And, } R1 + R2 = \frac{R2}{0.133}$$

$$\text{So, } R1 = \frac{R2}{0.133} - R2$$

For R2 = 47 kΩ, R1 = 306 kΩ

The easiest solution is to choose one resistor and then solve for the other.

## 2 Additional Considerations

The slew rate of the power supply on the unregulated side can dictate the amount of time that is available for backing up data after an NMI occurs and before a reset occurs. For example, assume the nominal 12-V supply has a slew rate of 0.5 V/ms. In this example, an NMI is generated at 9 V, and the 5-V linear regulator begins to drop out at 7 V. The NMI will occur 4 ms before the regulator drops out causing the F-RAM Processor Companion  $V_{DD}$  input level to drop. The comparator is a convenient way to generate an interrupt, which provides enough time for the processor to save critical data to the nonvolatile RAM. It can also be used to poll the power conditions. After the NMI occurs, it is advisable to monitor the signal continuously and to avoid conducting critical activity until the NMI clears. If the NMI is the result of a brownout, then eventually the condition will clear and normal operation can resume. If it is not a brownout, the reset pin ( $\overline{RST}$ ) will eventually be asserted.

### 3 Summary

From this application note it is clear that system designers can use the F-RAM Processor Companion for dual purposes in a system. In addition to being an F-RAM nonvolatile memory, it can be used to generate a power-fail interrupt to the host controller, which eliminates a separate power-fail detection circuit. A well-implemented early power-fail detection signal can give the host controller enough time to prepare the system for a power down.

### 4 Related Application Notes

You can refer to the following application notes for better understanding of the F-RAM Processor Companion devices.

- [AN407 - A Design Guide to I2C F-RAM Processor Companions – FM31278, FM31276, FM31L278, and FM31L276](#)
- [AN408 - A Design Guide to SPI F-RAM Processor Companion - FM33256B](#)
- [AN401 – Charging Methods for the F-RAM RTC Backup Capacitor](#)
- [AN402 - F-RAM RTC Oscillator Design Guide](#)
- [AN404 - F-RAM RTC Backup Supply \(VBAK pin\) and UL Compliance](#)

**Revision history**

Document version	Date of release	Description of changes
**	2013-06-07	New Spec.
*A	2014-11-06	Changed title from “Generating a Power-Fail Interrupt using the F-RAM Processor Companion Power-Fail Comparator” to “Generating a Power-Fail Interrupt using the F-RAM Processor Companion”. Added Related Application Notes
*B	2016-06-02	Updated to new template.
*C	2017-08-17	Updated logo and copyright.
*D	2021-05-26	Updated to Infineon template.



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