AN34359

PCB Layout Guidelines for West Bridge™ Generation A Peripheral Controllers in Wafer Level Chip Scale Package

Associated Project: No

Associated Part Family: West Bridge® Astoria™, West Bridge® Arroyo™, West Bridge® Antioch™

Software Version: NA

Related Application Notes: None

To get the latest version of this application note, or the associated project file, please visit http://www.cypress.com/go/AN34359.

The West Bridge™ peripheral controllers support high-speed USB as well as mass storage access and are available in a wafer level chip scale package (WLCSP) with 81-balls. The size of this package is less than 4 x 4 mm with a 0.4 mm pitch. This application note discusses the PCB layout guidelines for West Bridge controllers in the WLCSP.

Introduction

The West Bridge™ controllers support high-speed USB and mass storage access. These controllers provide access from a processor interface and a high-speed USB (HS-USB) interface to the peripherals: SD, MMC/MMC+, CE-ATA, and NAND. The West Bridge controllers support interleaving accesses between the processor interface, the HS-USB, and the peripherals. Therefore, an external processor and an external USB host can transfer data to each other, and to the mass storage peripherals, simultaneously.

The West Bridge controllers are available in two packages, a 100-ball very fine ball grid array (VFBGA) package and an 81-ball WLCSP.

This application note discusses the PCB layout guidelines for West Bridge controllers in the WLCSP.

Package Overview

The West Bridge peripheral controllers are available in an 81-ball WLCSP. Table 1 summarizes the critical dimensions for the PCB layout design. The Table 1shows the package diagrams.

Table 1.Package Dimensions for West Bridge WLCSP

Parameter	Size
Package Size	3.784 x 3.788 x 0.55 mm
Ball Count	81
Ball Pitch	0.4 mm
Ball Diameter	0.26 mm

PCB Layout Guidelines

West Bridge controllers in WLCSP have 81-balls, with a 0.4 mm pitch. Due to the space constraints, routing all the signals successfully may require up to eight PCB layers.

All the outermost rows of pads must be routed on the top PCB layer. A 5 mil trace width is recommended on the top and bottom layers.

Figure 1. Example Top Layer

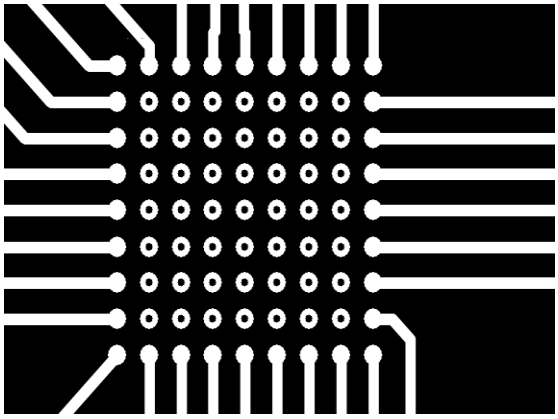
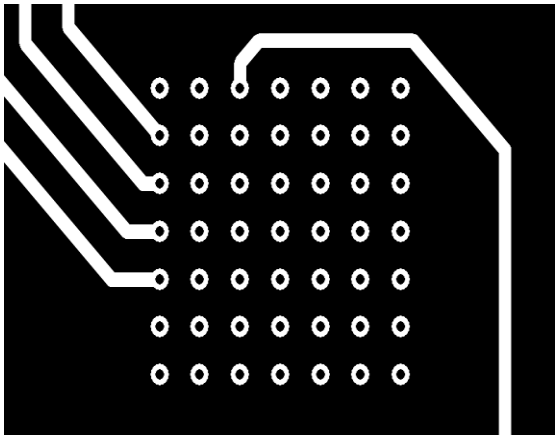
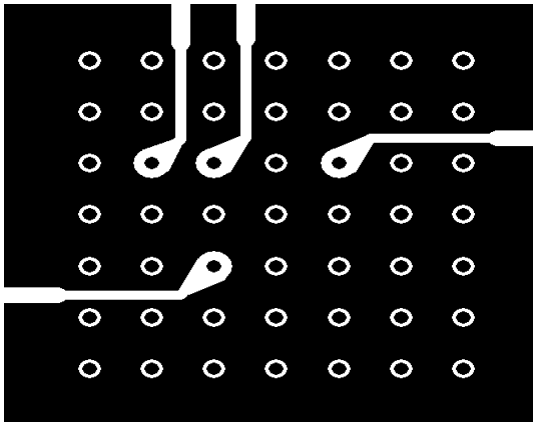


Figure 2. Example Bottom Layer



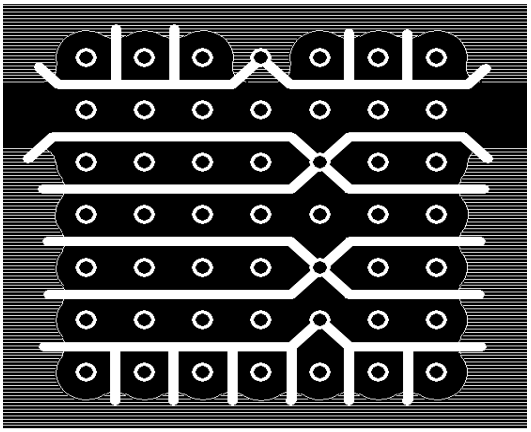
- For pads in the inner rows, use the ‘via in pad’ technology. A 4.3 mil drill hole diameter can be used for the vias. The recommended pad diameter is 10.5 mils. The size and the layout of the vias and through capture pads, it significantly impact the available routing space. The drill hole must be plugged and planarized to create a flat surface. This prevents the solder from wicking through the holes during the assembly process.
- For the inner layers, a 3 mil trace width must be used neck down. Once the trace exits the pad array, the standard trace and space geometry can be used.
- The traces must be teardropped on the inner layers as shown in Figure 3.

Figure 3. Teardrop Traces on Inner Layers



- When the power plane is split, the recommended pattern is as in Figure 4. A 3 mil wide trace must be used to connect the power and the ground pins to the plane outside the ball array.
- To ensure reliable signal integrity, the trace lengths between the West Bridge controller and the USB connector must be less than 2 inches.

Figure 4. Recommended Pattern for Connecting Power and GND Pins



Summary

West Bridge peripheral controllers in WLCSP provide a significant advantage in terms of board space, which is critical in handset solutions.

This application note enables manufacturing high density PCBs with West Bridge peripheral controllers in WLCSP, with high yields.

Additional Resources

1. AN1168 – High-speed USB PCB Layout Recommendations
2. West Bridge® Antioch Advance Datasheet
3. West Bridge® Astoria Advance Datasheet
4. Errata Document for West Bridge® Astoria

Appendix A

Figure 5. Package Diagram for West Bridge Antioch in WLCSP – 001-13820 *G

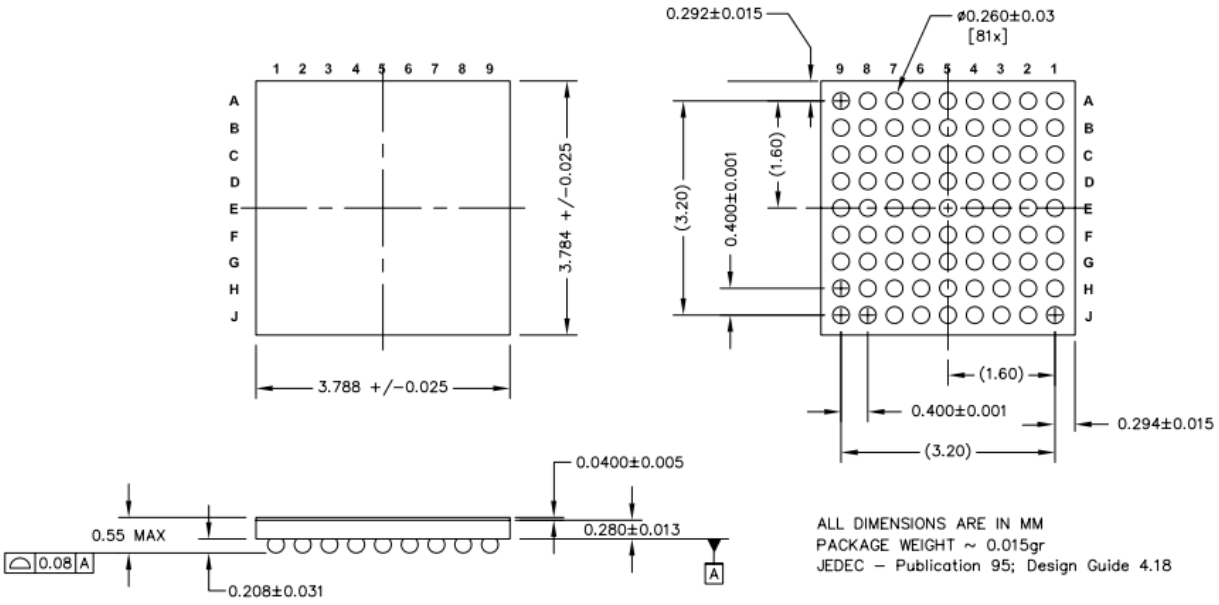
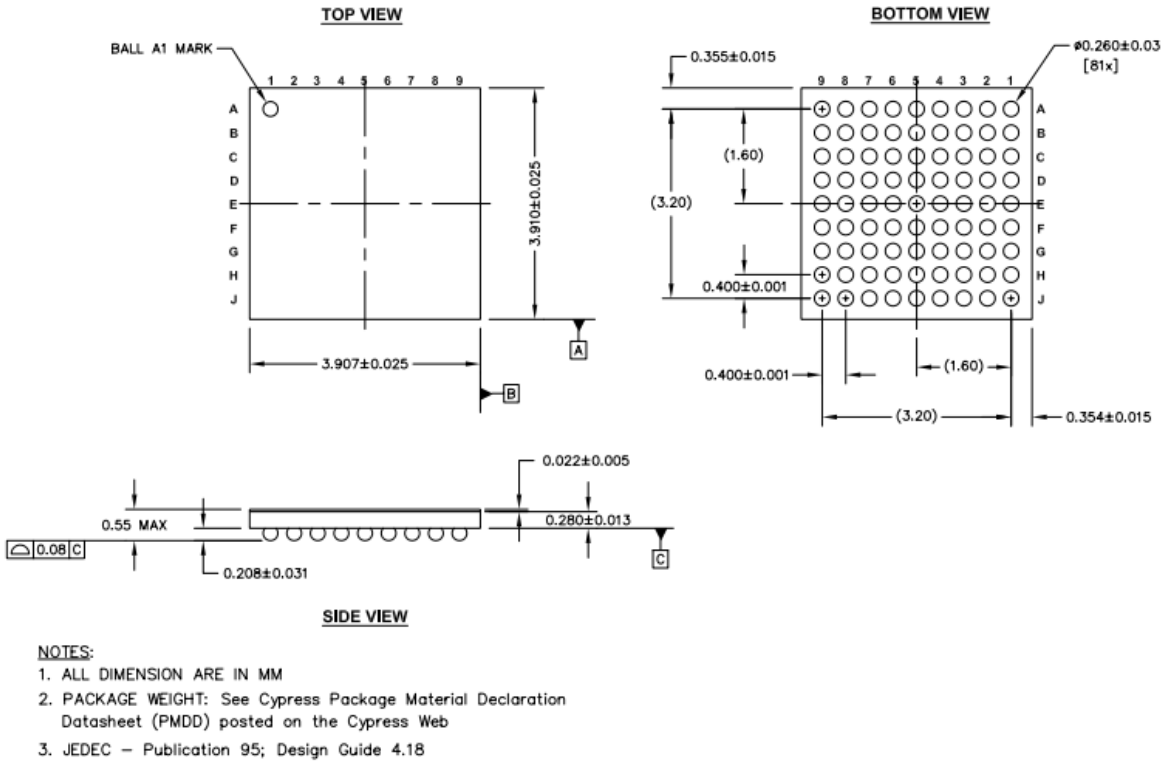


Figure 6. Package Diagram for West Bridge Astoria in WLCSP - 001-45618 *D



NOTES:
1. ALL DIMENSION ARE IN MM
2. PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress Web
3. JEDEC – Publication 95; Design Guide 4.18

Document History

Document Title: AN34359 - PCB Layout Guidelines for West Bridge™ Generation A Peripheral Controllers in Wafer Level Chip Scale Package

Document Number: 001-34359

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1508344	OSG	09/25/2007	New application note.
*A	2664370	OSG	02/25/2009	Updated PCB Layout Guidelines.
*B	3160320	ANOP	02/14/2011	Updated Document Tile to read as “PCB Layout Guidelines for West Bridge™ Generation A Peripheral Controllers in Wafer Level Chip Scale Package”. Updated Abstract. Updated Introduction. Updated Package Overview. Updated PCB Layout Guidelines. Added Additional Resources. Updated Summary. Updated Appendix A (Added Figure 6).
*C	3416346	PRVE	10/20/2011	Updated to new template. Completing Sunset Review.
*D	4566212	PRVE	11/10/2014	Updated to new template. Completing Sunset Review.
*E	5877280	AESATMP9	09/13/2017	Updated package diagrams for 001-13820 from *E to *G, 001-45618 from *B to *D and Updated logo and copyright.

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