# BGF153

## Integrated Fuse in CSP

## Protection device for overcurrent and Electrical Over Stress (EOS)

## Application Note AN260

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| **Page** | **Subjects (major changes since last revision)** |
|---|---|
| All | Remove of related content for BGF137, because EOL. |
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# 1 Introduction

## 1.1 Integrated Fuse

State-of-the-art electronic devices and products always require sufficient protection against electrical overstress (EOS) and electrostatic discharge (ESD) events in order to prevent personal injuries, product malfunctions and to fulfill quality standards and regulations.

Typically lithium-ion batteries may rupture, ignite, or explode when exposed to high temperatures and possibly catch fire because of battery cell overheating in case of short-circuiting. In some cases adjacent cells may also then heat up and ignite or explode. In the event of fire, the battery can emit toxic smoke and also ignite other adjacent devices. Therefore, battery powered as well as mains powered equipment need careful EOS protection that would switch off the power supply before the battery will explode. For that purpose the BGF153 fuse was introduced to the market. It offers one of the smallest Chip Scale Package with the smallest sizes available in the market. The wafer level package is a green package with a size of only 0.58 mm x 0.28 mm and a total height of 0.15 mm (**Figure 1**).


**Figure 1** Package Configuration and Schematic Diagram of the BGF153

## 1.2 Working principles

In the normal operating conditions as shown in the **Figure 2** system current flows through the BGF153 into IC pin. The fuse introduces a very low resistance to the circuit of less than 100 mΩ.

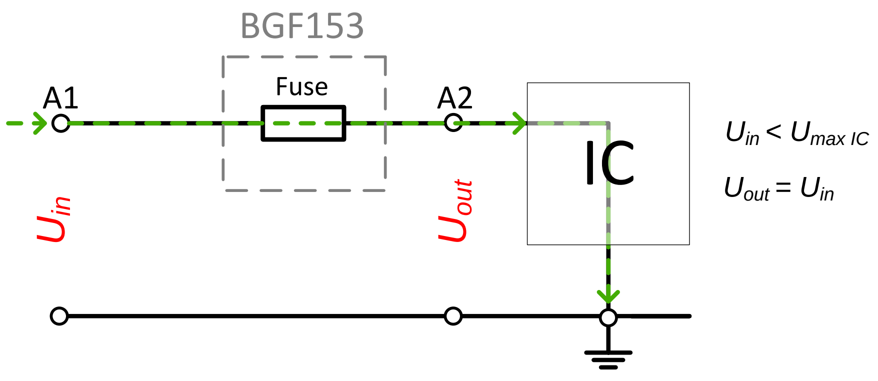


**Figure 2** Schematic Diagram of the BGF153 connected to an IC und normal operating conditions

In case of an overvoltage event, or in case of an IC malfunction (short inside the IC), transient current as demonstrated in **Figure 3** flows directly in the IC and may cause a severe heat generation in the IC.

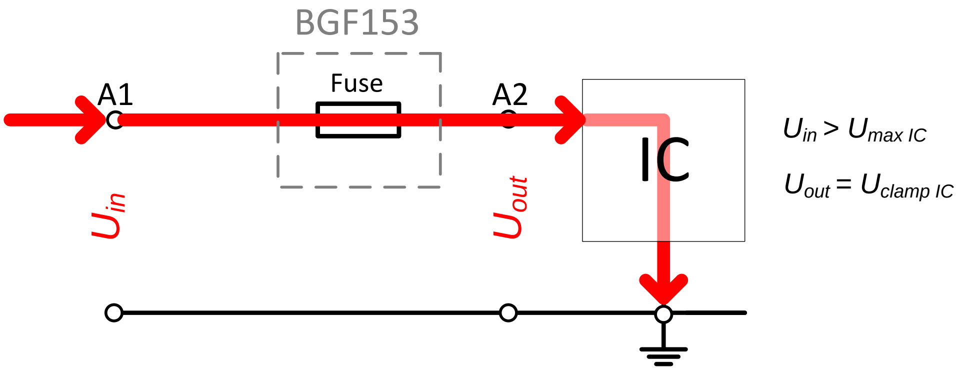


**Figure 3** Schematic Diagram of the BGF153 connected to an IC in case of an overvoltage event

When the overcurrent mode persists for a certain time, the fuse suffers from very strong self-heating process and blows. Physically, it means that the fuse turns into an open circuit and isolates the IC from the input stage of BGF153 as shown the **Figure 4**.

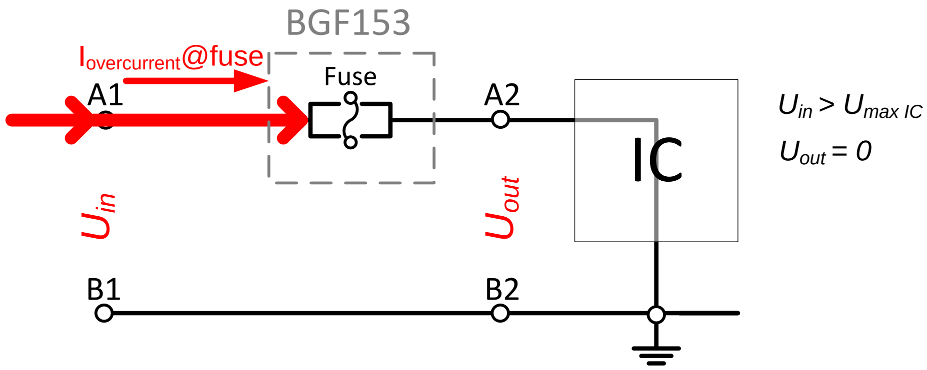


**Figure 4** Schematic Diagram of the BGF153 connected to an IC in case of a constant overcurrent

Regarding a system level ESD strike according IEC61000-4-2, the BGF153 is restricted to +-4kV (more than 8kV HBM). Using the ESD153 direct at the Vcc port (e.g. charging port), normally a TVS diode is placed in front anyway to catch the ESD strike before and to protect the IC regarding ESD stress. A huge capacitor between the BGF153 fuse must be avoided. Otherwise the entire ESD strike is discharged into the capacitor via the BGF153 fuse. The fuse can be damaged. As higher the capacitor value would be, as more ESD charge is passed via the fuse to the capacitor.

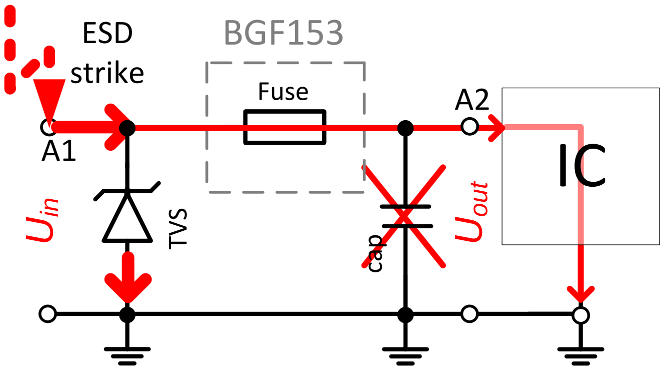


**Figure 5** TVS for System Level ESD protection in front of the BGF153 and the IC

## 1.3 Target Applications of BGF153

The Infineon's Fuse Product Family is targeting the following application areas:

- Electronic equipment for communications, office productivity and entertainment
- Smart phones, low-cost phones, MP3 players and GPS navigation systems
- Tablet PCs, notebooks, netbooks, calculators, mobile phones, phablets
- Subcomponents of the mobile devices where the interfaces require security from overcurrent events
- Digital cameras and players and recorders using video media such as DVDs, VCRs or camcorders, audio equipment, televisions, set-top-boxes
- Power management, power supplies and every system where batteries and battery chargers involved

## 1.4 Key Features of BGF153 Fuse

The key features of the BGF153 can be highlighted as:

- RoHS and WEEE compliant package
- Very small form factor (0.58 mm x 0.28 mm x 0.15 mm)
- 1 channel fuse:
  - Nominal operating current 0.75 A / Fusing current 2 A
  - Fast fusing time, $t_F$ 100 ms @ 2 A and 25 °C ambient
  - Very low fuse resistance, R < 100 mΩ

## 1.5 Package Outline and Bottom View of the BGF153

Following figure shows schematic symbol and bottom view of the BGF153:

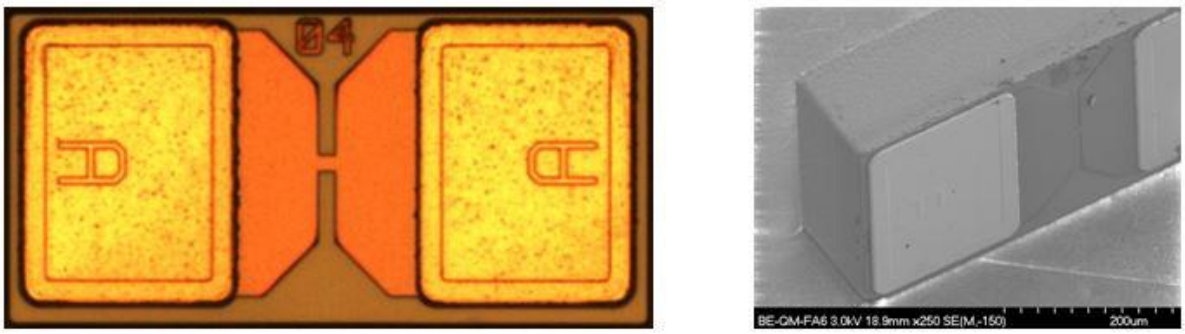

**Figure 6** Package outline and bottom view of the BGF153

## 1.6 DC Characteristics of BGF153

**Table 1 DC Characteristics for BGF153** at $T_A$ = 25 °C, unless otherwise specified

| Parameter | Symbol | Value | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Fuse resistance | R | – | 0.09 | 0.1 | Ω | $I$ = 100 mA |
| Fusing time | $t_F$ | – | 1 | – | ms | $T_A$ = 25 °C, $I$ = 2 A |
| | | – | – | 100 | | $T_A$ = -30 °C, $I$ = 2 A |
| Fuse life time | $t_L$ | 1000 | | | | $T_A$ = 25 °C, $I$ = 0.75 A |
| Insulation resistance post fusing | $R_i$ | 0.1 | 20 | – | MΩ | 2 A forced current<br>20 V compliance |

# 2 Fuse Characteristics

This section covers the electrical performance of the fuse shown in **Figure 1**. The electrical characteristics of BGF153 fuse are presented and gathered in this section.

## 2.1 Maximum Ratings of BGF153

The maximum ratings of the BGF153 fuse are limited mainly by the thermal resistance $R_{th}$ of the Fuse, PCB metal routing and thermal characteristics of the PCB material and are given in the **Table 2**:

**Table 2** **Maximum Ratings** at $T_A$ = 25 °C, pin A1 to A2, unless otherwise specified[1)]

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Operating temperature range | $T_{OP}$ | -30 | - | +85 | °C |
| Storage temperature range | $T_{STG}$ | -55 | - | +150 | °C |
| Fuse resistance at 100mA | $R_{fuse}$ | - | 0.09 | 0.1 | Ω |
| Fusing time at 2 A, -30 °C | $t_F$ | - | - | 100 | ms |
| Fuse lifetime at 0.75A at 25 °C | $t_L$ | 1000 | 200000 | | h |
| Insulating resistance post fusing [4)] | $R_I$ | 0.1 | 20 | - | MΩ |
| Electrostatic discharge according to IEC61000-4-2 [3)] | $V_E$ | -4 | – | 4 | kV |

1) BGF153 soldered on the reference PCB with thermal resistance (junction/ambient) 200 K/W

2) Contact discharge IEC61000-4-2 ($R$ = 330 Ω, $C$ = 150 pF)

## 2.2 Fuse Resistance

For applications involving battery recharger where the fuse element is located between a power management and external recharger, the fuse has to show the lowest possible electrical resistance in order to limit the voltage drop across it. BGF153 provides a slightly higher fuse resistance in range of 85 mOhm over the typical charger current window (200 mA up to 1 A). The flatness of the fuse resistances as functions of DC rated current and as a function of the ambient temperatures are shown in the **Figure 7.**

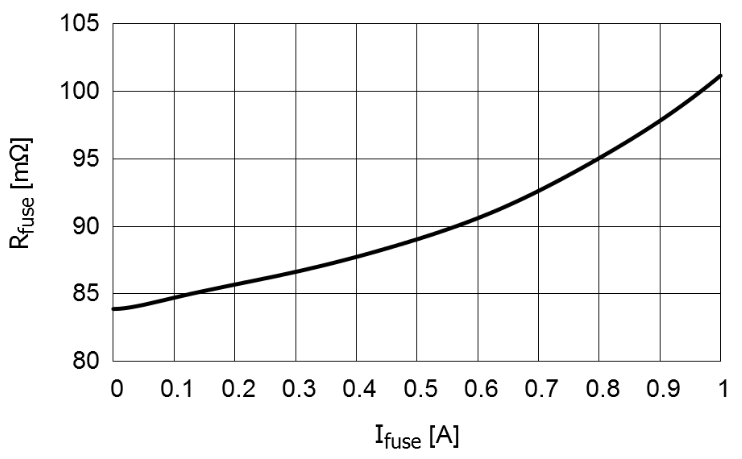


**Figure 7** BGF153 Fuse resistance as function of DC rated current from A1 to A2 and vice versa (DC current forced for 10 seconds for each measurement point)

## 2.3 Fuse Lifetime and destruction of the BGF153

This subsection relates to the life and operational time of the BGF153. Just as mentioned in the previous section, electron migration and self-heating process are responsible in particularly for the lifetime reduction of the fuse. In the **Figure 8** the average lifetime versus the current float through the fuse is shown.

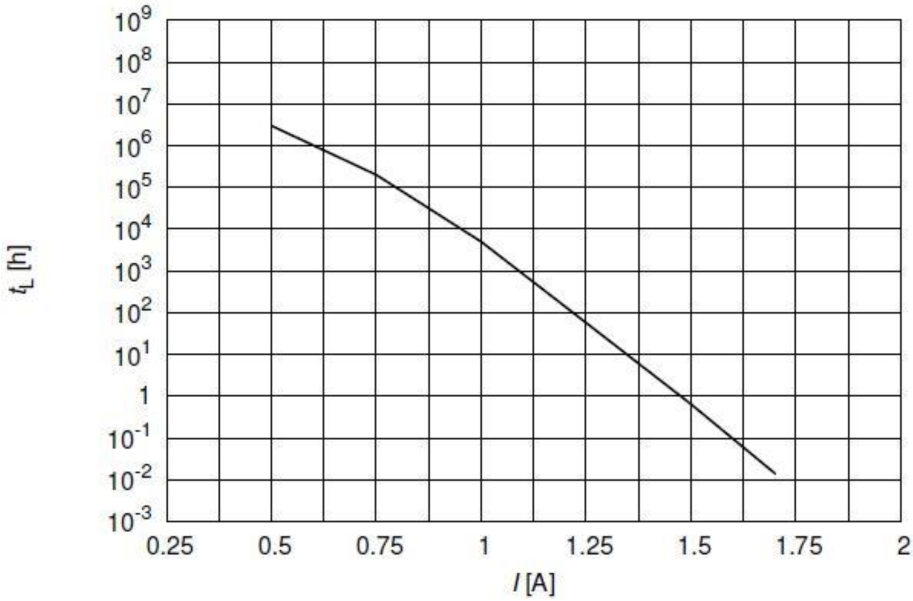


**Figure 8** Average lifetime versus current flow curve of the BGF153 Fuse

The **Figure 9** demonstrates the final destruction of the BGF153 Fuse after a current of the 2 A is driven from A1 to A2 pad. The post fusing resistance after fusing event rises to several Mega Ohms, preventing the ESD Current from spreading further into the circuit (building an open circuit).

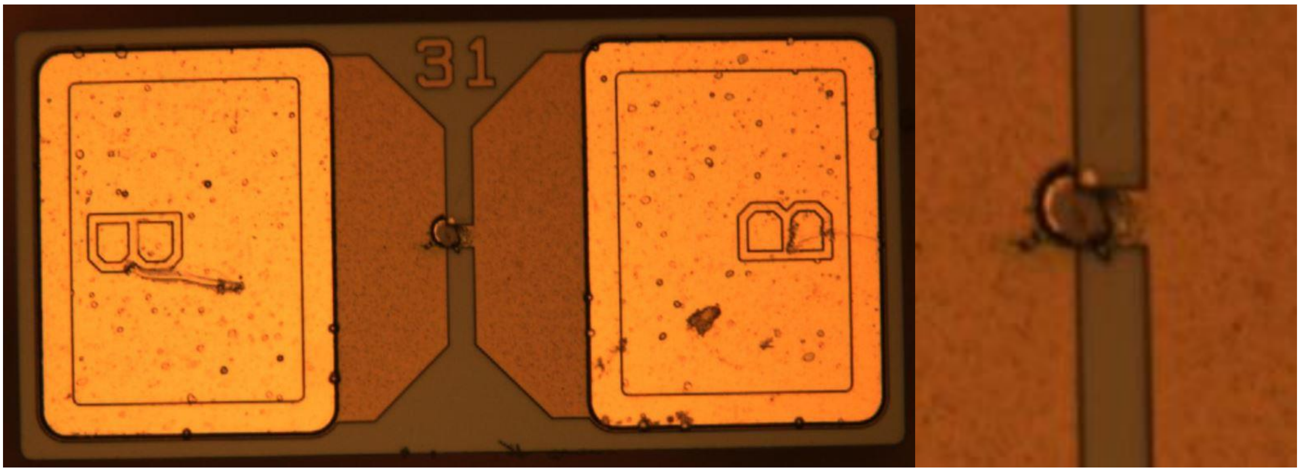


**Figure 9** Zoom of the BGF153 fuse element after an overcurrent event. Insulation post fusing resistance 20MOhm

# 3 Assembly Recommendations

## 3.1 PCB Layout for BGF153

PCB design and stack-up are key factors for achieving highly reliable solder joints. The interconnect solder joint-to-board are influenced by many factors such as Pad technology (Solder Mask Defined SMD and Non-Solder Mask Defined NSMD), Specific pad dimensions, Pad finish (also called metallization or final plating), Via Layout and Technology. Generally, NSMD pad design is recommended for Wafer Level packages. This is based on the fact that these packages and their connection pads are very small, and NSMD design eliminates the influence of PCB manufacturing tolerances of the solder mask layer. The solder paste is applied onto the PCB metal pads by stencil printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. Too much solder paste will cause solder bridging, whereas too little solder paste can lead to insufficient solder wetting between all contact surfaces. Further information can be found in the Recommendations for Board Assembly for Infineon WLL Packages by following this link.

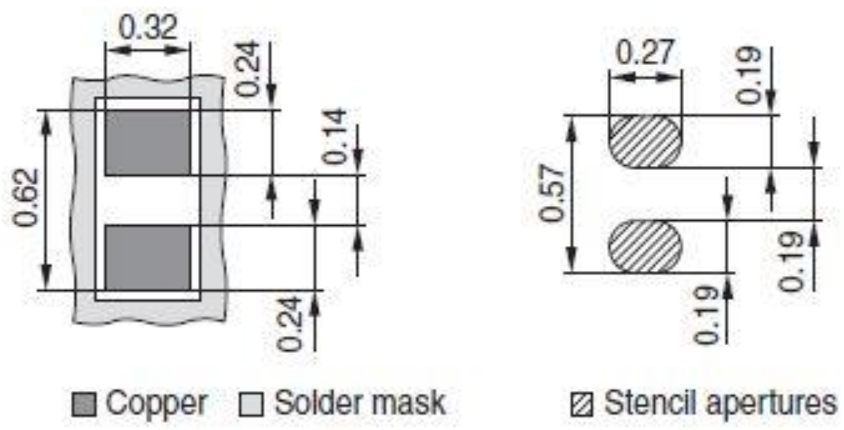


**Figure 10** WLL-2-1: Footprint (Dimension in mm)

## 3.2 Soldering Profile and Soldering Recommendation

BGF153 are Wafer-Level-Packages and can be only mounted by reflow soldering.

It is of a high importance to use only the necessary amount of the solder flux on the PCB pads. The over portion of the solder flux under the BGF153 can cause malfunctions during fusing event. The solder flux when used in plenty may build thick layer under the fusing contact preventing total destruction of the fuse contact during fusing event. Normally the Silicon-Nitride passivation and Aluminum-Cupper are immediately blown away from the Silicon oxide by a self-heating process if the current exceeds 1.75 A for BGF153. If there is an excess of the solder flux than recommended, then the metal parts are injected into this excess of solder flux building some resistance between the remained fuse pads. Therefore the resistance between fuse pads after the fuse event rises only up to some Kilo Ohm and not up to desired 20 Mega Ohms.

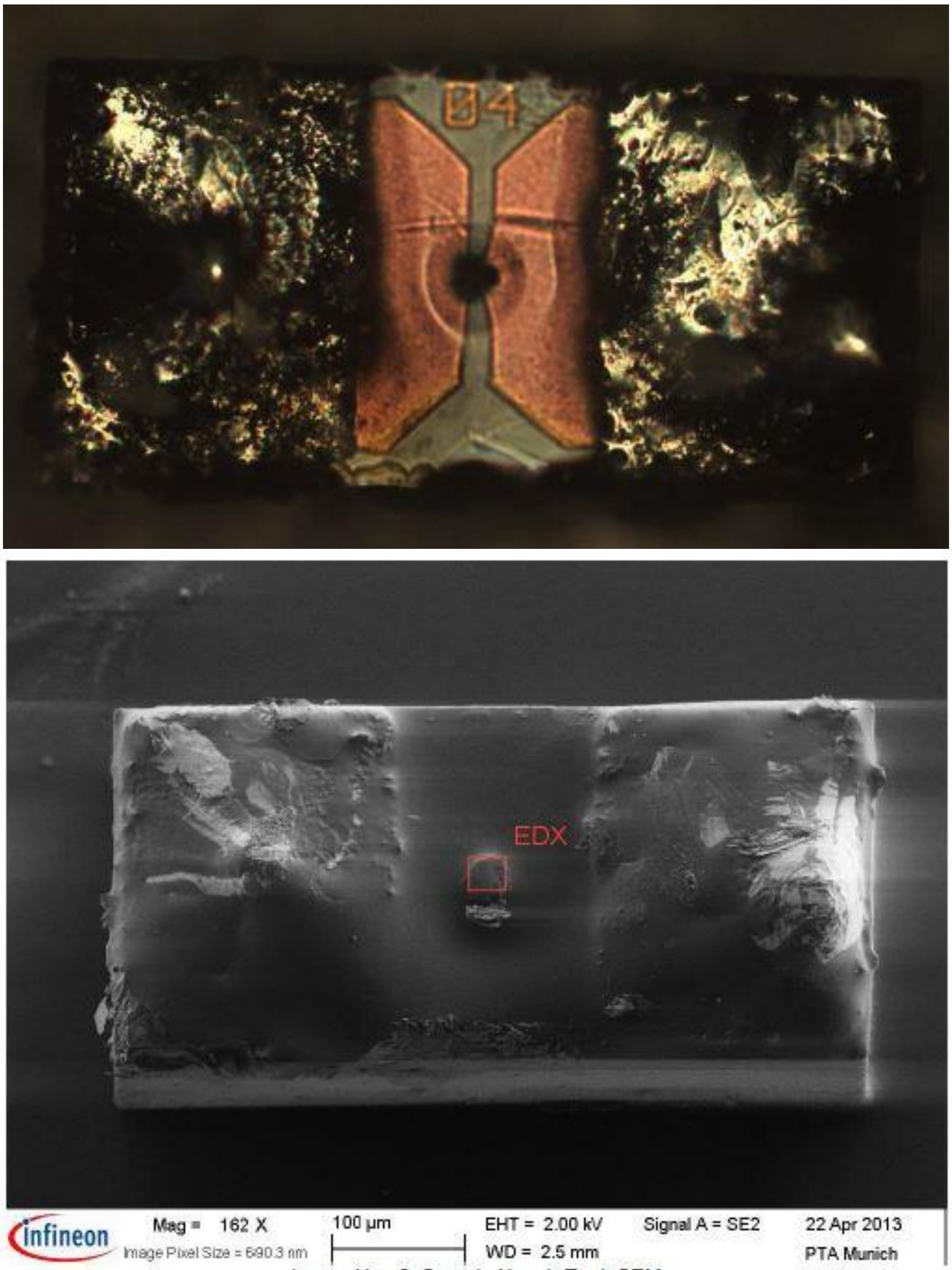


**Figure 11** Solder flux over portion caused malfunction after fusing.

## References

[1] Infineon Technologies AG, “Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology”, Application Note 210, RF and Protection Devices, April 22, 2010, Rev. 1.0

# Terminology

| | | |
|---|---|---|
| $C_L$ | ... | Line capacitance |
| $I_{PP}$ | ... | Peak pulse current |
| $I_R$ | ... | Reverse current |
| $I_{RWM}$ | ... | Reverse working current maximum |
| $R_{DYN}$ | ... | Dynamic resistance |
| $T_A$ | ... | Ambient temperature |
| $T_{OP}$ | ... | Operation temperature |
| $t_p$ | ... | Pulse duration |
| $t_r$ | ... | Pulse rise time |
| $T_{stg}$ | ... | Storage temperature |
| $V_{CL}$ | ... | Reverse clamping voltage |
| $V_{ESD}$ | ... | Electrostatic discharge voltage |
| $V_{FC}$ | ... | Forward Clamping Voltage |
| $V_{Hold}$ | ... | Holding Voltage |
| $V_{IEC}$ | ... | Equivalent stress level according IEC 61000-4-2 (R = 330 Ω, C = 150 pF) |
| $V_R$ | ... | Reverse voltage |
| $V_{RWM}$ | ... | Reverse working voltage maximum |
| $V_{Trig}$ | ... | Triggering Voltage |
| $Z_0$ | ... | Impedance |
| DVI | ... | Digital Visual Interface |
| EFT | ... | Electrical Fast Transient |
| ESD | ... | Electrostatic Discharge |
| HDMI | ... | High Definition Multimedia Interface |
| IEC | ... | International Electro technical Commission |
| MDDI | ... | Mobile Display Digital Interface |
| MIPI | ... | Mobile Industrial Processor Interface |
| PCB | ... | Printed Circuit Board |
| RoHS | ... | Restriction of Hazardous Substances Directive |
| S-ATA | ... | Serial Advanced Technology Attachment |
| TLP | ... | Transmission Line Pulse |
| USB | ... | Universal Serial Bus |
| SiNi | ... | Silicon nitride |

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