# USB PD Type-C multiport charger and adapter reference board with EZ-PD™ CCG7xC controller

## About this document

### Scope and purpose

This document provides an overview of USB PD Type-C multiport charger and adapter design with EZ-PD™ CCG7xC USB Type-C Power Delivery (PD) and buck-boost controller in multiport charger and adapter applications. Here, EZ-PD™ CCG7xC represents EZ-PD™ CCG7DC and EZ-PD™ CCG7SC controllers, which are used for dual and single-port applications respectively.

### Intended audience

This document is intended for anyone who uses the charger and adapter applications hardware designers using the EZ-PD™ CCG7xC USB Type-C PD and buck-boost controller.

*Note:* *This is a preliminary application note; the contents in this document are subject to change.*

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# 1 Introduction

USB-PD Type-C multiport charger and adapter design with EZ-PD™ CCG7xC controller application note provide an overview of EZ-PD™ CCG7xC's highly integrated single/dual-port USB Type-C PD solution with integrated buck-boost controllers and solution design using the EZ-PD™ CCG7xC in charger and adapter applications. This solution is based on a peak current-controlled two-switch buck converter for charger and adapter USB Type-C PD applications.

EZ-PD™ CCG7xC is a highly integrated dual-port USB Type-C PD solution with integrated buck-boost controllers. It complies with the latest USB Type-C and USB PD specifications, and targets charger and adapter applications. Integration offered by EZ-PD™ CCG7xC reduces the bill of materials (BOM) and provides a footprint-optimized solution for charger and adapter needs.

EZ-PD™ CCG7xC has integrated gate drivers for $V_{BUS}$ NFET on the provider path or for the buck bypass switch control. It also includes hardware-controlled protection features on the $V_{BUS}$. EZ-PD™ CCG7xC supports a wide input voltage range from 4 to 24 V with a 40-V tolerance and a programmable switching frequency between 150 to 600 kHz in an integrated PD solution. EZ-PD™ CCG7xC integrates monitoring, protection, and communication features to build a robust charger and adapter USB-C charging system.

EZ-PD™ CCG7xC is the most programmable USB PD solution with an on-chip 32-bit Arm® Cortex®-M0 processor, 128 kB flash, 16 kB RAM, and 32 kB ROM that leaves most flash available for the application use. It also includes various analog and digital peripherals, such as analog-to-digital converters (ADCs), pulse-width modulators (PWMs), $I^2C$/SPI/UART interfaces, and timers. The inclusion of a fully programmable MCU with analog and digital peripherals allows the implementation of custom system management functions such as power throttling, load sharing, temperature monitoring, and fault logging or event data recording.

The Power Delivery (PD) technology design provides the fastest charging possible through a USB Type-C (USB-C) cable. The USB PD Standard Power Range (SPR) standard defines the maximum power to deliver over a USB-C cable up to 100 W. This allows for providing multiple USB-C ports (Figure 1) on universal AC-DC adapters that can charge a wide range of devices such as smartphones, gaming laptops, power tools, and e-bikes.

However, these new requirements for high power and multiport have challenges for the converter topologies used till now. Considering a few factors such as electromagnetic compatibility, power factor correction, standby power, and average efficiency ensures that the chargers and adapters are effective and efficient. The size (power density), load sharing, and scaling up multiple ports became critical factors for design engineers and end-users. The power efficiency of USB-C chargers and adapters plays a crucial role in determining their power density. Therefore, converter topology, usage model, integration, and flexibility of controller functionalities are all key factors to consider when selecting the right adapter architecture for your needs.

Figure 1 shows the typical block diagram of a multiport adapter. The front-end AC-DC converter produces the requested output voltage while ensuring power factor correction (PFC) at the front end for up to 120 W of power. On the other hand, the buck converter (connected at the output of the AC-DC converter) ensures that the defined USB-C PD specifications and performance are met for multiport adapter applications.

## Introduction

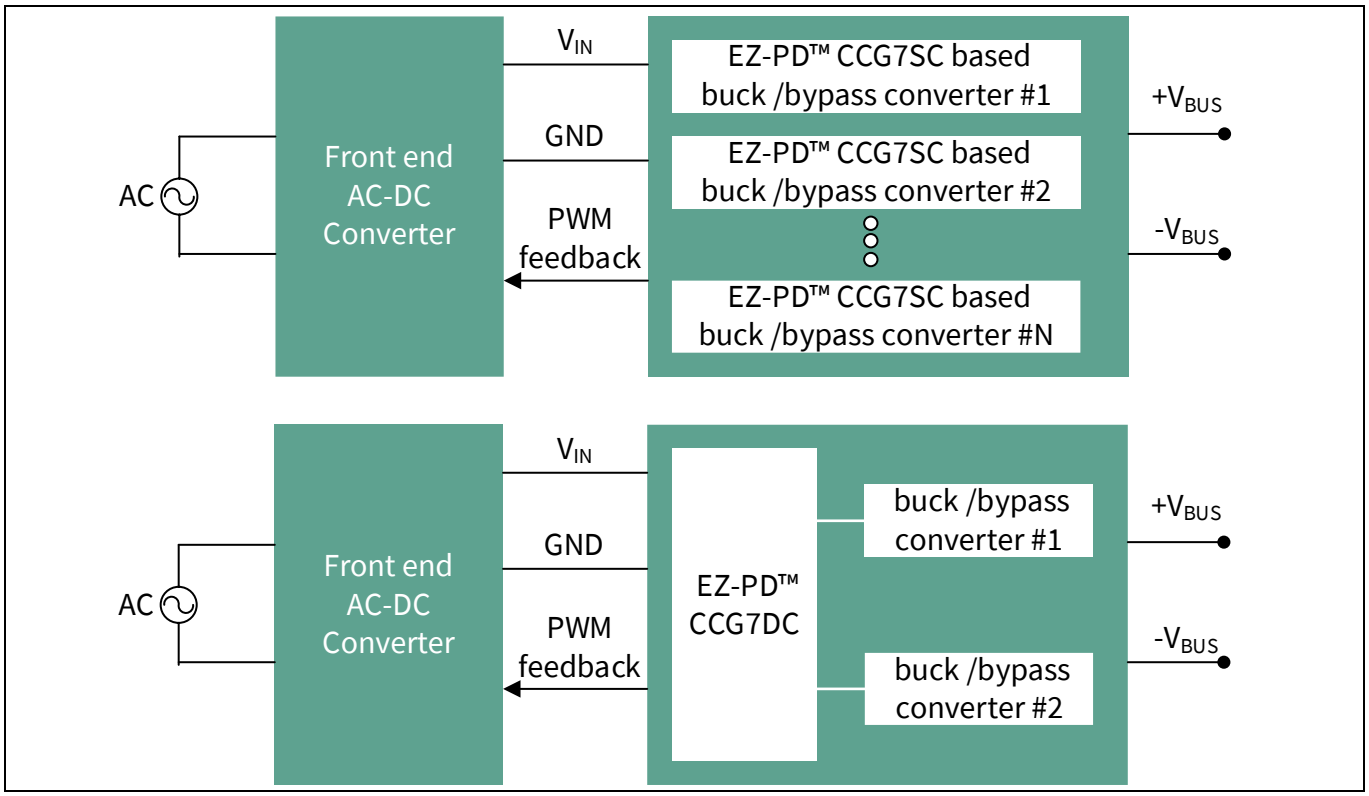


**Figure 1 High-level block diagram of a multiport adapter**

The design of an EZ-PD™ CCG7SC supports a single USB PD/Programmable Power Supply (PPS) port, featuring an integrated buck controller and gate driver, allowing easy scaling to multiport output. Additionally, the EZ-PD™ CCG7DC supports a dual PD/PPS port, capable of controlling two buck controllers with integrated drivers, which makes it an ideal choice for dual-port or multiport (multiples of 2) applications and a typical architecture of a 100 W dual-port charger as shown in Figure 2 and Figure 3.

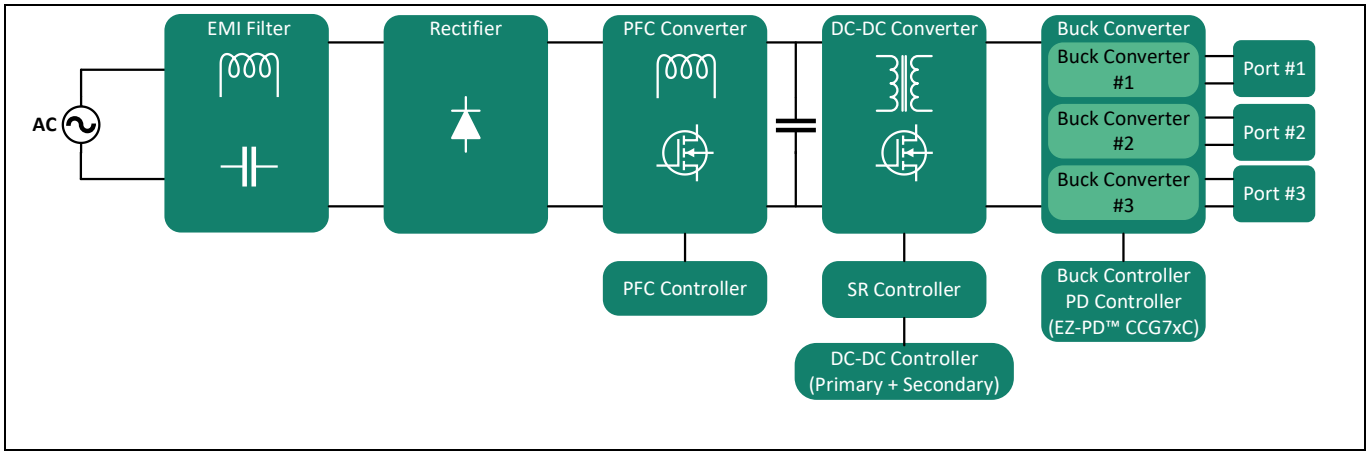


**Figure 2 Typical architecture of a three-stage three-port charger**

## Introduction

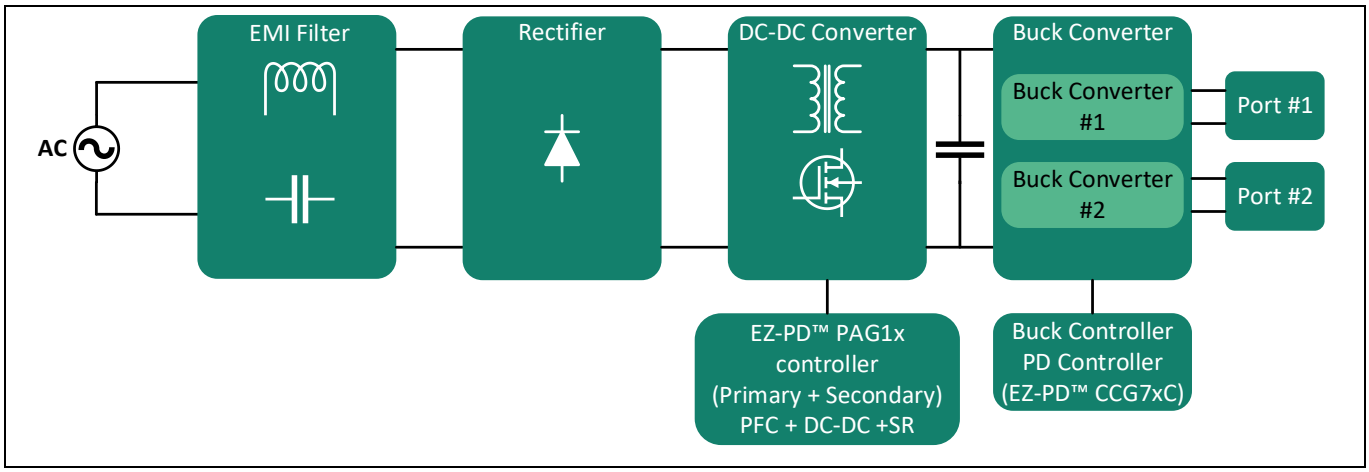


**Figure 3 Typical architecture of a two-stage dual-port charger**

*Note: This application notes discusses about the design of CCG7xC basedDC-DC converter, for frontend AC-DC converter design refer [7].*

# 2 EZ-PD™ CCG7xC features and applications

## 2.1 Applications

- EZ-PD™ CCG7DC used in dual-port consumer charging applications
- EZ-PD™ CCG7SC used in single-port consumer charging applications
- Power source charger
- Cigarette lighter adapter (CLA)

## 2.2 Features

### 2.2.1 USB PD

- EZ-PD™ CCG7DC supports two USB PD ports
- EZ-PD™ CCG7SC supports a single USB PD port
- Supports the latest USB PD 3.0 version 2.0 includes programmable power supply (PPS) mode

### 2.2.2 Type-C

- Configurable Type-C pull-up termination resistors ($R_P$)
- $V_{BUS}$ NFET gate driver
- Integrated 100 mW $V_{CONN}$ power supply, control, and protection

### 2.2.3 Buck-boost controllers

- EZ-PD™ CCG7DC supports two buck-boost controllers
- EZ-PD™ CCG7SC supports a single buck-boost controller
- Ranges between 150 to 600 kHz switching frequency
- 5.5 to 24 V input, 40-V tolerance
- 3.3 to 21.5 V output
- 20 mV voltage and 50 mA current steps for PPS
- Supports pulse-skipping mode (PSM) for light-load efficiency
- Supports forced continuous current/conduction mode (FCCM) for minimum ripple
- Soft start to reduce inrush current
- Programmable spread-spectrum frequency modulation for low EMI
- Switching synchronization with programmable phase shift across two ports to further reduce the EMI

### 2.2.4 Legacy/proprietary charging blocks

- Supports USB Battery Charging (BC) 1.2, QC 2.0/3.0, Apple Charging 2.4 A/3.0 A, and Samsung Adaptive Fast Charging (AFC)

### 2.2.5 Integrated voltage ($V_{BUS}$) regulation and current sense amplifier

- Supports current sensing (CS) for PPS current foldback operation
- Internal feedback network
- Supports external type 2 compensation network

### 2.2.6 System-level fault protection

- On-chip $V_{BUS\_C}$, overvoltage protection (OVP), overcurrent protection (OCP), undervoltage protection (UVP)
- $V_{BUS\_C}$-to-CC short protection
- Undervoltage lockout (UVLO)
- $V_{CONN}$ OCP
- Supports overtemperature protection (OTP) through external and/or internal temperature sensor
- Supports connector and board temperature measurement using external thermistors

### 2.2.7 32-bit MCU subsystem

- 48-MHz Arm® Cortex®-M0 CPU
- 128 kB flash
- 16 kB SRAM
- 32 kB ROM

### 2.2.8 Peripherals and GPIOs in EZ-PD™ CCG7DC

- 19 GPIOs
- Two overvoltage tolerant (OVT) GPIOs
- 3x 8-bit ADCs
- 4x 16-bit timers/counters/PWMs (TCPWMs)

### 2.2.9 Peripherals and GPIOs in EZ-PD™ CCG7SC

- Up to 13 GPIOs including two OV GPIOs
- 2x 8-bit ADCs
- 8x 16-bit timers/counters/PWMs (TCPWMs)
- 1x 12-bit ADC

### 2.2.10 Communication interfaces in EZ-PD™ CCG7DC

- 4x SCBs ($I^2C$/SPI/UART/LIN)

### 2.2.11 Communication interfaces in EZ-PD™ CCG7SC

- 3x Serial Communication Blocks (SCBs) such as $I^2C$, SPI, UART, and LIN interfaces

### 2.2.12 Clocks and oscillators

- Integrated oscillator, eliminating the need for an external clock

### 2.2.13 Power supply

- 4 to 24 V input (40-V tolerance)
- 3.3 to 21.0 V output
- Integrated LDO capable of 5 V at 150 mA in EZ-PD™ CCG7DC and 5 V at 75 mA in EZ-PD™ CCG7SC

### 2.2.14 Packages

- EZ-PD™ CCG7DC is available in 68-pin 8 mm x 8 mm QFN
- EZ-PD™ CCG7SC is available in 40-pin 6 mm x 6 mm QFN
- –40°C to +105°C extended industrial temperature range
- Max. 125°C operating junction temperature

## 2.3 EZ-PD™ CCG7DC block diagram

Figure 4 and Figure 5 show logic and functional block diagrams of the EZ-PD™ CCG7DC architecture respectively. For more details, see the EZ-PD™ CCG7DC datasheet (002-32352).

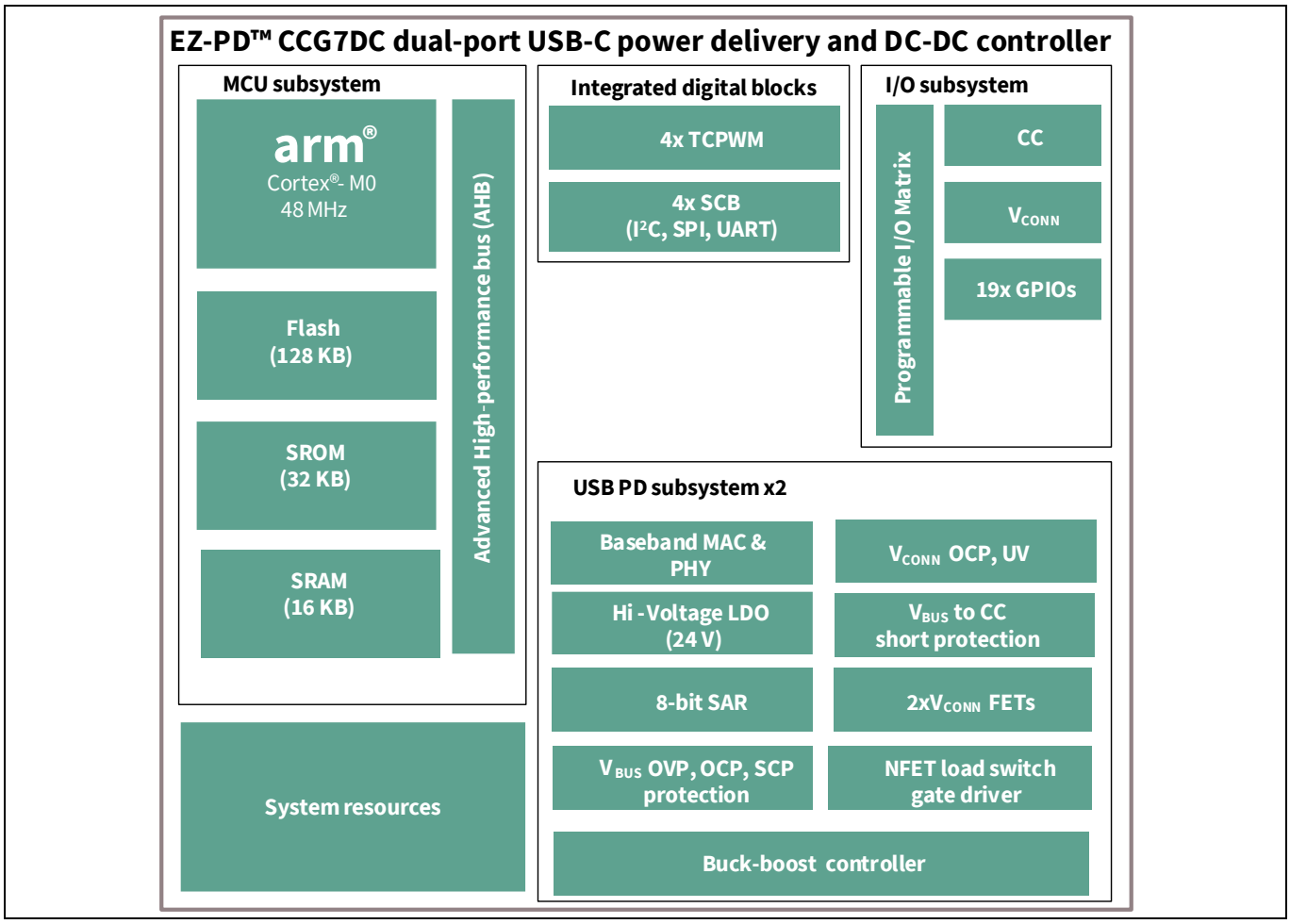


**Figure 4 Logic block diagram**

### EZ-PD™ CCG7xC features and applications

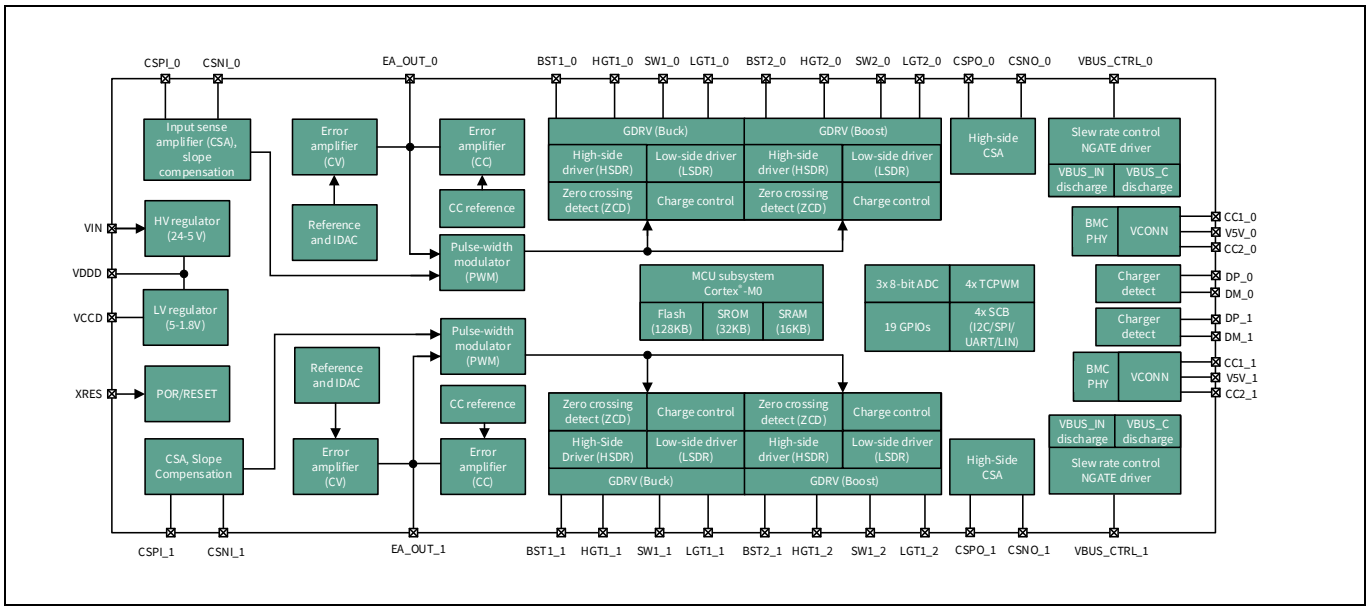


**Figure 5 Functional block diagram**

## 2.4 EZ-PD™ CCG7SC block diagram

Figure 6 and Figure 7 show logic and functional block diagrams of the EZ-PD™ CCG7SC architecture respectively. For more details, see the EZ-PD™ CCG7SC datasheet (002-35643).

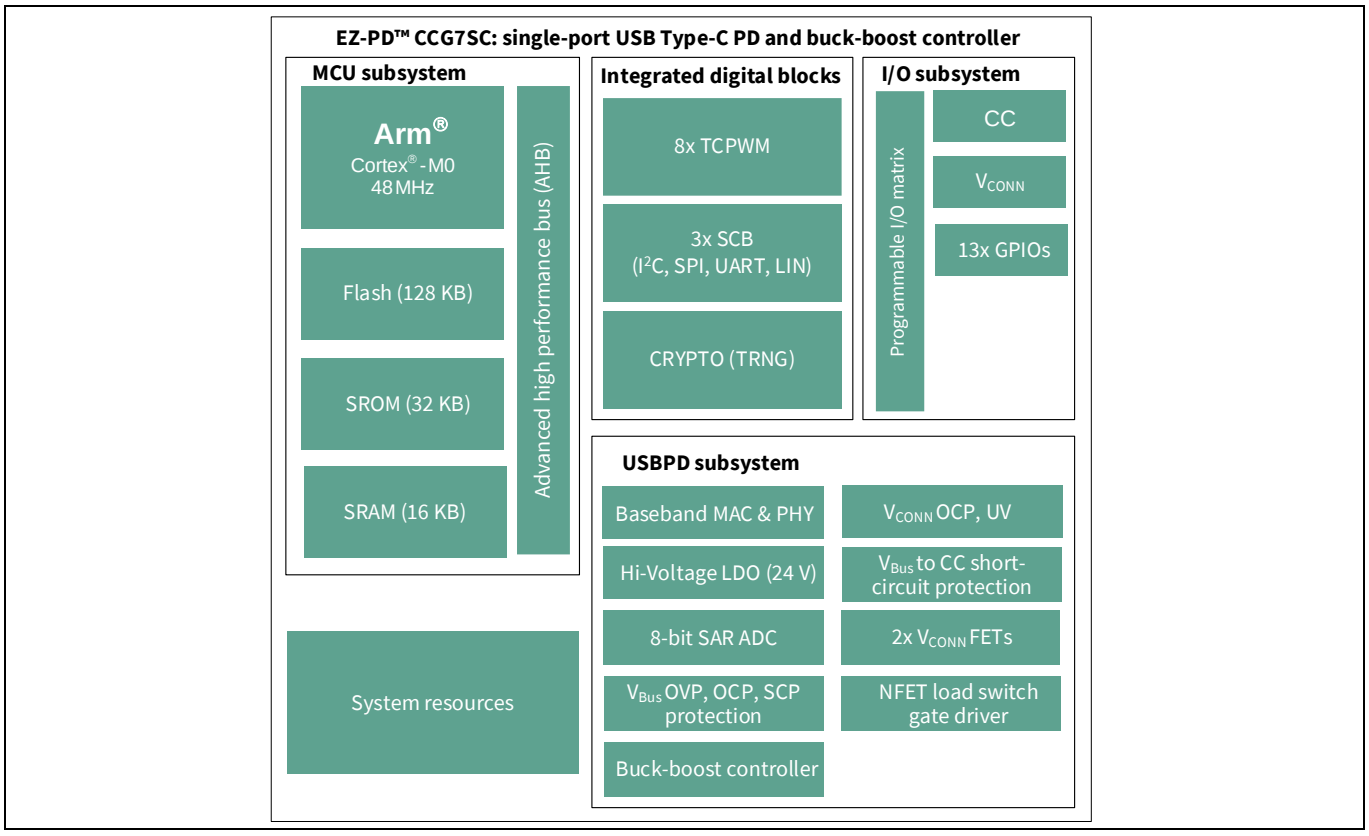


**Figure 6 Logic block diagram**

### EZ-PD™ CCG7xC features and applications

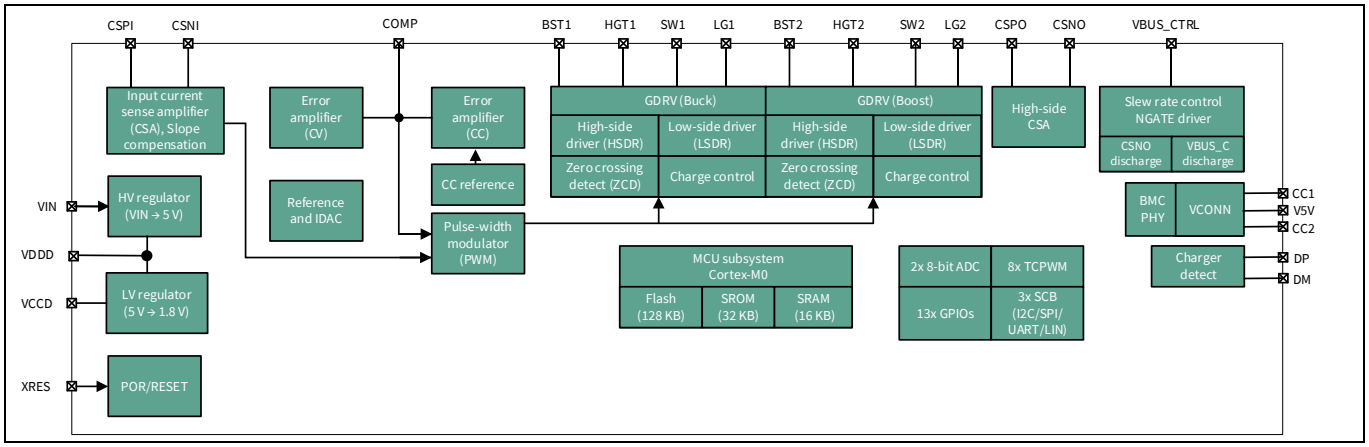


**Figure 7 Functional block diagram**

## 2.5 EZ-PD™ CCG7SC based step-down (buck) converter

Figure 8 shows a buck-only mode application block diagram using the EZ-PD™ CCG7SC. This application uses the integrated buck controller to supply the required voltage and current to the connected device. In a buck application, the negotiated voltage must always be lower than the input voltage.

The port will shut down if the input voltage drops lower than the output voltage because of the output voltage maintenance. This application can be configured to support the legacy charging protocols such as BC 1.2 dedicated charging port (DCP), Qualcomm QC 2.0/3.0, Apple charging, and Samsung AFC.

## EZ-PD™ CCG7xC features and applications

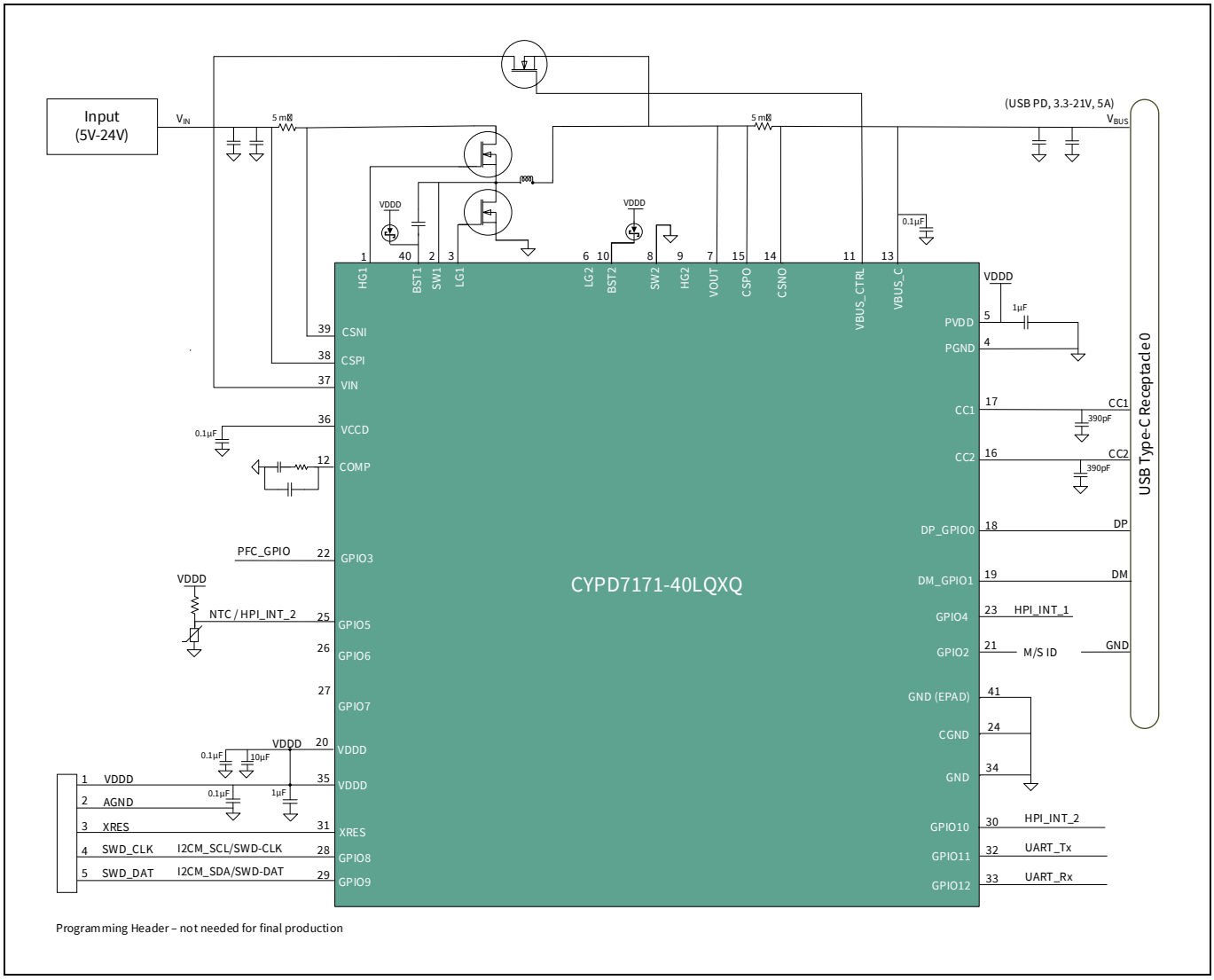


**Figure 8 EZ-PD™ CCG7SC-based step-down (buck) converter**

## 2.6 EZ-PD™ CCG7DC based dual output step-down (buck) converter

Figure 9 shows a dual output buck-only mode application block diagram using the EZ-PD™ CCG7DC. This application uses the integrated buck controller to supply the required voltage and current to the connected device. In a buck application, the negotiated voltage must always be lower than the input voltage.

The port will shut down if the input voltage drops lower than the output voltage because of the output voltage maintenance. This application can also be configured to support the legacy charging protocols – BC 1.2 DCP, Qualcomm QC 2.0/3.0, Apple charging, and Samsung AFC.

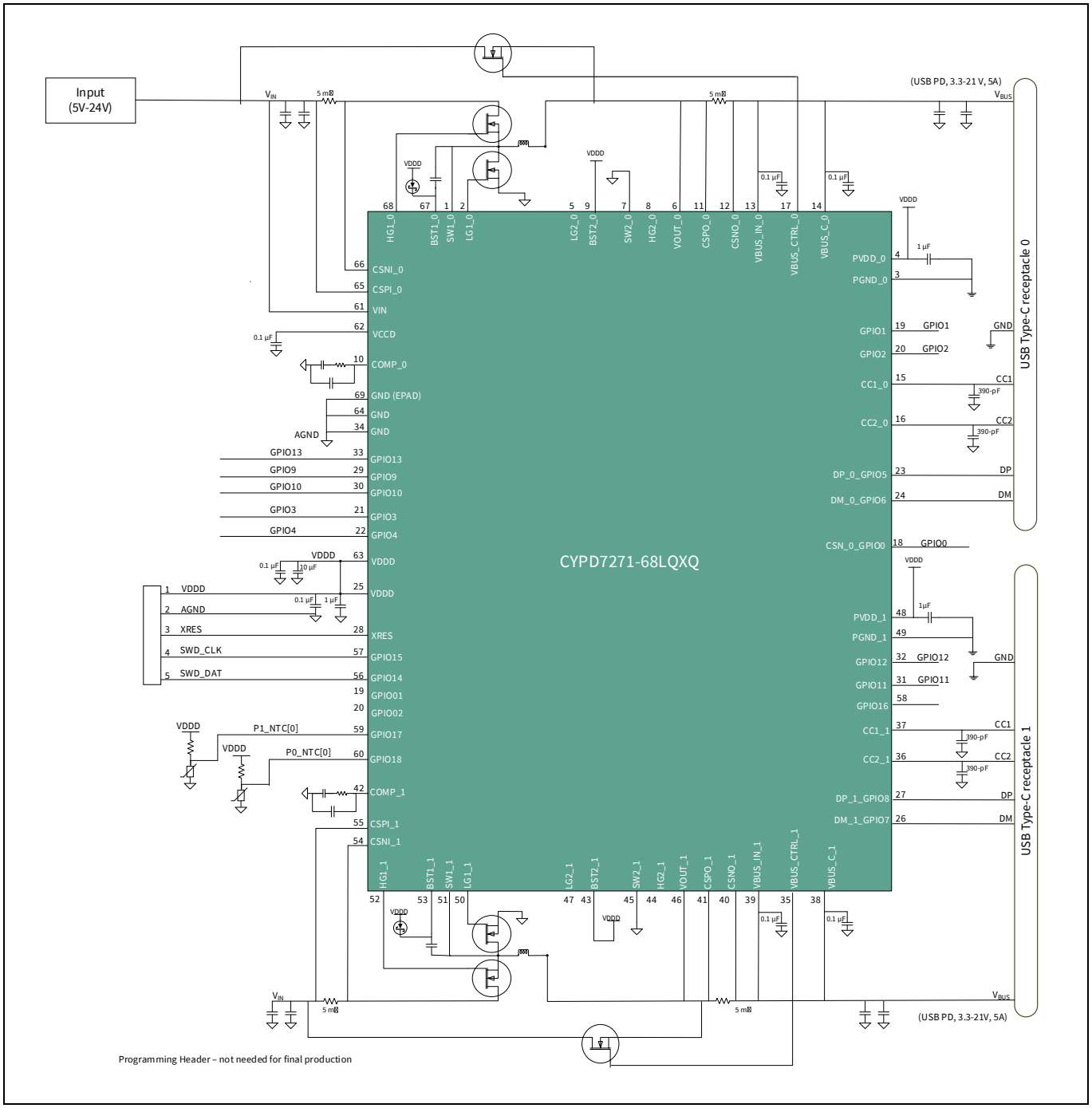


**Figure 9 EZ-PD™ CCG7DC based step-down (buck) converter**

## 2.7 EZ-PD™ CCG7SC in multiport AC-DC adapter application

Figure 10 illustrates a multiport USB PD Type-C AC/DC power adapter application block diagram using the EZ-PD™ CCG7SC. In this application, EZ-PD™ CCG7SC will always be in the downstream facing port (DFP) role supporting the device charging. It negotiates the power with the connected device and uses the integrated buck controller to supply the required voltage and current. The efficiency can be optimized by dynamically controlling the optocoupler feedback and thereby regulating the buck input voltage to the closest output voltage. This application can be configured to support the legacy charging protocols such as BC 1.2 DCP, Qualcomm QC 2.0/3.0, Apple Charging, and Samsung AFC.

Constant-frequency peak current-mode control (PCMC) is a popular control technique for switched-mode power converters. PCMC offers built-in OCP, robust dynamic responses, simplified voltage-loop compensator design, and rejection of input voltage disturbances.

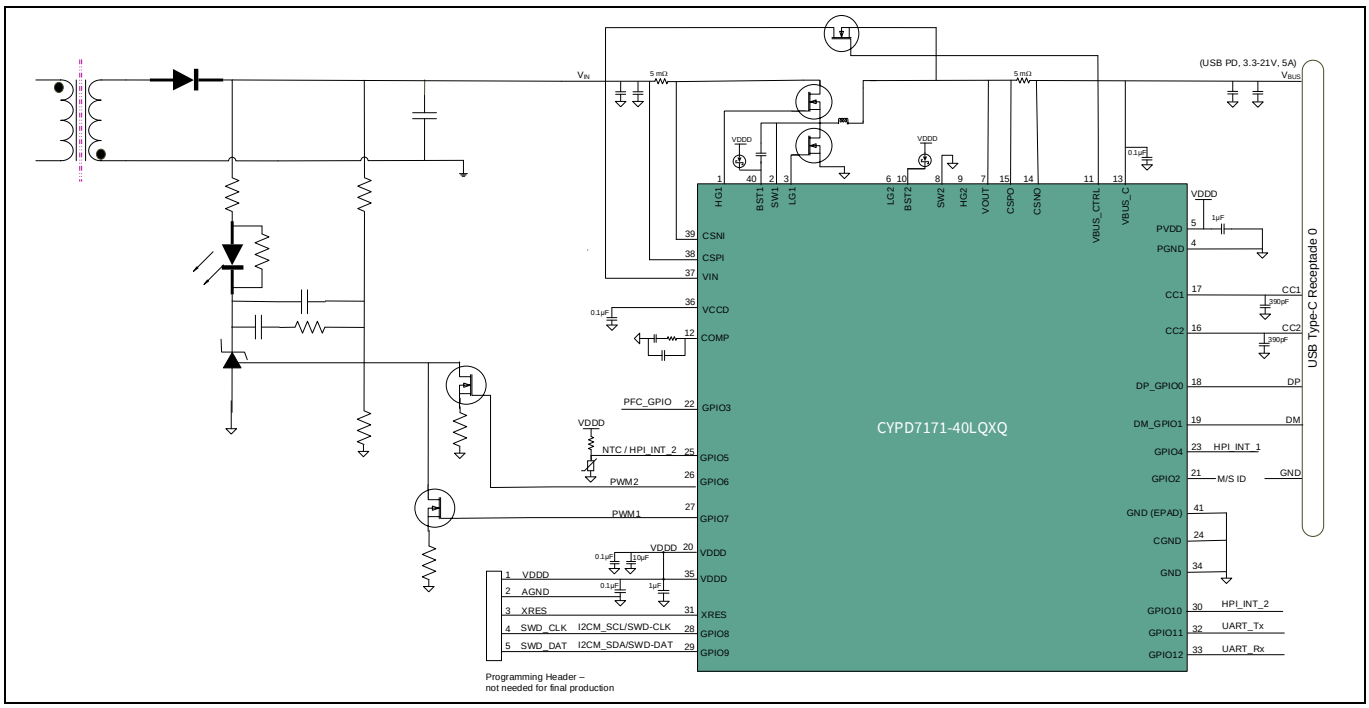


**Figure 10 EZ-PD™ CCG7SC multiport AC-DC adapter application diagram**

## 2.8 EZ-PD™ CCG7DC in multiport AC-DC adapter application

Figure 11 illustrates a two Type-C port AC/DC power adapter application block diagram using the EZ-PD™ CCG7DC. In this application, EZ-PD™ CCG7DC will always be in the DFP role supporting the device charging. It negotiates the power with the connected device and uses the integrated buck controller to supply the required voltage and current. The efficiency can be optimized by dynamically controlling the optocoupler feedback and thereby regulating the buck input voltage to the closest output voltage. This application can be configured to support the legacy charging protocols such as BC 1.2 DCP, Qualcomm QC 2.0/3.0, Apple Charging, and Samsung AFC.

Constant-frequency peak current-mode control (PCMC) is a popular control technique for switched-mode power converters. PCMC offers built-in OCP, robust dynamic responses, simplified voltage-loop compensator design, and rejection of input voltage disturbances.

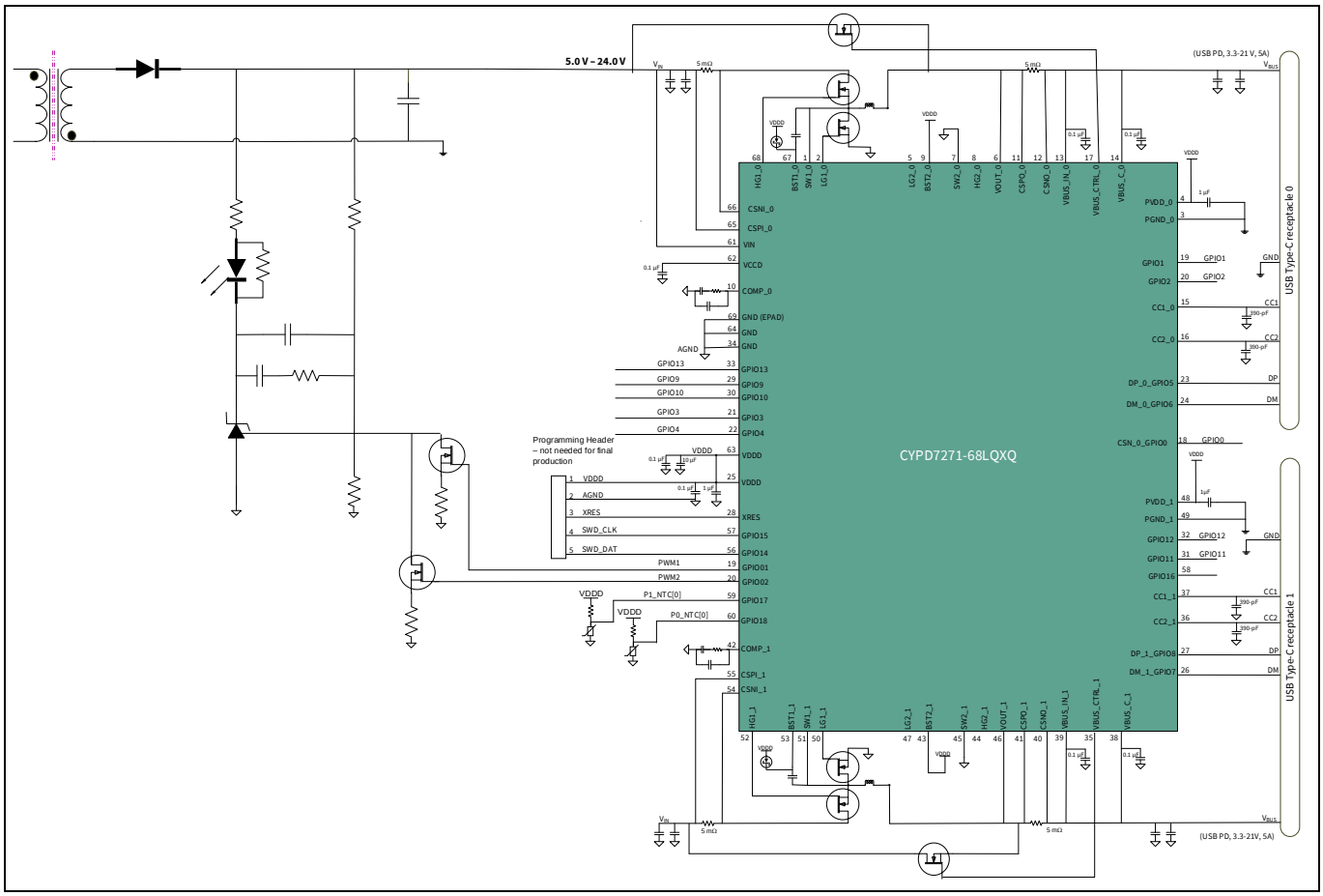


**Figure 11 EZ-PD™ CCG7DC multiport AC-DC adapter application diagram**

# 3 Multiport charger and adapter solution reference design requirements and features

In this document, the multiport charger and adapter solution reference design is taken as a use case to elaborate the design guidelines for EZ-PD™ CCG7xC in consumer applications.

## 3.1 System description

The EZ-PD™ CCG7DC multiport charger and adapter solution “REF_CCG7DC_120W_2C” and EZ-PD™ CCG7SC multiport charger and adapter solution “REF_CCG7SC_120W_3C” design solutions exhibit the features of the EZ-PD™ CCG7xC USB Type-C controller with PD and buck-boost controller. It is designed to operate from 5.0 V to 22.5 V DC input and output between 3.3 V and 21 V at 5 A and a maximum of 100 W USB PD power at each of its two source-only ports when EZ-PD™ CCG7DC is used and a single source-only port when EZ-PD™ CCG7SC is chosen. Load sharing can be configured between two ports when EZ-PD™ CCG7DC is chosen and between two or more boards when EZ-PD™ CCG7SC is chosen.

## 3.2 Detailed feature list

- Highly integrated dual-port USB Type-C PD controller-based solution
- Two independent Type-C USB-PD charging ports controlled by an EZ-PD™ CCG7DC controller and a single Type-C USB PD charging port controlled by a CCG7SC controller
- Nominal switching frequency 400 kHz
- USB PD source PDOs
  - Fixed PDOs: 5 V/5 A, 9 V/5 A, 15 V/5 A, 20 V/5 A
  - PPS: 3.3 to 11 V, 5 A; 3.3 to 16 V, 5 A; 3.3 to 21 V, 5 A, with a power limit
- Power output protections
  - Overvoltage protection
  - Undervoltage protection
  - Overcurrent protection
  - Short-circuit protection
  - Overtemperature protection
- Other power protections
  - $V_{BUS}$-to-CC short protection
- Legacy charging support
  - USB BC 1.2
  - 2.4 A Apple Charging
  - Qualcomm QC 2.0, 3.0, 4.0
  - Samsung AFC

## 3.3 Operating conditions and characteristics

**Table 1 Operating conditions and characteristics**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage [1] | $V_{IN}$ | Full performance – meets all specs | 5.0 | – | 22.5 | V |
| Output voltage range [1] | $V_{OUT}$ | Rated load ($I_{OUT}$) | 3.3 | – | 21.0 | V |
| Output current range | $I_{OUT}$ | Across all output voltages | 0 | – | 5 | A |
| Switching frequency | $F_{SW}$ | Full load (with 10 percent spread spectrum) | 360 | 400 | 440 | kHz |
| Steady-state output voltage | $V_{OUT}$ | Applies to DC accuracy, line regulation, load regulation, and output ripple | 0.95 × $V_{OUT}$ | – | 1.05 × $V_{OUT}$ | V |
| Output voltage during transient loads | $V_{OUT}$ | Applies to DC accuracy, line regulation, load regulation, and output ripple,<br>Load current step 25 percent of maximum output current ($I_{OUT}$) | 0.95 × $V_{OUT}$ - 0.1 | – | 1.05 × $V_{OUT}$ + 0.1 | V |
| Inrush current | $I_{Inrush}$ | $V_{IN}$: 0 to 12 V<br>$V_{IN}$ rise time: 10 ms | – | – | 20 | A |
| Port power output | $P_{OUT}$ | – | – | – | 100 | W |
| System power output (Note 1) | – | Total power which can be drawn from the connected ports | – | – | 120 | W |
| Output OVP | – | – | – | 1.20 × $V_{OUT}$ | – | V |

[1] The minimum input voltage operation and power rating depends on the front-end AC-DC converter PD specifications.

# 4 Hardware design for the buck converter

In the given range of input voltage, the choice of converter topology needs to provide a stable output voltage. From the application specifications, the input voltage can be higher than the required output voltage. The buck converter topology as shown in Figure 12 provides step-down voltages seamlessly to the output and the buck bypass switch operation discussed in Section 4.8. The multiport charger and adapter solution board hardware components chosen to meet the Type-C USB PD standards.

## 4.1 Key specifications

- Input voltage range ($V_{IN}$): +5.5 to +22.5 V DC
- Output voltage range ($V_{OUT}$): +3.3 to +21 V DC
- Output current range ($I_{OUT}$): +0.0 to +5.0 A DC
- Topology: Synchronous buck converter
- Control method: Peak Current Mode Control (PCMC)
- Compensator: Type 2 compensator
- Support for USB PD PPS current limit operation

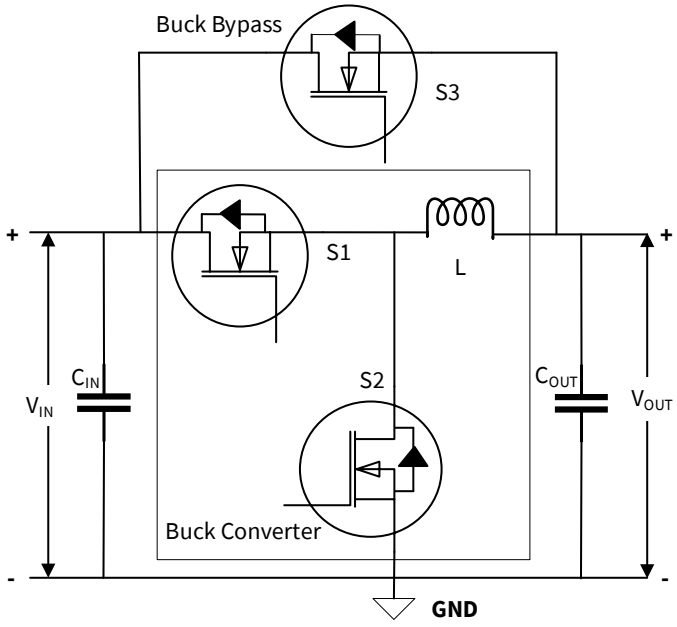


**Figure 12 Simplified buck converter with bypass switch**

## 4.2 Input capacitor selection

The function of input multilayer ceramic capacitors (MLCCs) is to reduce the ripple voltage amplitude on the input line and the root mean square (RMS) ripple current handled by the input bulk capacitors. Additionally, these reduce the switching noise on the input lines, thereby reducing the conducted electromagnetic interference (EMI). The input capacitor's bank comprises a combination of ceramic and electrolytic capacitors. Ceramic capacitors use to bring down the effective series resistance (ESR) of the capacitor bank, as ceramics offers extremely low equivalent series resistance and limit the input voltage switching ripple. Bulk electrolytic capacitors use to support the change in line current during load transient.

When the converter operates in buck mode, the series switch (S1) in Figure 12 causes a pulsating ripple current with high di/dt at the input. In the absence of input filter capacitors, the DC resistance of PCBs and parasitic inductance generates a large voltage ripple at the input. Input filter capacitors provide a short and low-impedance path for ripple current, which reduces conducted and radiated EMI, and provides stability to the line voltage during input voltage fluctuations. Note that the pulsating input current waves have high RMS values which cause significant heating and high harmonic content, resulting in EMI.

In an application, it recommends keeping the input voltage ripple lower than ±5 to ± 10 percent of the input voltage. The input voltage peak-to-peak ripple produced by the input capacitor is equal to the input capacitor's ESR multiplied by the capacitor's RMS current.

The chosen input capacitor's current ratings should be equal to or greater than the RMS capacitor current $I_{Cin\_rms}$ and its voltage rating is 40 to 50 percent higher than the maximum applied input voltage.

### 4.2.1 Input capacitor RMS current – buck mode

The RMS current of the input capacitor in buck mode is:

$$I_{C\,IN\_rms} = \sqrt{\frac{1}{T}\int_0^T i_{C_{IN}}^2\ dt}$$

The input capacitor current, when switch S1 is on is ($I_{IN} - I_L$) and when switch S1 is off is $I_{IN}$, then $I_{C\,IN\_rms}$ is as follows:

$$I_{C\,IN\_rms} = \sqrt{\frac{1}{T}\left(\int_0^{DT}(I_{IN} - I_L)^2\ dt + \right) + \int_{DT}^{T}(I_{IN})^2\ dt}$$

By neglecting the inductor ripple current ($\Delta I_L$) in a buck converter ($I_L = I_{OUT}$) and using the relation ($I_{IN} = D \times I_{OUT}$), the RMS current of the input capacitor in buck mode is:

$$I_{C\,IN\_rms} = I_{OUT}\sqrt{D(1-D)}$$

Where,

$I_L$ = Inductor current.

The duty cycle of a buck converter $D = \frac{V_{OUT}}{V_{IN} * \zeta}$

$\zeta$ = Efficiency of the power converter

### 4.2.2 Input ceramic capacitor selection – buck mode

The current flowing through the input capacitor ($I_{CIN}$) is the difference between the input current ($I_{IN}$) and inductor current ($I_L$) during the switch S1 on-state, and only the input current ($I_{IN}$) during the switch S1 off-state. From this operation, during the switch S1 off-state, the input capacitor ($C_{IN}$) gets charged with input current ($I_{IN}$), and during the switch S1 on-state, the input capacitor ($C_{IN}$) gets discharged. In steady-state, the input capacitor's charges added and removed are equal (i.e., capacitor amp-second balance). The input voltage ripple $\Delta V_{in\_pk-pk}$ goes from its minimum to maximum value during the S1 off-state; that is, the charging period.

It is known that:

$$I_{IN} = C\frac{dV_{in}}{dt} = \frac{C\Delta V_{in}}{t_{off}}; \qquad \text{in buck converter } I_{IN} = DI_{OUT} \text{ and } t_{off} = (1-D)T_{sw}$$

The input MLCC value to meet the input voltage ripple requirement in buck mode is:

$$C_{IN\_MLCC} \gg = \frac{D\,(1-D)\,I_{OUT\_MAX}}{\Delta V_{IN\ pk-pk} \times f_{sw}}$$

Where,

$\Delta V_{IN\ pk-pk}$ = Allowed maximum peak-to-peak input voltage ripple

$f_{sw}$ = Operating/switching frequency of the converter

$I_{OUT\_MAX}$ = Rated maximum output current

The loss because of the input capacitor's ESR is:

$$P_{C_{in}} = I^2_{C_{in\ rms}} \times R_{C_{in\_mlcc}}$$

Where,

$R_{Cin\_mlcc}$ = Input MLCC network's total ESR.

### 4.2.3 Input bulk capacitor selection – buck mode

The input supply lines are typically incapable of providing the required input current quickly enough for the converter to respond to a fast-transient load current. The input bulk capacitor provides the energy necessary to source current to the buck supply until the host supply can fill the demand. The choice of the input bulk capacitor must meet the allowable ripple current requirement and overshoot, and undershoot specifications because of load transients.

The ESR of the input bulk capacitor ($R_{CIN\_bulk}$) and the capacitance ($C_{IN\_bulk}$) need to meet the transient response requirement.

The ESR of the input bulk capacitor is:

$$R_{Cin\_bulk} \ll 0.5\left(\frac{V_{IN\_transient}}{I_{OUT_{step}} \times D_{BUCK_{MAX}}}\right)$$

Where,

$V_{IN\_transient}$ = Allowed input voltage transient undershoot or overshoot due to output load current transients

$I_{OUT\_step}$ = Allowed change in output load current

**Hardware design for the buck converter**

$D_{BUCK\_MAX}$ = Maximum duty cycle in buck mode

The capacitance of the input bulk capacitor to meet the output load transients is:

$$C_{IN\_bulk} \gg \frac{D_{BUCK} \times I_{OUT\_step}}{2 \times \pi \times f_{bw\_emi\_filter} \times V_{IN\_transient}}$$

Where,

$f_{bw\_emi\_filter}$ = Bandwidth of the input EMI LC filter

$D_{BUCK}$ = Duty cycle in buck mode

Input voltage transient undershoot/overshoot because the load step is:

$$V_{IN\_transient} = \frac{I_{OUT\_step} \times D_{BUCK}}{2 \times \pi \times f_{bw\_emi\_filter} \times (C_{IN\_bulk} + C_{IN\_mlcc})} + I_{OUT\_step} \times D_{BUCK} \times (R_{C\ IN\_bulk})$$

Input voltage ripple is:

$$V_{IN\_ripple} = \frac{I_{OUT} \times D_{BUCK} \times (1 - D_{BUCK})}{f_{sw} \times (C_{in\_bulk} + C_{in\_mlcc})} + I_{OUT\_max} \times D_{BUCK} \times (R_{C_{in\_mlcc}})$$

## 4.3 Power inductor selection

The chosen power inductor value must satisfy buck converter input and output specifications. The lower the inductor value, the smaller the size, therefore, resulting in a high peak current.

### 4.3.1 Power inductor value – buck mode

The basic inductor current and voltage relation are $V_L = L\frac{dI_L}{dt}$. In a buck converter, the change in inductor current during the switch S1 on-time is equal to the change in current during the switch S1 off-time. The change in the inductor current ($I_L$) during the switch S1 on time is $\frac{\Delta I_L}{DT_{sw}}$.

$$L_{buck} = \frac{(V_{IN\_max} - V_{OUT}) \times D_{Buck}}{\Delta I_L \times f_{sw}}$$

$\Delta I_L$ can be fraction (0.2 to 0.4) of the Iout_max

Where,

$V_{IN\_max}$ = Maximum input voltage

### 4.3.2 Inductor peak current – buck mode

The maximum current passing through the power inductor in buck mode is:

$$I_{L\_max\_buck} = \frac{\Delta I_L}{2} + I_{OUT\_max}$$

Switches S1 and S2 must withstand this peak current.

**Hardware design for the buck converter**

### 4.3.3 Inductor RMS current – buck mode

The RMS current passing through the power inductor in buck mode is:

$$I_{L\_rms\_buck} = \sqrt{(I_{OUT\_max})^2 + \frac{(\Delta I_L)^2}{12}}$$

## 4.4 Power switches selection

The voltage rating of the selected power switches must be 1.5 to 2 times the maximum applied input voltage to the converter and the continuous drain current rating to be greater than the computed switch peak current in a converter. The power losses of a converter depend on the chosen MOSFET characteristics such as drain-source on-state resistance ($R_{ds\_ON}$), rise time ($t_r$), fall time ($t_f$), total gate charge ($Q_g$), MOSFET diode reverse recovery charge ($Q_{rr}$), and switching frequency ($f_{sw}$) of the converter. The efficiency of the converter depends on the chosen power MOSFETs, so a few basic empirical formulas are provided in the following sections.

### 4.4.1 Power MOSFET selection – buck mode

When the switch (S1) is turned on, the current passed through the switch $I_{S1}$ is the current drawn from the input line. The switch RMS current $I_{S1\_rms\_ON}$ is:

$$I_{S1\_rms\_ON} = \sqrt{\left(I_{OUT}^2 + \frac{\Delta I_L^2}{12}\right)(D_{BUCK})}$$

When the switch (S2) is turned on the current passed through the switch RMS current $I_{S2\_rms\_ON}$ is:

$$I_{S2\_rms\_ON} = \sqrt{\left(I_{OUT}^2 + \frac{\Delta I_L^2}{12}\right)(1 - D_{BUCK})}$$

### 4.4.2 Power MOSFET losses – buck mode

In a synchronous buck converter, the power MOSFET losses can be conduction, switching, body diode reverse recovery, dead time, and gate charge losses. The empirical formulas for each of the losses are provided for S1 and S2 separately.

Conduction losses in switch (S1): $(I_{S1\_rms\_ON})^2 \times R_{ds\_ON}$

Switching losses in switch (S1):

$$V_{IN} \times \left(I_{OUT} - \frac{\Delta I_L}{2}\right) \times 0.5 \times (t_{r\_s1}) \times f_{sw} + V_{IN} \times (I_{OUT} + \frac{\Delta I_L}{2}) \times 0.5 \times (t_{r\_s1}) \times f_{sw}$$

Diode reverse recovery losses ($t_{f\_s1}$) = $V_{IN} \times Q_{rr} \times f_{sw}$

Conduction losses in switch (S2): $(I_{S2\_rms\_ON})^2 \times R_{ds\_ON}$

Switching losses in switch (S2):

$$V_{IN} \times (I_{OUT} - \frac{\Delta I_L}{2}) \times 0.5 \times (t_{f\_s2}) \times f_{sw}$$

Dead time and gate charge losses are for S1 and S2.

**Hardware design for the buck converter**

Dead time losses = $2 \times V_{S2Diode} \times (I_{OUT}) \times (t_{deadtime}) \times f_{sw}$

MOSFET gate charge losses = $2 \times Q_G \times fsw \times V_{GD}$

Where,

$t_{deadtime}$ = Dead time between S1 and S2

$t_{r\_s1}$ = Rise time of the S1

$t_{f\_s1}$ = Fall time of the S1

$t_{r\_s2}$ = Rise time of the S2

$t_{f\_s2}$ = Fall time of the S2

$Q_{rr}$ = Reverse recovery charge of the switch

$R_{ds\_ON}$ = MOSFET drain-source on-state resistance – datasheet parameter

$V_{GD}$ = Gate driving voltage

$Q_G$ = Gate charge

### 4.4.3 Power MOSFET selection – buck bypass mode

When the converter-connected device demands fixed DPO voltages such as 5.0 V, 9.0 V, 15.0 V, and 20.0 V to reduce the buck converter conversion losses, the buck bypass switch (S3) will be turned ON, and the front-end AC-DC converter provides the requested voltage. When the switch (S3) is turned on, the current passed through the switch $I_{S3}$ is the current drawn from the output. The switch average current is $I_{OUT}$. The S3 gets a gate drive signal from $V_{BUS\_CTRL}$.

## 4.5 Output capacitor selection

When there is a change in the load current (load transient), the converter's output feedback control loop senses the change and adjusts the duty cycle of the converter. Typically, in an application, the rate of change in load current is faster than the loop response. Therefore, add the output to support the load transients bulk capacitors, and for output ripple to be within the specified limits, add the high-frequency bypass capacitors (MLCCs) in parallel to the output bulk capacitors.

### 4.5.1 Output capacitor selection – buck mode

The output capacitor is required to maintain a regulated output voltage while the switch (S1) is OFF and must be able to respond to a change in the load current. It is necessary to minimize the amount of ripple on the output voltage. The output capacitors maximum ESR can be computed using the specified maximum output voltage ripple, $\Delta V_{OUT\ pk-pk}$ and the maximum load current $I_{OUT\_max}$. The maximum ESR of the output capacitors must be lower than the computed $R_{Cout\_max}$ to have an output voltage ripple below the specification value.

$$R_{Cout\_max} = 0.5 \times \left(\frac{\Delta V_{OUT_{pk-pk}}}{I_{OUT_{max}}}\right)$$

Where,

$\Delta V_{OUT\_pk-pk}$ = Allowed output voltage ripple, typically it will be 3 to 5 percent of $V_{OUT}$.

**Hardware design for the buck converter**

The output capacitor value in a buck converter to meet the specified ripple requirement is:

$$C_{OUT\_MLCC} \gg \frac{\Delta I_L}{8 \times f_{sw} \times \Delta V_{OUT\ pk-pk}}$$

The output capacitor must be able to handle output current transient requirements.

$$C_{OUT\_Bulk} = \frac{I_{OUT\_Step}}{\Delta V_{OUT\_transient}} \times \frac{1}{2 \times \pi \times f_{BW\_Buck}}$$

The output voltage ripple equation is as follows:

$$\Delta V_{OUT\ pk-pk} = \frac{\Delta I_L}{8 \times f_{sw} \times C_{OUT\_MLCC}} + \Delta I_L \times R_{C\ OUT\_max}$$

## 4.5.2 Output capacitor RMS current – buck mode

Ripple current flowing through the output capacitor in buck mode is:

$$I_{C\ OUT\_rms} = \sqrt{I^2_{L\_max\_buck} - I^2_{OUT\_max}}$$

Or RMS current in the output capacitor in buck mode is:

$$I_{C\ OUT\_rms} = \frac{\Delta I_L}{\sqrt{12}} \cong 0.3\Delta I_L$$

Where,

$\Delta I_L$ = Power inductor peak-to-peak ripple current (continuous conduction mode)

## 4.6 Current sense resistor selection

EZ-PD™ CCG7xC internal high-side current sense amplifiers (CSAs) measure the peak current ($I_{IN}$) sensing through an external CS resistor ($R_i$) placed in the $V_{IN}$ path. The drop across $R_i$ applies between the EZ-PD™ CCG7xC terminal CSPI and CSNI. The choice of external CS resistor ($R_i$) is critical to the control of the buck converter; a smaller value of $R_i$ will provide lower power loss, and at the same time, it should support the dynamic range required for the measurement.

A minimum of 5 mΩ CS resistor is required to have a good signal-to-noise ratio (SNR) in the feedback path and to accurately measure the input current. EZ-PD™ CCG7xC has the programmable CSA gain to amplify the feedback signal. Ensure the product of CSA gain and $V_i$ ($I_{IN} \times R_i$) is not more than 1.60 V. A CSA gain setting of 9 is recommended for better signal fidelity.

## 4.7 Bootstrap circuit design

A bootstrap circuit is used in half-bridge configurations to supply bias to the high-side MOSFET (S1), as it requires a voltage supply referenced at the source of the high-side MOSFET. The basic circuit elements are $C_{BOOT}$ and $D_{BOOT}$ are designed to reliably drive the high-side MOSFET.

**Hardware design for the buck converter**

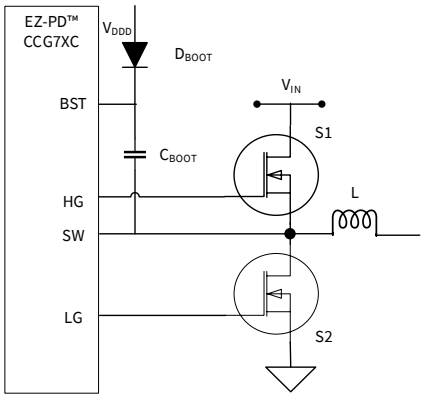


**Figure 13 Bootstrap circuit**

## 4.7.1 Bootstrap capacitor ($C_{Boot}$) design

The minimum charge needs to be supplied by the bootstrap capacitor: $Q_{bs} = 2 \times Q_g$

The bootstrap capacitor must be able to supply this charge and retain its full voltage. If that does not happen, there will be a significant amount of ripple on the $V_{BS}$ voltage (voltage across the $C_{Boot}$).

$$C_g = \frac{Q_g}{(V_{DDD} - V_{F\,BOOT\,DIODE})}$$

$C_{BOOT} \gg 20 \times C_g$

Where,

$V_{DDD}$ = Supply voltage

$V_{F\,BOOT\,DIODE}$ = Forward voltage drop across the bootstrap diode

$Q_g$ = Gate charge of high-side FET

The chosen bootstrap capacitor ($C_{BOOT}$) must withstand a minimum of switch node voltage (SW) + $V_{DDD}$ .

## 4.7.2 Bootstrap diode ($D_{Boot}$) design

The bootstrap diode ($D_{BOOT}$) must block the full power rail voltage when the high-side MOSFET (S1) is switched on. It must be a fast recovery diode to minimize the amount of charge fed back from the bootstrap capacitor ($C_{BOOT}$) into the $V_{DDD}$ supply. Similarly, the high-temperature reverse leakage current is important if the capacitor must store charge for long periods of time. The current rating of the bootstrap diode is the product of the gate charge of the MOSFET and the switching frequency ($f_{SW}$).

$I_{DBOOT} = Q_G \times f_{SW}$

## 4.8 Buck converter bypass FET design

The buck converter bypass switch is connected parallel to the synchronous buck converter. This proprietary configuration supports achieving higher efficiency. The bypass function is designed to operate when a device connects a USB Type-C connector and requests fixed output voltages (PDO), such as 5.0 V, 9.0 V, 15.0 V, or 20.0 V, complying with the USB PD standards. In this case, the front-end AC-DC converter output voltage directly routes to the USB-C connector via a MOSFET (Bypass) connected in parallel to the buck converter. By effectively bypassing the buck converter, the converter losses significantly reduce when the connected devices request PDOs.

The bypass MOSFET (S3) is controlled with the built-in high-side drive $V_{BUS\_CTRL.}$ The choice of buck bypass switch (S3) can be with lower $R_{ds\_ON}$, to have lower conduction losses. The MOSFET minimum drain current ($I_D$) can be the maximum load current and the minimum drain to source voltage ($V_{DS}$) can be the maximum input voltage applied to the buck converter.

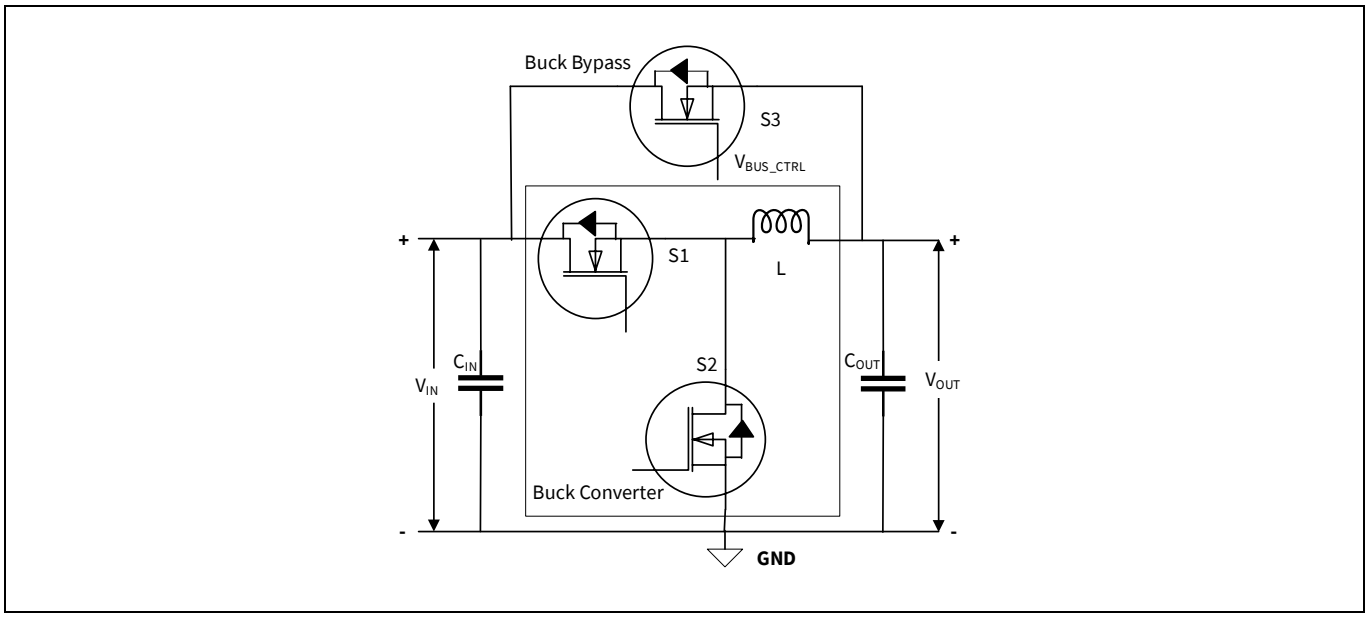


**Figure 14 Buck converter bypass FET**

## 4.9 Decoupling capacitor selection

The choice of decoupling capacitors at $V_{DDD}$, $V_{CCD}$, and $P_{VDD}$ must meet the values recommended in the EZ-PD™ CCG7xC datasheet and the typical values are shown in Figure 15. The chosen capacitors must have low ESR to bypass the AC signal present in the DC voltage, and typically it is a combination of high and low-value capacitors. The high-value capacitors, typically in the range of 4.7 to 10 µF, suppress the low-frequency noise, and the high-frequency noise is suppressed by low-value capacitors, typically in the range of 0.01 to 0.1 µF.

To absorb the dynamic change of voltages at $V_{BUS\_IN}$, $V_{BUS\_C}$, and $V_{IN}$, place the capacitor value in the order of 0.1 µF.

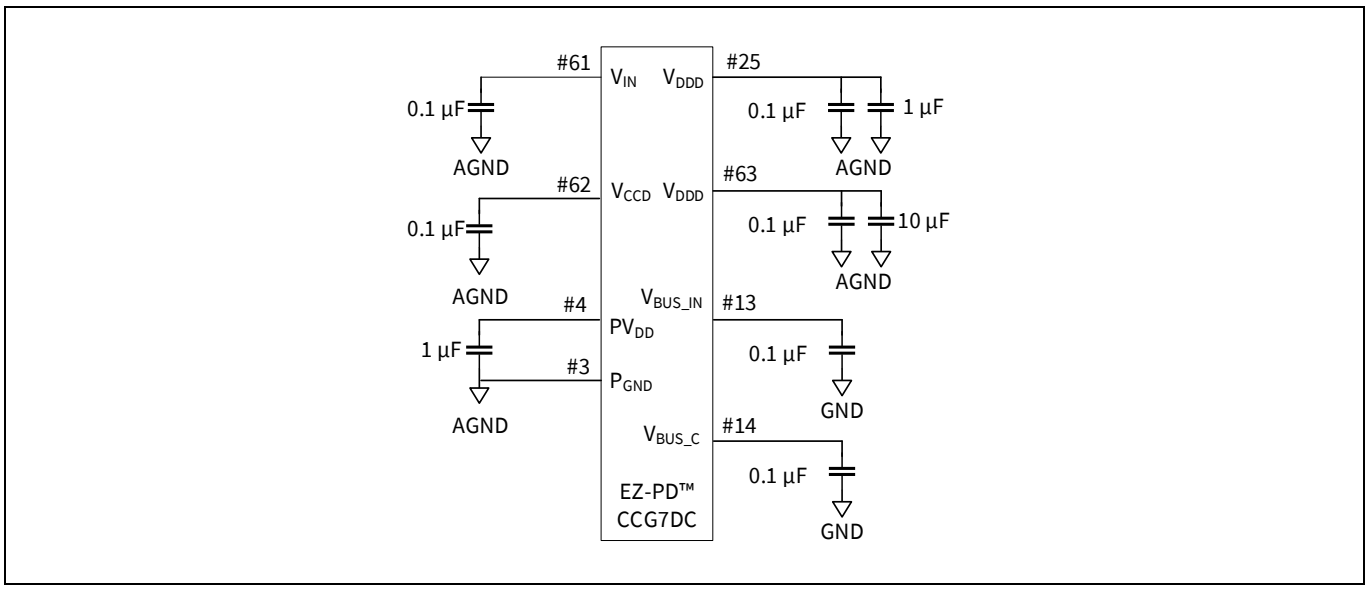


**Figure 15 Decoupling capacitors in EZ-PD™ CCG7DC**

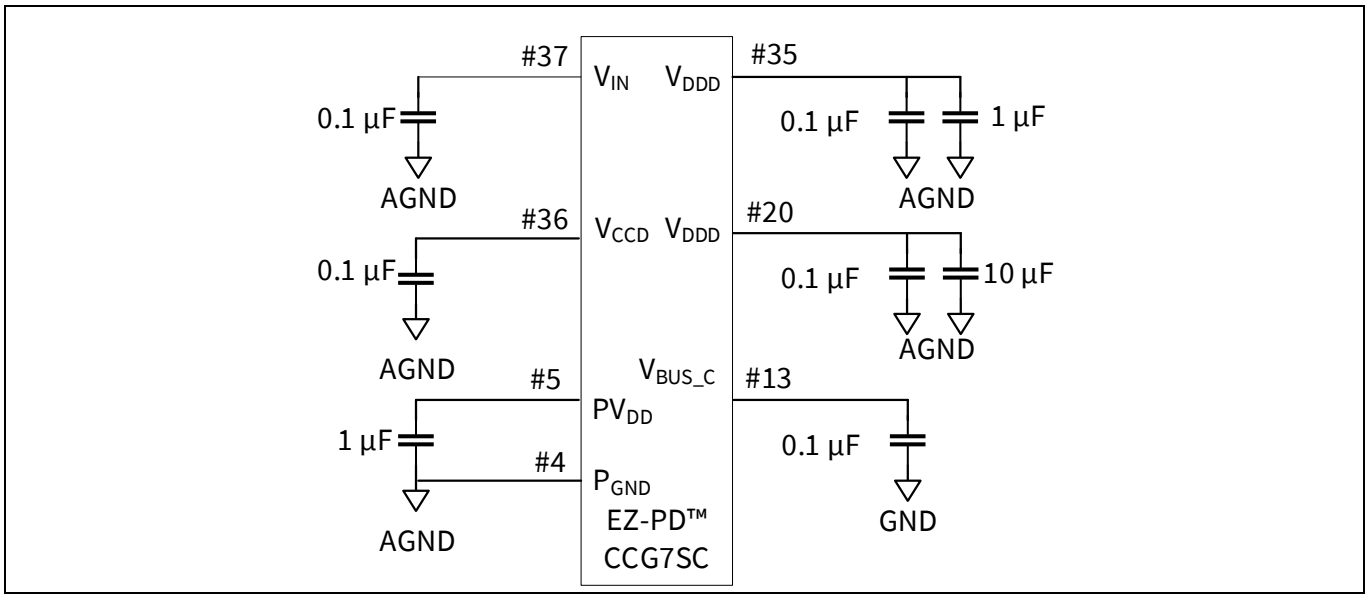


**Figure 16 Decoupling capacitors in EZ-PD™ CCG7SC**

## 4.10 Cable voltage drop compensation

In an ideal PD connection, the voltage at the sink port must be the same as the contracted voltage. Though the source supplies the requested voltage, the voltage at the sink end may be less because of the external cable voltage drop. The external cable voltage drop depends on two parameters: cable resistance and requested sink current. By considering the external cable resistance as a constant, which is a fixed value for a captive design and a typical value for a receptacle design, the source will supply an extra voltage in addition to the contracted voltage to compensate for the external cable drop for the changing load current or sink current.

The USB cable resistance goes up to ~500 mΩ, considering the use case of a more than 3-meter-long cable connected between the car dashboard and the rear charging port. Configure the USB cable resistance through EZ-PD™ Configuration Utility [4].

## 4.11 $V_{BUS}$ discharge

EZ-PD™ CCG7DC supports $V_{BUS}$ discharge capability on $V_{BUS\_IN}$ and $V_{BUS\_C}$ ends (before and after the provider FET, respectively). $V_{BUS\_IN}$ discharge is via #13, while the $V_{BUS\_C}$ discharge is via #14 of the EZ-PD™ CCG7DC for port #0, and $V_{BUS\_IN}$ discharge is via #39, while the $V_{BUS\_C}$ discharge is via #38 of the EZ-PD™ CCG7DC for port #1.

EZ-PD™ CCG7SC supports $V_{BUS}$ discharge capability on $V_{OUT}$ (pin #7) and $V_{BUS\_C}$ (pin #13) ends (before and after the provider FET, respectively).

The discharge FET and resistors are internal to EZ-PD™ CCG7xC and no need for external components for either of the discharge paths.

$V_{BUS\_IN}$ and $V_{BUS\_C}$ discharge are enabled upon disconnecting the USB cable and during the output voltage transitions from higher to lower voltage. The default discharge resistor values are set to 500 Ω on $V_{BUS\_IN}$ and 2 kΩ on $V_{BUS\_C}$. Maximum and minimum discharge strength values are software-configurable pre-processor switches. Configure the discharge drive strength through EZ-PD™ Configuration Utility [4].

## 4.12 CC and DP/DM terminations

EZ-PD™ CCG7xC supports termination needed on the CC line for Type-C Power Delivery. The only external component needed is a 390 pF capacitor on each of the CC lines (CC1 and CC2).

EZ-PD™ CCG7xC also has the required termination on the D+/D- lines to support the legacy charging protocols such as BC 1.2, Samsung AFC, Apple Charging, and Qualcomm Charging. EZ-PD™ CCG7xC supports two pairs of D+/D- lines, which is useful in dual-port charging systems.

# 5 Hardware configuration for buck-only converter

In the buck-only converter configuration, terminate the EZ-PD™ CCG7xC controller unused pins (boost converter application silicon/controller pins) as recommended:

- SW2 – Terminate this silicon/controller pin to power ground/battery negative terminal
- BST2 – Terminate this silicon/controller pin to $V_{DDD}$
- HG2 – Floating
- LG2 – Floating

# 6 Constant current and constant voltage regulation

The EZ-PD™ CCG7xC targets charging sink devices such as cell phones, battery banks, and laptops in the charger and adapter applications. The sink device broadcasts its state of battery charging to the source device, the EZ-PD™ CCG7xC built-in constant current (CC) loop, and a constant voltage (CV) loop, which transition automatically from CC to CV mode and vice versa based on the connected sink device battery status. In CC mode, EZ-PD™ CCG7xC modulates the feedback to keep the load current constant, and in CV mode, the output voltage is constant.

The CC/CV feedback loops implement using two transconductance amplifiers, and an external compensator network sets the frequency response of the CC and CV feedback loops. Figure 17 shows the port #0 control loop architecture of the EZ-PD™ CCG7DC pinout for reference. Figure 18 shows the control loop architecture of the EZ-PD™ CCG7SC pinout for reference.

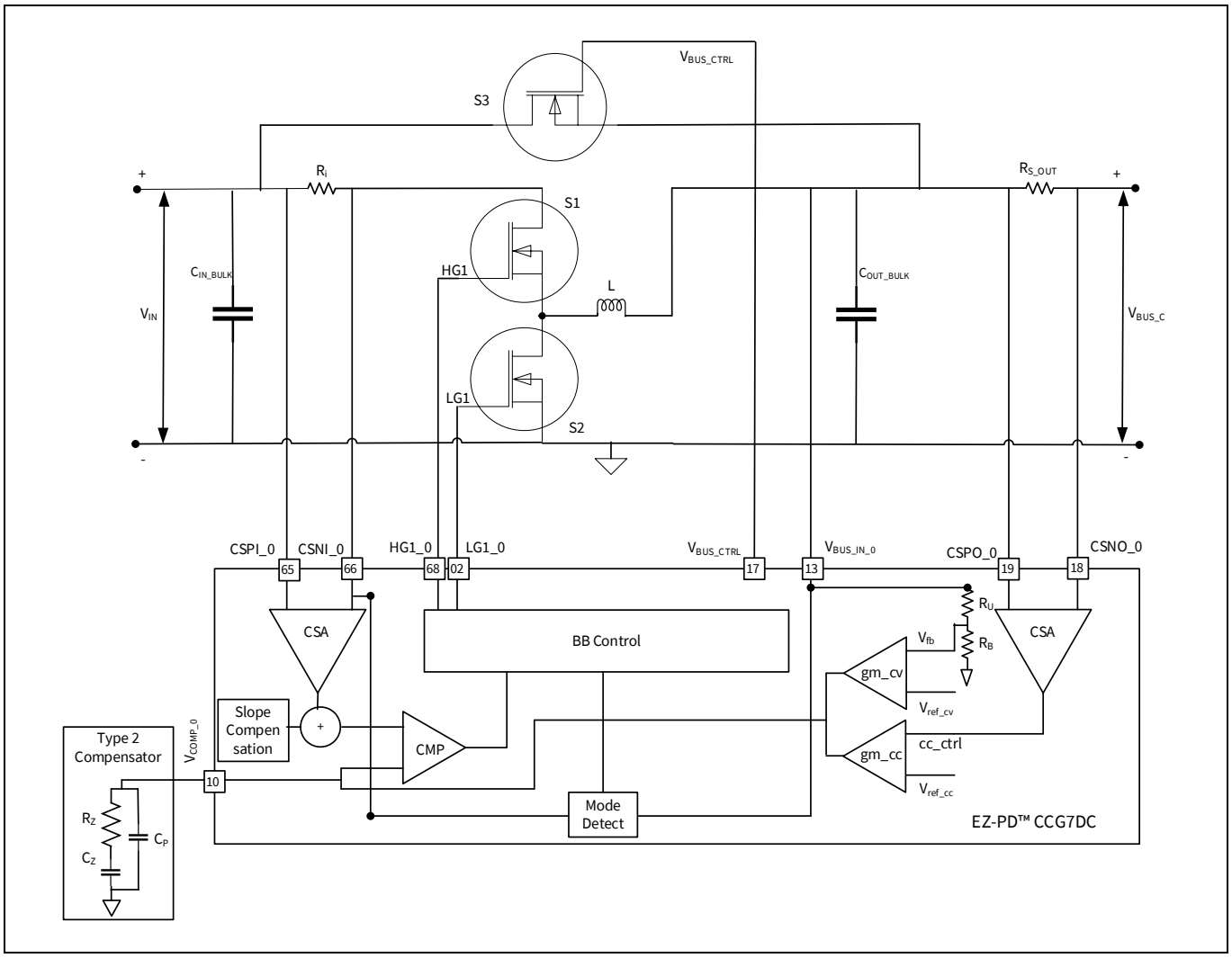


**Figure 17 Control loop architecture – EZ-PD™ CCG7DC**

The error amplifier block regulates output voltage ($V_{BUS\_C}$) or output current ($I_{OUT}$) during CV or CC mode, respectively. Figure 17 shows the port #0 control loop architecture.

### Constant current and constant voltage regulation

EZ-PD™ CCG7xC design regulates the constant output voltage ($V_{BUS\_C}$) in the 3.3 V to 21 or 21.5 V range, with a 20 mV step size as needed by the PPS specification. Default 5 V output voltage ($V_{BUS\_C}$) is dictated by the reference voltage $V_{ref\_cv}$ and the internal resistor divider of $R_U$ 200 kΩ and $R_B$ 34.5 kΩ. CC operation can be achieved based on the $V_{ref\_cv}$ setting and gain of the amplifier ($CSA_{OUTPUT}$).

The EZ-PD™ CCG7xC silicon family supports $V_{BUS\_C}$ current ($I_{OUT}$) measurement and control using an external sense resistor $R_{S\_OUT}$ (5 mΩ) in series with the $V_{BUS\_C}$ path. The voltage drop across the external sense resistor, $R_{S\_OUT}$, measures the average output current ($I_{OUT}$). $R_{S\_OUT}$ also controls the output current in the PPS current foldback mode of operation.

The CV and CC loops are independent of each other, sharing the same external compensation network. The compensation network must be designed based on the choice of the power converter operating mode and the chosen power stage component values.

Figure 18 shows the single-port EZ-PD™ CCG7SC controller-based control loop architecture and here CSNO is multiplexed with $V_{BUS\_IN}$.

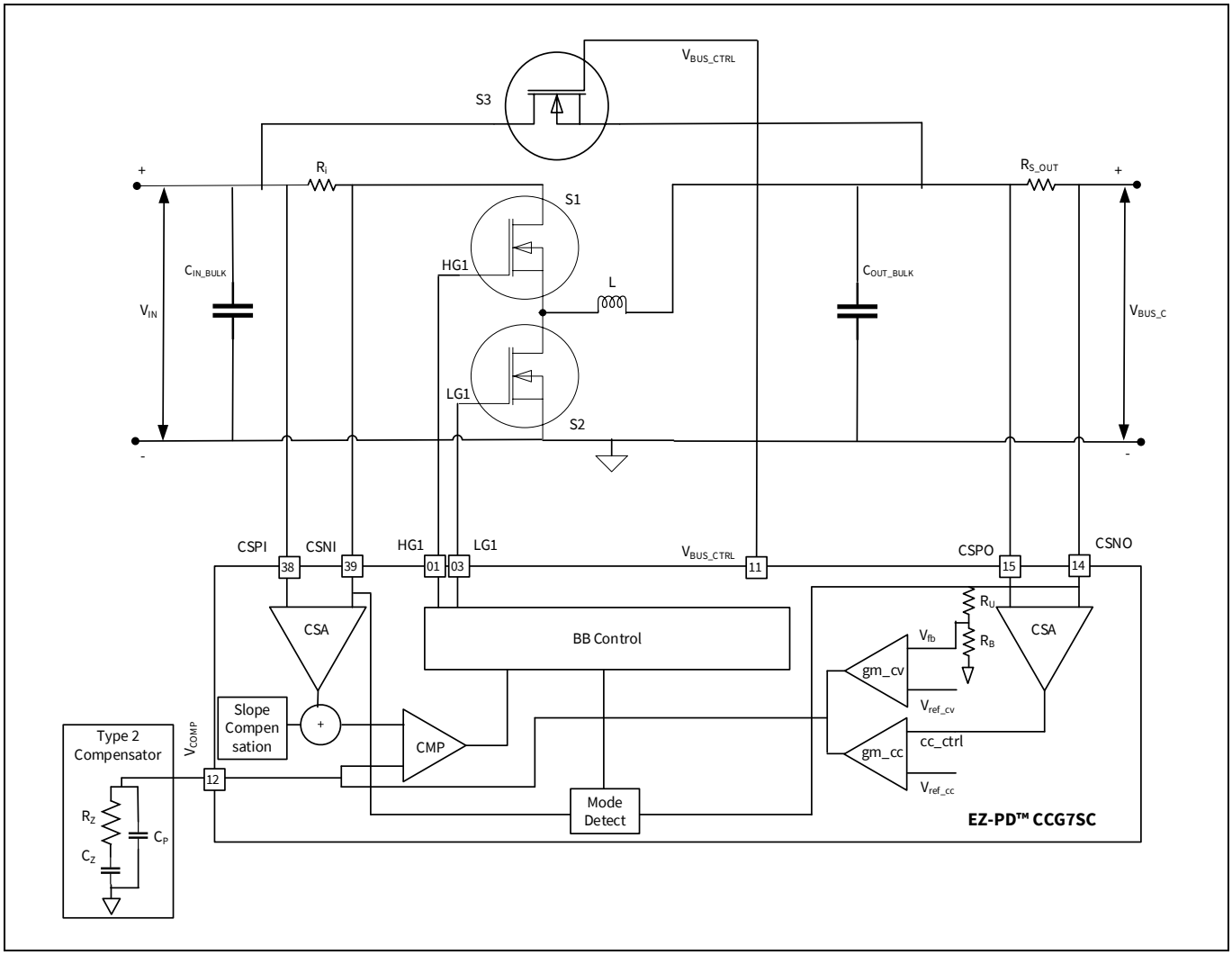


**Figure 18 Control loop architecture – EZ-PD™ CCG7SC**

# 7 Control system design

Type 2 external compensator component ($R_Z$, $C_Z$, and $C_P$) values are based on the desired loop crossover frequency ($f_c$), chosen power component values, and transconductance amplifier gain ($g_{m\_cv}$).

## 7.1 Type 2 compensator component selection

Compute the compensator resistor $R_Z$ by choosing the required crossover frequency. As a thumb rule, in a buck converter, the crossover frequency can be about one-tenth of the switching frequency.

$$R_Z = \frac{2\pi \times (R_U + R_B) \times R_i \times C_{out} \times f_c}{R_B \times g_{m\_cv}}$$ – for buck converter

EZ-PD™ CCG7xC has an internal resistive divider from the output to the error amplifier $R_B$ = 34.5 kΩ, $R_U$ = 200 kΩ.

$R_i$ is the input CS resistor multiplied by the input CS amplifier (CSA) gain ($G_{CSA}$).

The compensator zero ($f_{Zcomp}$) is placed at the dominant pole ($f_{pplant}$) of the power converter, simplifying the equation to get $C_Z$:

$$C_Z = \frac{R_{out} \times C_{out}}{R_Z}$$ – for buck converter

The compensator pole ($f_{Pcomp}$) is placed at ESR zero ($f_{zplant}$) of the power converter, simplifying the equation to get $C_P$:

$$C_P = \frac{R_{Cout} \times C_{out}}{R_Z}$$

# 8 Fault protections

The EZ-PD™ CCG7xC offers integrated fault protection features such as input UVP/OVP, output ($V_{BUS\_C}$) UVP/OVP, $V_{BUS\_C}$ OCP and SCP, $V_{BUS}$-to-CC short protection, and internal temperature protection. The EZ-PD™ CCG7xC supports board temperature measurement using external thermistors. This application note discusses a few external system-level fault protections.

## 8.1 Input UVP/OVP

EZ-PD™ CCG7xC supports input UVP and OVP when the input voltage is below or above reliable threshold levels. It guarantees predictable behavior when the EZ-PD™ CCG7xC is up and running. The input UV and OV fault thresholds are configurable using EZ-PD™ Configuration Utility [4].

## 8.2 Output ($V_{BUS}$) UVP/OVP

EZ-PD™ CCG7xC supports monitoring of output ($V_{BUS\_C}$) UV and OV faults using internal $V_{BUS\_IN}$/$V_{BUS\_C}$ resistor dividers. The fault thresholds and response times are configurable using EZ-PD™ Configuration Utility [4].

## 8.3 $V_{BUS}$ OCP and SCP

EZ-PD™ CCG7xC supports monitoring of output ($V_{BUS\_C}$) OC and SC faults using internal comparators. An SC is at a higher threshold compared to an OC threshold. Response times for SCP are much faster compared to OCP. External filters on the CS path increase the response time to OCP and SCP. The OCP and SCP thresholds and response times are configurable using EZ-PD™ Configuration Utility [4].

## 8.4 $V_{BUS}$-to-CC short protection

EZ-PD™ CCG7xC CC pins have integrated protection from accidental shorts to HV $V_{BUS\_C}$ and $V_{BAT}$. EZ-PD™ CCG7xC silicon handles up to 24 V external voltage on its CC pins without damage.

## 8.5 Built-in OTP

EZ-PD™ CCG7xC supports OTP through an integrated ADC circuit and internal temperature sensor. The overtemperature cutoff value, restart value, and debounce period (ms) are configurable using EZ-PD™ Configuration Utility [4].

## 8.6 $V_{CONN}$ switches and protection

EZ-PD™ CCG7xC's internal LDO voltage regulator is capable of powering a 100 mW $V_{CONN}$ supply for electronically marked cable assemblies (EMCAs), $V_{CONN}$-powered devices (VPDs), and $V_{CONN}$-powered accessories as defined in the USB Type-C specification [3]. All circuitries include $V_{CONN}$ switches and OCP is integrated into the device.

## 8.7 Transient voltage suppression (TVS) diode selection

The TVS diode at the input of a system protects the downstream electronic circuits and equipment during a transient overvoltage to immediately conduct and shunt current to the ground, keeping the system voltage exposure to a safe, low level. However, during normal operation, the TVS diode has no impact. Choose a diode which has a breakdown voltage ($V_{BR}$) higher than the normal operating voltage. Ensure that the nominal voltage ($V_{IN}$) stays below reverse standoff/reverse working maximum voltage, $V_{RWM}$, rather than breakdown voltage $V_{BR}$, to assure very low system leakage.

It recommends choosing discrete single-line TVS diodes which have low junction capacitance, low dynamic resistance, and ESD-withstanding capacity based on the regulatory/IEC standard.

Testing and measurement techniques - Electrostatic discharge immunity test (IEC 61000-4-2) relates to the immunity requirements and test methods for electrical and electronic equipment subjected to static electricity discharges, from operators directly, and from personnel to adjacent objects.

It recommends placing TVS diodes on the USB Type-C receptacle pins VBUS, CC lines, DP, and DM as shown in Figure 19.

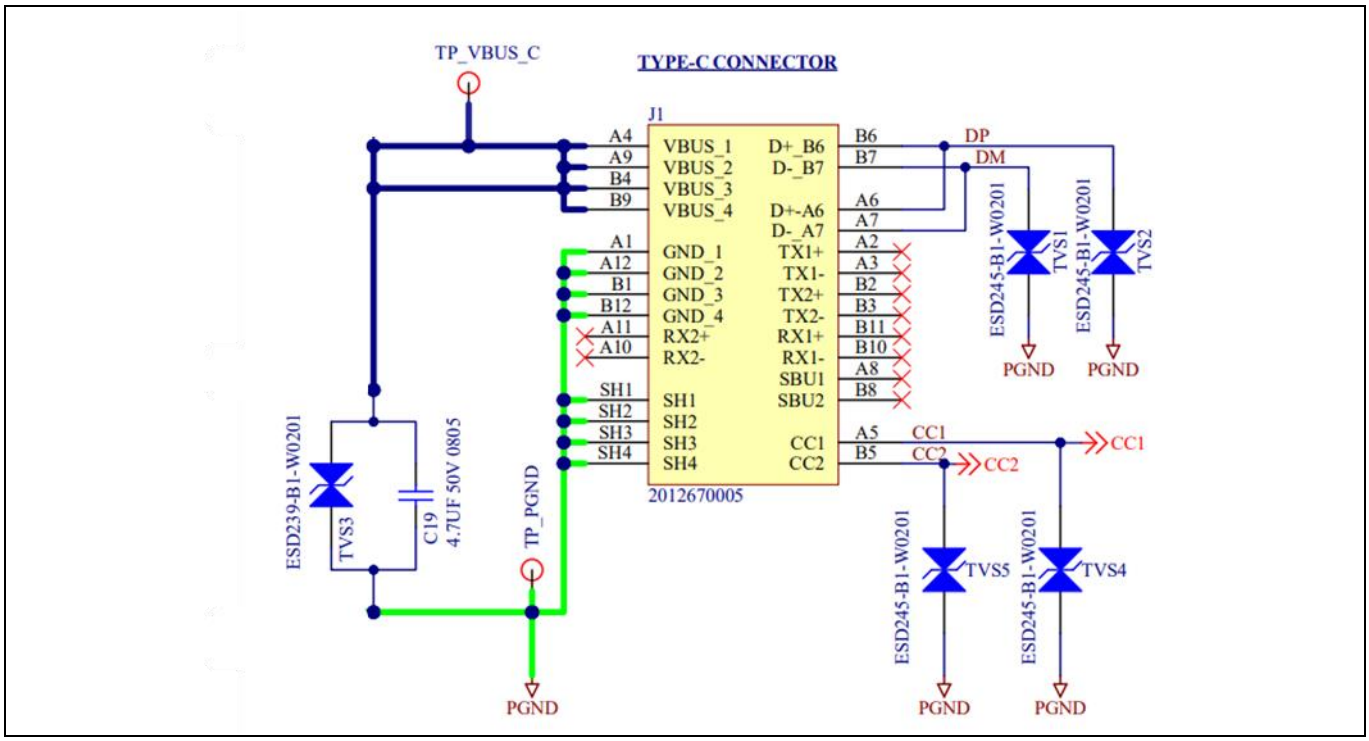


**Figure 19 Electrostatic discharge diodes on the USB Type-C connector**

## 8.8 External thermistor OTP

Measures the temperature of power circuit components in the vicinity with an NTC thermistor. The resistance falls as the temperature increases and measures the voltage drop across the thermistor to protect the circuit by turning off the PWM to the power-switching MOSFETs. Adjust the temperature thresholds by the choice of a series resistor connected to the NTC thermistor, and obtain these characteristics from the NTC datasheets. Select an NTC thermistor and resistor (R) value such that the voltage is linear in the desired temperature region.

In the case of EZ-PD™ CCG7DC, terminates port #0 NTC RT1 to silicon pin #60, and port #1 NTC RT2 to silicon pin #59 to sense the temperature of the NTC-placed locations. In the case of EZ-PD™ CCG7SC, terminates the NTC RT1 to silicon pin #22.

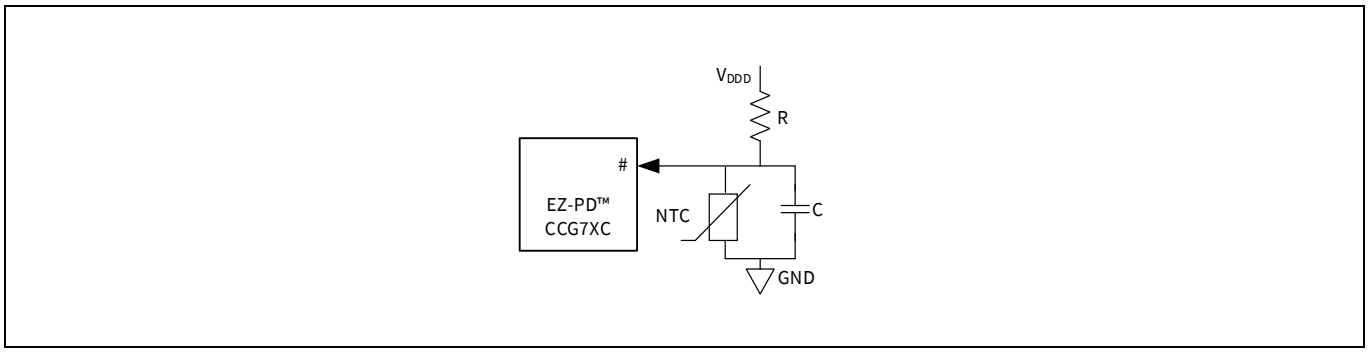


**Figure 20 NTC thermistor**

## 8.9 Protection diodes

In a highly noisy environment, ensure that signals are clamped to within the power rails specified in the EZ-PD™ CCG7xC datasheet table, “absolute maximum ratings”. Adding an external clamp diode prevents the device from exceeding operating conditions, which enhances the life span and corrects the functionality. Choose the clamping diode in such a way that its diode drop falls within the absolute maximum ratings. The diode connectivity is shown in Figure 21.

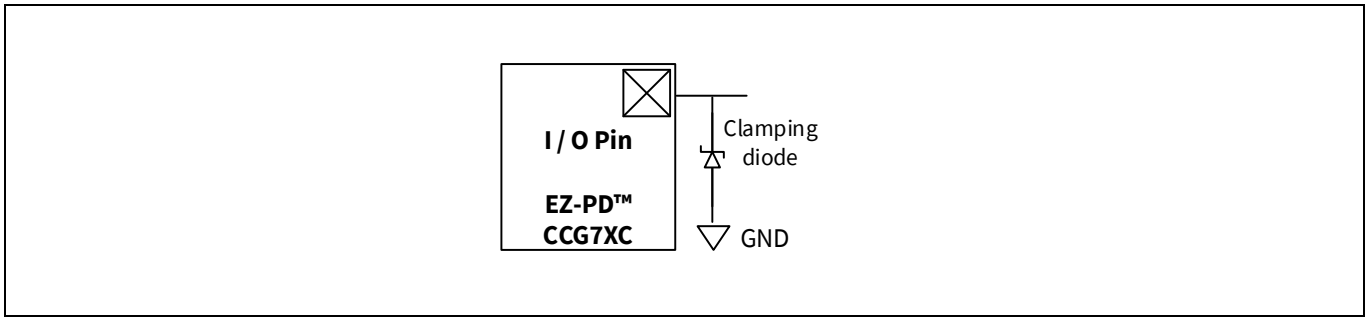


**Figure 21 External clamping diodes**

# 9 Application example – buck converter

## 9.1 Key specifications

- Input voltage range: +5.0 to +22.5 V DC
- Output voltage range: +3.3 to +21 V DC
- Output current range: 0.0 to 5.0 A

## 9.2 Power components selection – buck converter

Buck converter design example calculations use the following inputs.

- $V_{IN}$: 12 V DC, $V_{OUT}$: 5 V DC, $I_{OUT}$: 3 A, $f_{sw}$: 400 kHz; loop BW ($f_{C\_Buck}$): 10 kHz

**Table 2 Buck converter power components calculation**

| Parameter | Formula | Calculated value | Remarks |
|---|---|---|---|
| Input bulk capacitor | $\frac{D_{BUCK} \times I_{tran\_max}}{2 * \pi * f_{bw\_emi\_filter} \times V_{in\_transient}}$ | 11.05 µF | Considered load transient ($I_{tran\_max}$) 1A<br>EMI filter bandwidth ($f_{bw\_emi\_filter}$) 10 kHz<br>Allowed input voltage transient ($V_{in\_transient}$) 5 percent of $V_{IN}$ |
| Input MLCC | $\frac{D_{BUCK}\,(1 - D_{BUCK})\,I_{out\_max}}{\Delta V_{in\_pk-pk} \times f_{sw}}$ | 5.06 µF | Considered 3 percent of $V_{IN}$ as ($\Delta V_{in\_pk-pk}$) peak-to-peak ripple |
| EMI filter inductor [at $V_{IN}$ = 13.5 V, $V_{BUS\_C}$ = 12 V, $I_{OUT}$ = 3 A] | $Z_{filter}^2 \times C_{filter}$ | 1.27 µH | $Z_{filter}$ = ($R_{OUT}$/D^2)/10<br>$C_{filter}$ = (D×(1-D)×($I_{OUT}$))/($f_{sw}$ × $V_{IN\_RIPPLE}$) – here $V_{IN\_RIPPLE}$ considered as 150 mV<br>$R_{OUT}$ = $V_{OUT}$/$I_{OUT}$ |
| Power inductor | $\frac{(V_{in\_max} - V_O) \times D_{BUCK}}{\Delta I_L \times f_{sw}}$ | 8.1 µH | Considered 30 percent of $I_{OUT}$ as inductor ripple ($\Delta I_L$) – $I_{tran\_max}$ considered as 1.0 A |
| Output bulk capacitor | $\frac{I_{tran\_max}}{2 \times \pi \times f_{C\_Buck} \times V_{out\_transient}}$ | 106 µF | Considered 3 percent transient on the output voltage ($V_{out\_transient}$) |
| Output MLCC | $\frac{\Delta I_L}{8 \times f_{sw} \times \Delta V_{out\_pk-pk}}$ | 5.6 µF | Considered 1 percent of output voltage as output voltage ripple ($\Delta V_{out\_pk-pk}$)<br>$\Delta I_L = \frac{(V_{in} - V_{out}) \times D_{BUCK}}{L \times f_{sw}}$ |

## 9.3 Plant transfer function – buck converter

The plant transfer function for the buck converter is:

$$G_{vc}(s) = \frac{kR_O(1 + sR_{cout}C_{out})F_n(s)}{R_i(1 + kR_OC_{out}\,s)}$$

The above component values are considered for the following frequency analysis.

**Table 3 Buck converter plant calculations**

| Parameter | Formula | Calculated value | Remarks |
|---|---|---|---|
| Plant pole – 1 $f_{Pplant}$ | $\frac{1}{2\pi R_O C_{out}}$ | 1.1 kHz | $C_{OUT}$ is the sum of output bulk and MLCCs<br>$R_{OUT} = V_{OUT}/I_{OUT}$ |
| Plant zero $f_{zplant}$ | $\frac{1}{2\pi R_{cout} C_{out}}$ | 92 kHz | Consider ESR as 20 mΩ. Note the actual ESR value from the selected output capacitor. |
| Plant pole – 2 $F_n(s)$ | $\frac{1}{1 + \left(\frac{s}{\omega_n}\right)^2 + \frac{s}{\omega_n Q}}$ | 1256 kHz | $\omega_n = \pi f_{SW}$ |
| Plant DC gain | $k = \frac{\frac{k \times R_O}{R_i}}{\left(1 + \frac{T_s R_O}{L}(m_c D' - 0.5)\right)}$ | 28 dB | $m_C = 1 + \frac{S_e}{S_n}$, where $S_e$ is the external slope added (50 to 100 percent of ($V_{OUT}$/L))<br>$S_n$ is the input slope of inductor current ($V_{IN}$/L)<br>D = (1-D)<br>$T_s = 1/f_{sw}$ |
| Feedback network gain $G_{div}(s)$ | $\frac{R_B}{R_U + R_B}$ | 0.147 p.u. | $R_B$ = 34.5 kΩ<br>$R_U$ = 200 kΩ |

## 9.4 Compensator transfer function – buck converter

The compensator transfer function is:

$$G_{cv}(s) = \frac{(1 + sR_Z C_Z)}{sC_Z\,(1 + sR_Z C_P)}$$

**Table 4 Buck converter type 2 compensator calculations**

| Parameter | Formula | Calculated value | Remarks |
|---|---|---|---|
| $R_Z$ | $\frac{2\pi \times (R_U + R_B) \times R_i \times C_{out} \times f_{C\_Buck}}{R_B \times g_{m\_cv}}$ | 1.28 kΩ | $R_i = R_s \times CSA_{IN}\ g_{m\_cv}$ = 1.20 millisiemens<br>$CSA_{IN}$ = 9<br>$R_s$ = 5 mΩ<br>$f_{C\_Buck}$ = 10 kHz |
| $C_Z$ | $\frac{R_O \times C_{out}}{R_Z}$ | 104 nF | – |
| $C_P$ | $\frac{R_{Cout} \times C_{out}}{R_Z}$ | 1.25 nF | Considered ESR as 20 mΩ |
| Compensator pole $f_{PComp}$ | $\frac{1}{2\pi R_Z C_P}$ | 99.5 kHz | Locate the pole to cancel the plant zero |
| Compensator zero $f_{ZComp}$ | $\frac{1}{2\pi R_Z C_Z}$ | 1.19 kHz | Locate the zero to cancel the plant pole |
| Compensator DC gain | $20 \log (\frac{g_{m\_cv}}{C_Z})$ | 82 dB | – |

## 9.5 Loop transfer functions – buck converter

**Table 5 Buck converter loop transfer function calculations**

| Parameter | Formula | Calculated value | Remarks |
|---|---|---|---|
| Loop gain $G_{LTF}(s)$ | $\frac{R_B}{R_U + R_B} \times \frac{gm\_cv}{2\pi f_x} \times \frac{1}{R_i * C_{out}} \times R_Z$ | 1.09 dB | $f_x = f_{c\_Buck}$; loop gain will be "1" |
| Crossover frequency $f_{C\_Buck}$ | $\frac{R_B}{R_U + R_B} \times \frac{gm\_cv}{2\pi} \times \frac{1}{R_i \times C_{out}} \times R_Z$ | 10.9 kHz | Calculated crossover frequency is close to the designed crossover frequency |
| Loop phase | $90 + \mathrm{Tan}^{-1}\left(\frac{f_{C\_Buck}}{f_{ZComp}}\right) - \mathrm{Tan}^{-1}\left(\frac{f_{C\_Buck}}{f_{PPlant}}\right) + \mathrm{Tan}^{-1}\left(\frac{f_{C\_Buck}}{f_{ZPlant}}\right) - \mathrm{Tan}^{-1}\left(\frac{f_{C\_Buck}}{f_{PComp}}\right)$ | 90.04 degrees | – |

# 10 PCB layout guidelines – best practices

The PCB layout plays an important role in achieving the system's functional, EMC, and thermal goals. The following guidelines reduce the design cycle time and cost to achieve electrical performance and meet consumer regulatory standards. Obtain acceptable performance with alternate layout schemes.

- **PCB layers stack – multilayer board:** A multilayer PCB helps in achieving the highest level of signal integrity. These examples show the layer stacking for a single-sided component placement PCB design.
  - **Top layer:** Switching power components and power traces
  - **Second layer:** GND plane; it is common practice to almost fill with the ground completely; this is the layer immediately under the power components/traces layer
  - **Third layer:** Switching signals and GND plane. Ensure that signals in the third layer do not overlap with signals or power traces in the bottom layer
  - **Bottom layer:** DC and low-frequency signals, GND plane, and DC power traces

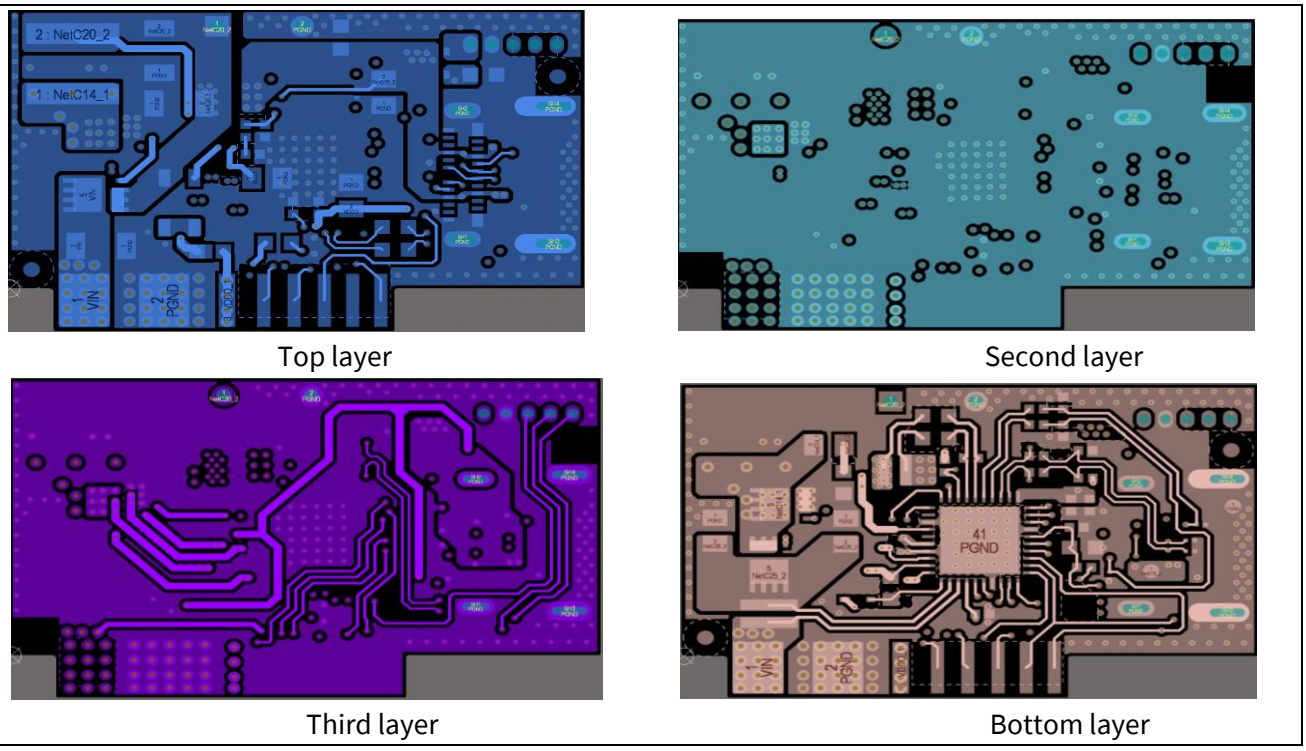


**Figure 22 PCB layers – top, second, third, and bottom layers**

- **Unused area:** In all layers, fill unused areas with copper to reduce the temperature of power components. Connect the copper areas to either $V_{IN}$, $V_{BUS\_C}$, or GND (preferably to GND).
- **Ground connection:** When routing the circuitry around the IC, the analog small-signal ground, and the power ground (used for the compensation networks) for switching currents must be kept separate. Connect at a point where switching activity is at a minimum to keep the analog ground quiet.
- **Ground plane:** Larger solid ground planes provide lower impedance; signals can disperse more easily with more area, reducing emissions, crosstalk, and noise. Ensure there is a good reason to use a split ground plane and they are only connected at a single point (some applications may demand separate analog and digital grounds to avoid noise coupling). Multiple ground connections in a split-ground PCB can create

### PCB layout guidelines – best practices

loops, resulting in an antenna that radiates EMI. The ground plane layer should be as close as possible to the layer with power MOSFETs.

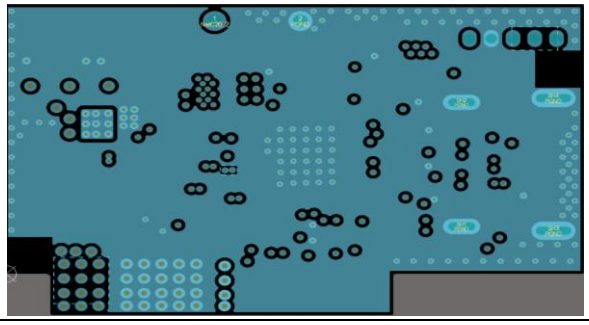

**Figure 23 PCB layer 2 (Ground plane)**

- **Ground vias:** Place several ground-connecting vias close to the component grounds directly to the dedicated ground plane. Do not keep the ground plane isolated. Stitch it to internal layers with vias for better EMI/EMC.
- **Avoid sharp right-angle bends:** Sharp right-angle bends cause changes in the characteristic impedance and reflections. This can be mitigated by rounding right-angle bends to help reduce the radiated EMI.
- **High dV/dT signals:** Keep the high dV/dT nodes such as SW1, SW2, BST1, BST2, HG1, and HG2 nodes away from sensitive small-signal nodes.
- **Separate high- and low-speed signals:** Keep high-speed signals such as PWM signals separate from low-speed signals such as compensation networks and analog signals separate from digital signals.
- **Control signals trace width:** To minimize the trace impedance, control signals traces should be at least 10 to 20 mil wide.
- **High current-carrying power-path traces:** High-current-carrying power-path traces should be as short as possible and should be sized to carry twice the rated current.
- **ESD immunity:** To improve the ESD immunity, connect MLCCs close to the USB Type-C connector GND and $V_{BUS}$ terminals through the low-impedance paths.
- **CC lines:** Keep trace length to a minimum from the Type-C receptacle to the configurable channel (CC) lines and the external ESD diodes.

# 11 Thermal considerations

In charger and adapter applications, the USB Type-C PD solutions are concealed in the casing without air cooling and an external heatsink. Typically, components such as power MOSFETs and inductors are surface mounted; therefore, the placement of power components and trace width, and the size of copper area are critical to limit thermal stress.

Place the power components in such a way that minimizes the length of the high-current flow paths through power MOSFETs, inductors, CS resistors, and input and output capacitors, which results in lower conduction losses. Low-impedance traces and solid low-impedance power component land patterns minimize thermal stress.

In a dual-output USB Type-C PD, ensure to have a symmetrical layout for each port to avoid hotspots.

See PCB layout guidelines – best practices for details of best practices to follow.

# 12 Circuit schematic and PCB layout review checklist

Table 6 is a checklist for the key circuit schematic component choices and Table 7 is a checklist for the PCB layout guidelines. Please provide an answer to each checklist item to find out the extent to which your hardware design meets these guidelines.

*Note: The silicon pinout details are based on the EZ-PD™ CCG7xC controller.*

**Table 6 Circuit schematic checklist**

| No. | Checklist item | Answer (Yes/No/NA) |
|---|---|---|
| 1 | Are the consumer-grade components chosen for the application? | |
| 2 | Are the current measurement resistors chosen with a minimum of 5 mΩ resistance value and is its tolerance better than 1 percent? | |
| 3 | Is the bypass capacitor connected between $V_{BUS\_IN}$ and GND 0.1 µF at maximum operating output voltage? | |
| 4 | Is the bypass capacitor connected between $P_{VDD}$ and $P_{GND}$ 1.0 µF at an operating voltage of 5.0 V? | |
| 5 | Is the capacitor connected at $V_{CCD}$ 0.1 µF at an operating voltage of 1.8 V? | |
| 6 | Is the bootstrap capacitor connected at the buck-side SW node and BST 0.1 µF at the maximum input voltage? | |
| 7 | Confirm that the chosen bootstrap diode forward voltage is small to ensure lower conduction losses. | |
| 8 | Confirm that the chosen bootstrap diode reverse recovery time is very small to achieve a reduction in reverse recovery losses. | |
| 9 | Confirm that a 1.0 µF capacitor is connected in parallel with 0.1 µF connected at VDDD pin #25 and this capacitor offers the specified capacitance at the operating voltage of 5.0 V. | |
| 10 | Confirm that a 10.0 µF capacitor is connected in parallel with 0.1 µF connected at VDDD pin #63 and this capacitor offers the specified capacitance at the operating voltage of 5.0 V. | |
| 11 | Confirm that a 0.1 µF ceramic bypass capacitor is connected at VIN pin #61 and the capacitor offers the specified capacitance at the maximum operating input voltage. | |
| 12 | Confirm that a 0.1 µF ceramic bypass capacitor is connected at VBUS_IN pin #13 and pin #39 to the ground and the capacitor offers the specified capacitance at the maximum operating output voltage. | |
| 13 | Confirm that a 0.1 µF ceramic bypass capacitor is connected at VBUS_C pin #14 and pin #38 to the ground and the capacitor offers the specified capacitance at the maximum operating output voltage. | |
| 14 | Confirm that provision is given for a ceramic capacitor between the silicon pins CSPO and CSNO. | |
| 15 | Is the 390 pF capacitor terminated between CC1, CC2, and ground respectively? | |

### Circuit schematic and PCB layout review checklist

| No. | Checklist item | Answer (Yes/No/NA) |
|---|---|---|
| 16 | Confirm that the chosen bulk capacitors carry the computed ripple current. | |
| 17 | Confirm that the calculated maximum temperature of the bulk capacitors is within the temperature range offered by the chosen capacitor. | |
| 18 | Confirm that the chosen bulk capacitors' ESR results in lower than the specification ripple limits. | |
| 19 | Do the chosen type 2 compensator resistor and capacitors have low tolerance across the operating conditions? | |
| 20 | Confirm that the chosen buck switches are of N-channel logic-level MOSFETs. | |
| 21 | Ensure that the chosen N-channel buck- MOSFETs' gate threshold voltage is much lower than 5.0 V. | |
| 22 | Confirm that the chosen buck bypass MOSFET is N-channel. | |
| 23 | Ensure that the chosen N-channel provider MOSFETs' maximum gate-source voltage is more than the DUT-rated output voltage. | |
| 24 | Ensure that the selected input TVS diode's reverse working maximum voltage ($V_{RWM}$) is higher than the maximum operating voltage. | |
| 25 | Ensure that the TVS diode breakdown voltage ($V_{BR}$) is significantly lower than the maximum allowable voltage rating of the silicon, specified in the silicon datasheet table "Electrical Specifications: Absolute Maximum Ratings and Pin Based Absolute Maximum Ratings" at $V_{IN}$, $V_{BUS\_C}$, DP, DM, CC1, and CC2? | |
| 26 | Ensure that the reverse current of the TVS diode ($I_R$) is low in nominal operating voltage. | |
| 27 | Confirm that the chosen inductors are magnetically shielded to minimize EMI. | |
| 28 | Confirm that the chosen inductor has a lower DCR value to ensure better efficiency. | |
| 29 | Is the chosen inductor's inductance variation less than 20%? | |
| 30 | Is the chosen inductor's saturation current much higher than the inductor's peak operating current? | |
| 31 | Are the selected power inductor SRFs much higher (at least 10 times) than the operating switching frequency? | |
| 32 | Is the selected NTC thermistor's operating range between -40°C and +125°C and/or lower than the maximum operating conditions of the DUT? | |
| 33 | Is the resistor connected in series with the NTC chip thermistor, and does the nominal resistance value meet the maximum operating temperature specifications? | |
| 34 | Is a capacitor connected across the (~1000 pF) NTC thermistor to roll off high-frequency noises? | |

### Circuit schematic and PCB layout review checklist

**Table 7 PCB layout guidelines checklist**

| No. | Checklist item | Answer (Yes/No/NA) |
|---|---|---|
| 1 | Is the EZ-PD™ CCG7xC exposed pad (EPAD) connected to the ground using vias? | |
| 2 | Are the EZ-PD™ CCG7xC SW1 and PGND pins routed differentially to the respective silicon pins with dedicated low-impedance trace? | |
| 3 | Are the EZ-PD™ CCG7xC SW1 and PGND traces provided with ground guarding on either side? | |
| 4 | Are the EZ-PD™ CCG7xC CSPI and CSNI pins connected to the input CS resistor using dedicated Kelvin connections with the shortest trace length? | |
| 5 | Are the EZ-PD™ CCG7xC CSPI and CSNI pins routed differentially, with no other switching or noisy trace next to them? | |
| 6 | Are the EZ-PD™ CCG7xC CSPI and CSNI traces provided with ground guarding on either side? | |
| 7 | Are the EZ-PD™ CCG7xC CSPO and CSNO pins connected to the output CS resistor using dedicated Kelvin connections with the shortest trace length? | |
| 8 | Are the EZ-PD™ CCG7xC CSPO and CSNO pins routed differentially with no other switching or noisy trace next to them? | |
| 9 | Are the EZ-PD™ CCG7xC CSPO and CSNO traces provided with ground guarding on either side? | |
| 10 | Are bootstrap capacitors and diodes placed close to the EZ-PD™ CCG7xC pins? | |
| 11 | Are compensator network elements ($R_Z$, $C_Z$, $C_P$) placed near the EZ-PD™ CCG7xC COMP pin and the silicon ground? Is it ensured that corresponding traces avoid noisy nodes and traces? | |
| 12 | Are the decoupling capacitors placed close to the silicon pin and silicon ground with minimum trace length? | |
| 13 | Is it ensured that the MOSFET gate driver traces are short and wide? | |
| 14 | Is it ensured that the solid ground plane is placed in layers adjacent to MOSFET gate driver signal traces? | |
| 15 | Is it ensured that the return current path is as short as possible? | |
| 16 | Are the high-frequency capacitors placed as close as possible to the half-bridges to ensure that the high di/dt current loop area is reduced significantly? | |
| 17 | Is it ensured that the SW node area is optimized? | |
| 18 | Is it ensured that any unused area is filled with copper and connected to GND? | |
| 19 | Are analog small-signal ground and power ground kept separated and connected at a point where switching activities are less? | |
| 20 | Is it ensured that a large solid ground plane is provided without any unnecessary split? | |
| 21 | Is it ensured that sufficient ground vias are placed near the component ground to the dedicated ground layer? | |
| 22 | Is it ensured that sharp right-angle bends are avoided? | |

### Circuit schematic and PCB layout review checklist

| No. | Checklist item | Answer (Yes/No/NA) |
|---|---|---|
| 23 | Is it ensured that high dV/dT nodes are kept away from sensitive small-signal nodes? | |
| 24 | Is it ensured that high-frequency and low-frequency signal traces are kept separate? | |

# References

[1] Infineon Technologies AG: *Bootstrap component selection for control ICs*; Available online

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[6] USB-C Power Delivery Controllers; Available online

[7] USB-C adapters and chargers; Available online

### Application notes

[8] Infineon Technologies AG: *Design considerations for EMI reduction in automotive power management systems*; Available online

[9] Infineon Technologies AG: *Hardware design guidelines for DRP applications using EZ-PD™ USB Type-C controllers*; Available online

[10] Infineon Technologies AG: *EZ-USB™ HX3 hardware design guidelines and schematic checklist*; Available online

[11] Infineon Technologies AG: *CoolMOS™ - How to select the right CoolMos™ and its power handling capability*; Available online

Contact Infineon Support to obtain these documents.

### Datasheets

[12] Infineon Technologies AG: *EZ-PD™ CCG7DC dual-port USB-C Power Delivery and DC-DC Controller*

[13] Infineon Technologies AG: *EZ-PD™ CCG7SC single-port USB-C PD and buck-boost controller (Preliminary)*

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[15] Infineon Technologies AG: *EZ-PD™ CCG7S Automotive single-port USB Type-C with PD and buck-boost controller*

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[17] Infineon Technologies AG: *EZ-PD™ CCG7x RSC power stage design calculator*

[18] Infineon Technologies AG: *EZ-PD™ CCG7D automotive rear seat charger (RSC) solution demo (SD2211) kit test report*

[19] Infineon Technologies AG: *EZ-PD™ CCG7S automotive rear seat charger (RSC) solution demo (SD2220) kit test report*

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|---|---|---|
| ** | 2023-10-31 | Initial release |

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