Hardware design guidelines for WLC transmitter

Applicable for WLC1115

About this document

Scope and purpose

This document provides design guidelines for the WLC1115-based power transmitter solution board for wireless charging (WLC) applications.

Intended audience

Wireless transmitter hardware designers using WLC1115 wireless transmitter with integrated USB Type-C power delivery (PD) controller.

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1 About WLC1115

Wireless power transmission, based on loosely coupled inductive power transfer, is a widely used near-field power conversion topology. These power transfer systems are common in consumer appliances such as electric toothbrushes or cell phone chargers, medical devices (power supply and implantable devices), and automotive (in-cabin charger) applications. The Qi wireless power topology utilizes series LC resonance tanks on both transmitter and receiver halves of the wireless power transfer system. The resonant topology offers low EMI along with ZVS turn-on of transmitter-side FETs and receiver-side rectifier FETs. The in-band communication between the transmitter and receiver sections offers a compact solution for wireless charging in low-power consumer applications.

WLC1115 is a highly integrated, Qi-compliant wireless transmitter with integrated USB Type-C power delivery (PD). It complies with the latest USB Type-C, WPC and PD specifications and has integrated gate drivers for buck and inverter power stage MOSFETs. It also includes hardware-controlled protection features on the VBUS. WLC1115 supports a wide input voltage range (4 V to 24 V). The single-chip solution provides system control and in-band communication (FSK modulation and ASK demodulation) with minimal external circuits.

1.1 WLC1115 features and applications

1.1.1 Typical applications

- Wireless charging pads for extended power profile (EPP) (15 W) and basic power profile (BPP) (5 W)
- Smart speakers
- Portable accessories
- Furniture and home goods
- Docking stations

1.1.2 Features

- Qi v1.3.x compliant transmitter (MP-A11 coil)
- Integrated USB-PD controller
- Supports latest USB-PD 3.1 version
- Programmable power supply (PPS) mode
- Configurable resistors (R_P, R_D)
- Support for USB-PD legacy charging protocols like QC 2.0/3.0 and AFC
- Integrated buck converter controller for VBRIDGE (VBRG)
- Integrated gate drivers for buck converter and inverter
- Integrated Q factor detection
- Integrated FSK modulator
- Wide input voltage range: 4.5 to 24 V
- Communication ports: I^2C, UART
- Protection
- Overcurrent protection (OCP), overvoltage protection (OVP)
- Supports overtemperature protection through integrated ADC circuit and internal temperature sensor
- Temperature range
  –40°C to +105°C extended industrial temperature range

- Package
  - 68-pin QFN 8.0 x 8.0 x 0.65 mm LD68B 5.7 x 5.7 mm E-PAD

Figure 1 shows the WLC1115 internal architecture in the form of a logic block diagram. Refer to the datasheet [2] for more details.

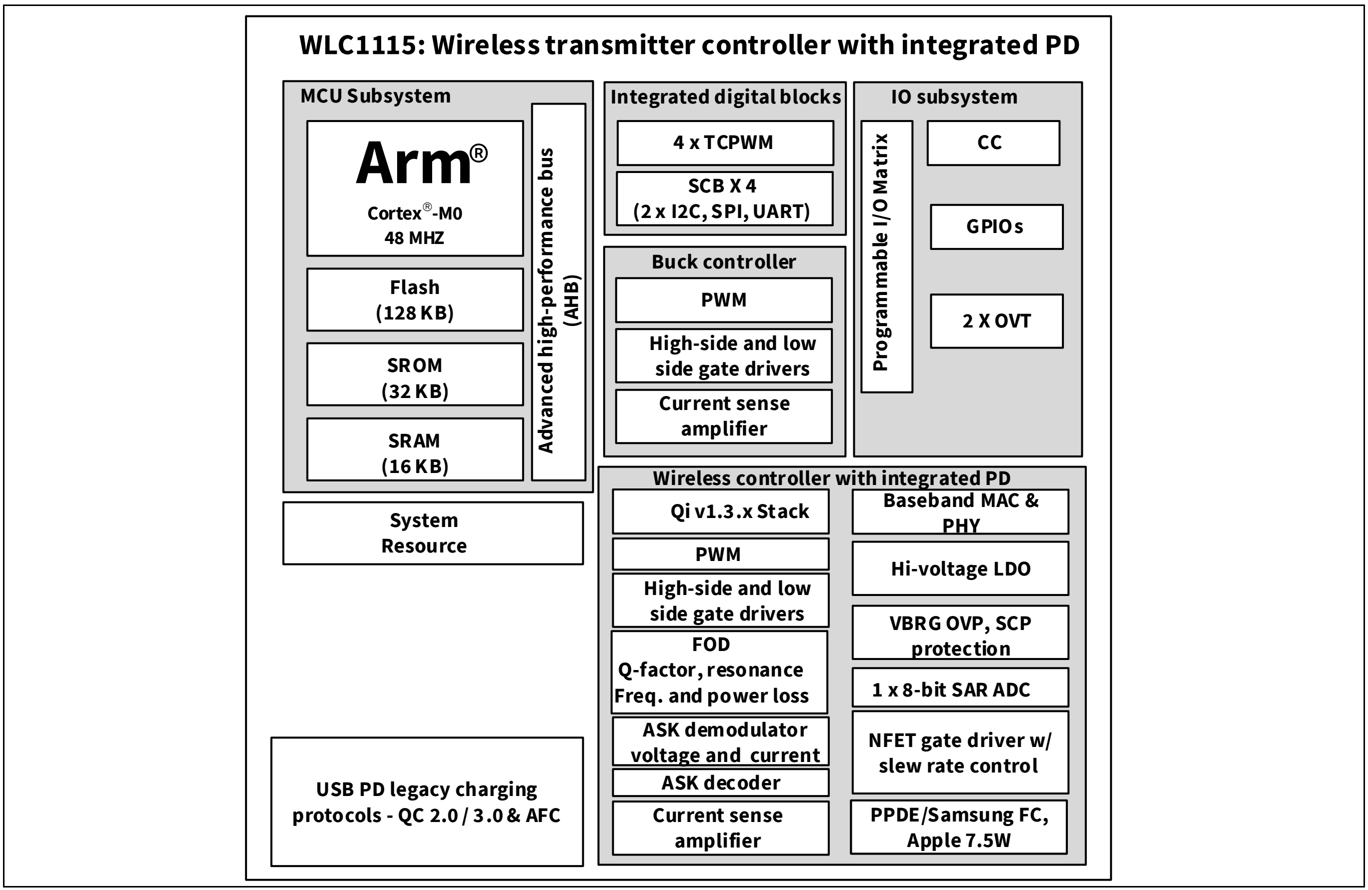


Figure 1 **WLC1115 logic block diagram**

1.2 WLC1115 in wireless transmitter application

A Qi-compliant wireless power transmitter unit with WLC1115 is shown in Figure 2 for the MP-A11 coil. A Qi-certified transmitter seamlessly works with a Qi-certified receiver irrespective of the make or the Qi Standard used. The most common power supply to the transmitter unit uses a USB-C power adapter through the Type-C connector. The MP-A11 coil-based transmitter system uses fixed-frequency variable-input voltage control for the inverter stage. The variable voltage is provided by the buck stage. With a USB-PD type input, the input voltage can be dynamically changed to keep the buck stage input close to the output, which optimizes the buck stage efficiency.

A transmitter board with WLC1115 needs a minimal number of external components for system control. Some signal conditioning circuits and amplifier circuits are required for the in-band communication. WLC1115 integrates the buck and inverter stage control. All the protection features for buck are also available within WLC1115. An external authentication chip interfaced to WLC1115 over I^2C completes the requirements for the Qi 1.3.2 Standard. The internal oscillator of WLC1115 meets the needs of FSK for in-band communication. For a higher-resolution clock (to have better accuracy for proprietary implementation), an external oscillator can be interfaced with WLC1115.

WLC1115 monitors the individual power stage currents and voltages for implementing the protection features. With an on-chip 32-bit Arm® Cortex®-M0 processor, 128 kB flash, 16 kB RAM and 32 kB ROM, the firmware supporting the complete Qi state machine logic can be programmed on to WLC1115.

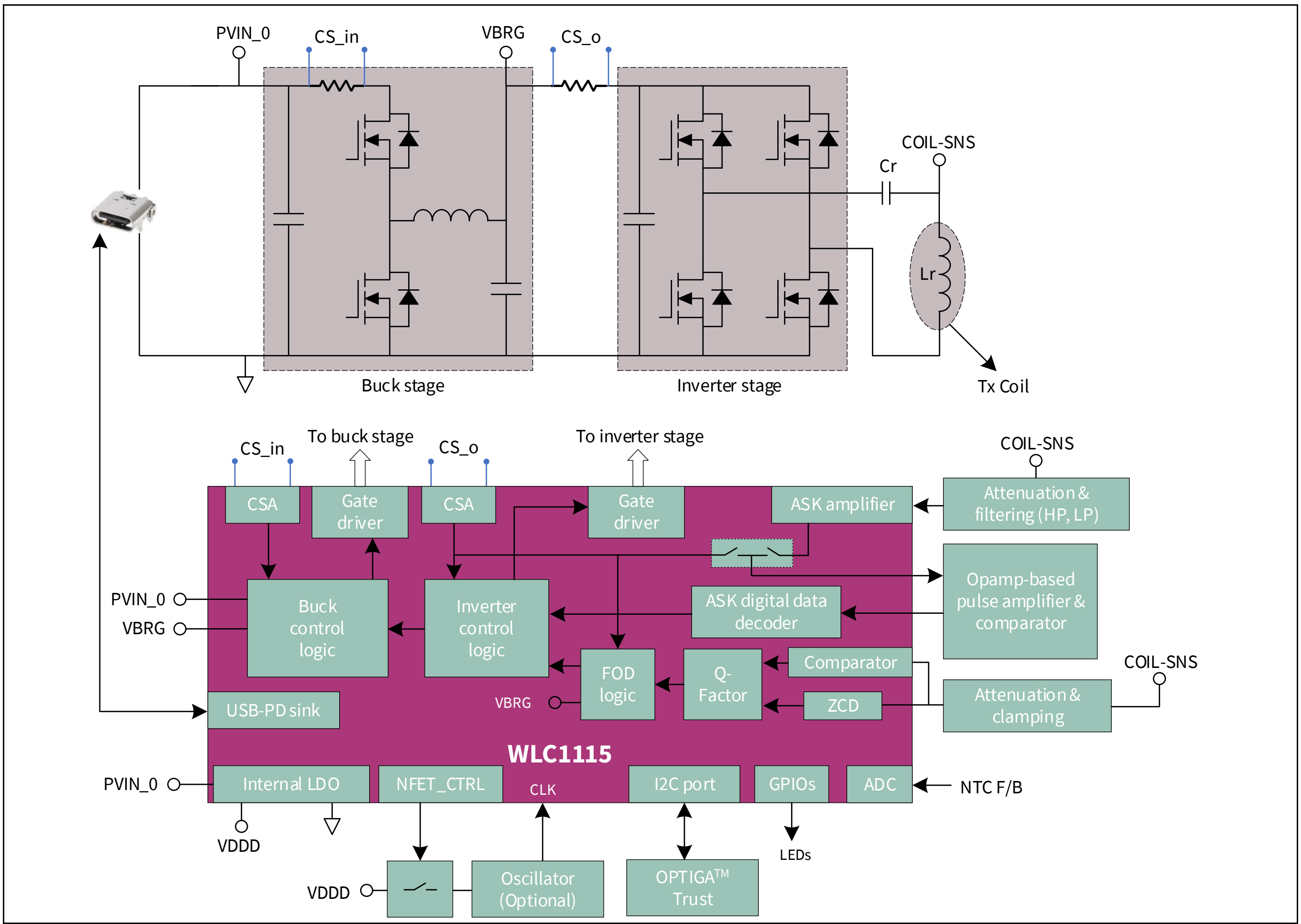


Figure 2 **Wireless power transmitter system with WLC1115**

1.3 MP A11 15 W power transmitter board (REF_WLC_TX15W_C1)

REF_WLC_TX15W_C1 MP-A11 15 W transmitter board, based on WLC1115, is a Qi-compliant transmitter design with MP-A11 type transmitter coil. The transmitter unit works with an input from a Type-C USB-PD adaptor. The transmitter board offers the following value propositions:

- Low bill of materials (BOM) cost for Qi v1.3.2 compliance
- Single MCU system that handles USB-PD, buck, inverter control and Qi state machine
- Form factor comparable to off-the-shelf chargers
- Simple to manufacture; ready-to-market layout
- Critical system-level parameters (foreign object detection (FOD) power loss threshold, inverter switching frequency, etc.) are configurable using a utility

The 15-W transmitter solution board is developed on a compact two-layer PCB. The PCB area under the MP-A11 transmitter coil is just FR4 without any copper. This is for a mechanically secure interface and for connecting the Tx coil to the PCB circuitry, and this part of the board can be cut. The board top-side placement section with key sections is shown in Figure 3. The wireless charger transmitter board key specifications are listed in Table 1.

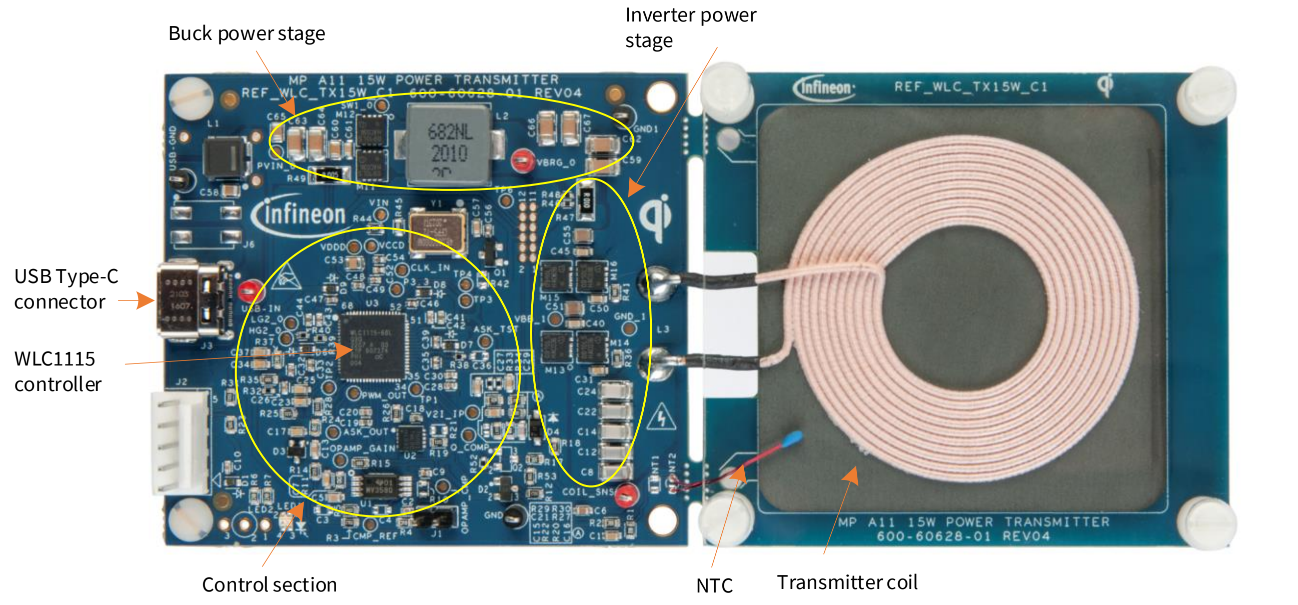


Figure 3 REF_WLC_TX15W_C1 MP-A11 15 W power transmitter board key sections

Table 1 REF_WLC_TX15W_C1 power transmitter board brief specification

Parameter	Value
Feature list	
Compatible transmitter coil	1-coil MP-A11
Input type/Connector	USB Type-C
Input PDO voltage	9 V, 15 V, 20 V
Typical output power	15 W
Peak system efficiency	More than 83 percent with test receiver WRM483265-10F5-12V-G
Inverter switching frequency	127.7 kHz
Standby power	13.4mA at 5V i.e 67mW
ASK demodulator	AC voltage (coil voltage) based and DC current based
FSK modulator	Meets Qi v1.3.2 requirements
Foreign object detection	Based on power loss, Q-factor and resonant frequency
Other Protections	OVP, UVP, OCP, short-circuit protection (SCP), OTP
Authentication	Meets Qi v1.3.2 requirements
PCB details	59 x 66 mm/two layers/2 oz. copper
Operating temperature	0°C to +85°C
Storage temperature	-40°C to +125°C
Other features	Samsung proprietary extension, up to 7.5W charging for iPhones
Compliance / Certification	
USB certification	USB PD v3.1
Qi certification	Qi 1.3.2
Conducted and radiated emission pre-compliance	CISPR 32 Class B or equivalent

2 Hardware design

This section covers the requirements and design or selection criteria for the transmitter board key components shown in Figure 4. The blocks in gray indicate the power stage components. The blocks in green are the circuit blocks for the control section of the WLC1115-based wireless transmitter design.

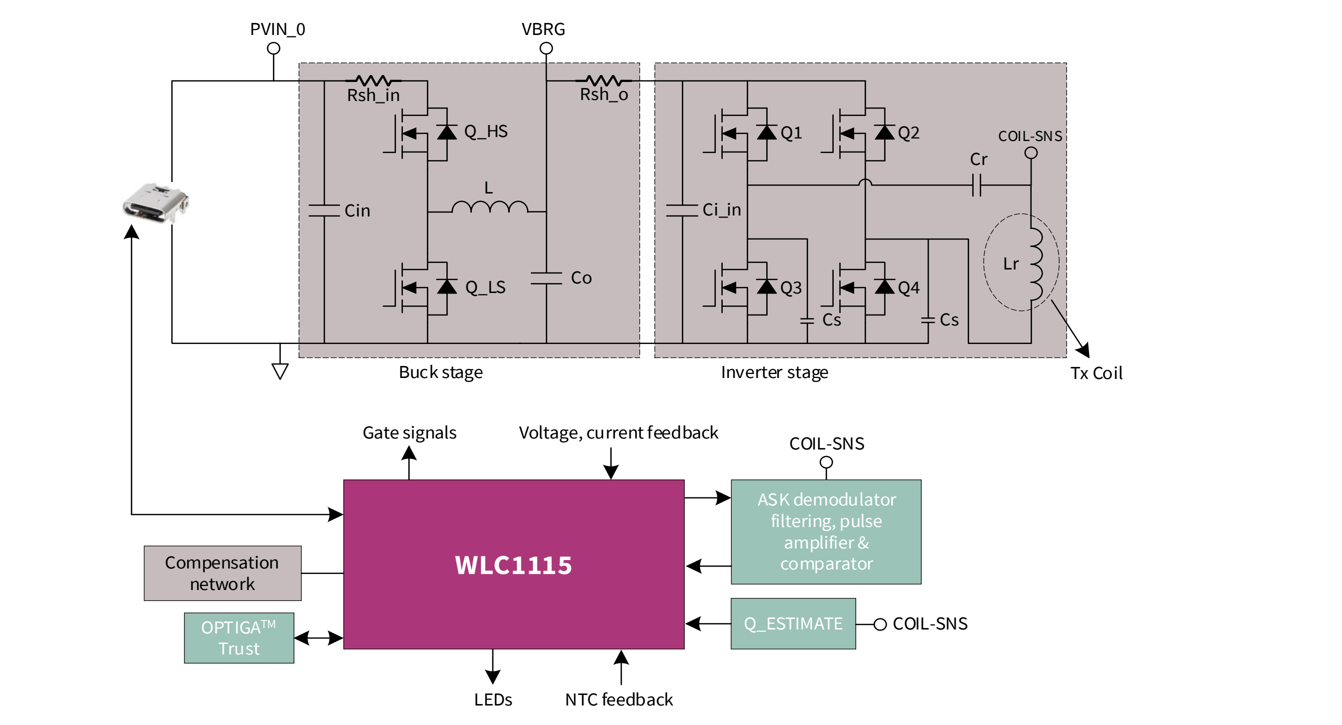


Figure 4 **WLC1115-based wireless transmitter board key components**

2.1 Buck power stage

The DC-DC converter stage in REF_WLC_TX15W_C1 is shown in Figure 5. The power stage consists of a filter at input, a synchronous buck converter power stage, and shunt resistors for control and output current measurements.

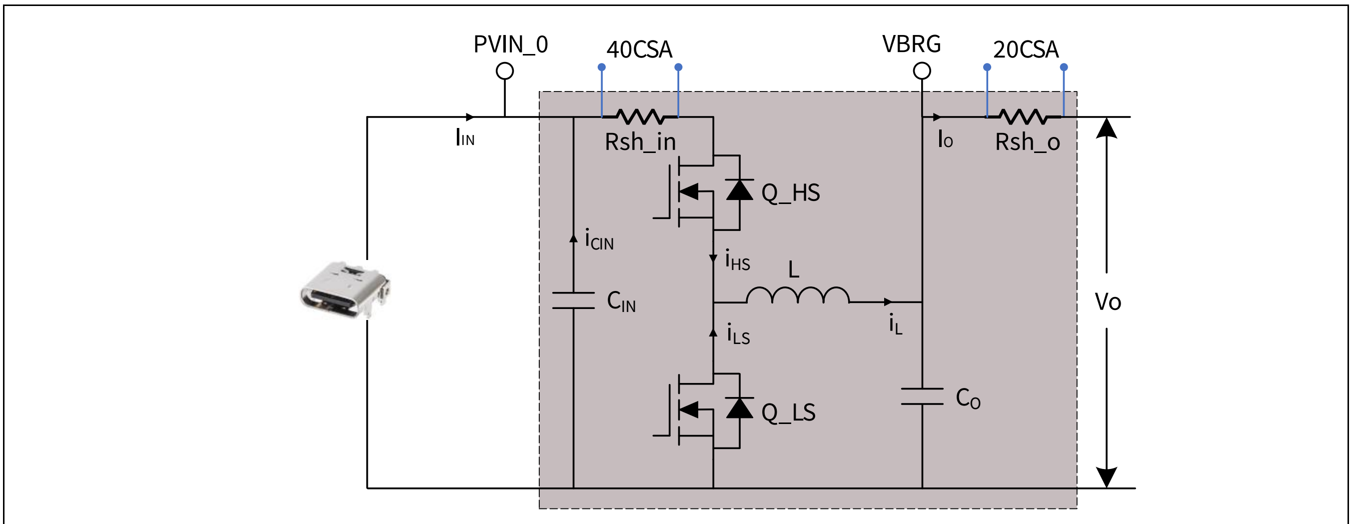


Figure 5 **Buck converter stage in REF_WLC_TX15W_C1**

The input to the buck converter is from a USB-PD source or from a standard AC-DC power adapter with fixed output voltage. With a USB-PD input, the PD contract is adjusted dynamically based on the buck converter output voltage requirement to keep stress on FETs minimal and hence achieve good efficiency. The closed-loop control for the buck stage is based on peak current mode control (PCMC), most of which is implemented inside WLC1115. The external components for control are the Type 2 compensation network components (refer to section 2.1.7). The output voltage and Q_HS current are used for output voltage regulation. Since the gate drivers, high-side current sense (CS) amplifiers and voltage feedback networks are integrated into WLC1115, the converter stage is highly simplified.

Use of WLC1115 helps in having the following features for the buck stage:

- Highly integrated PD-based solution, compliant with latest USB Type-C PD requirements
- Integrated gate drivers and firmware-configurable turn-on/-off gate drive strength
- Switching frequency range up to 600 kHz
- Flexibility to dynamically change input voltage to 5 V, 9 V, 15 V or 20 V with PD input
  - Helps achieve good efficiency
  - Reduces standby power by operating at 5 V in idle mode
- Protections on input and output side of buck stage
  - Input UVP, OVP
  - Output UVP, OVP
  - Output OCP, SCP
  - Protections specific to PD (e.g., VBUS to CC short)

The steady-state waveforms for key components of the buck converter are shown in Figure 6 for continuous conduction mode (CCM) or forced continuous conduction mode (FCCM) operation. The design and selection of power stage components of the buck stage can be derived from the steady-state waveforms.

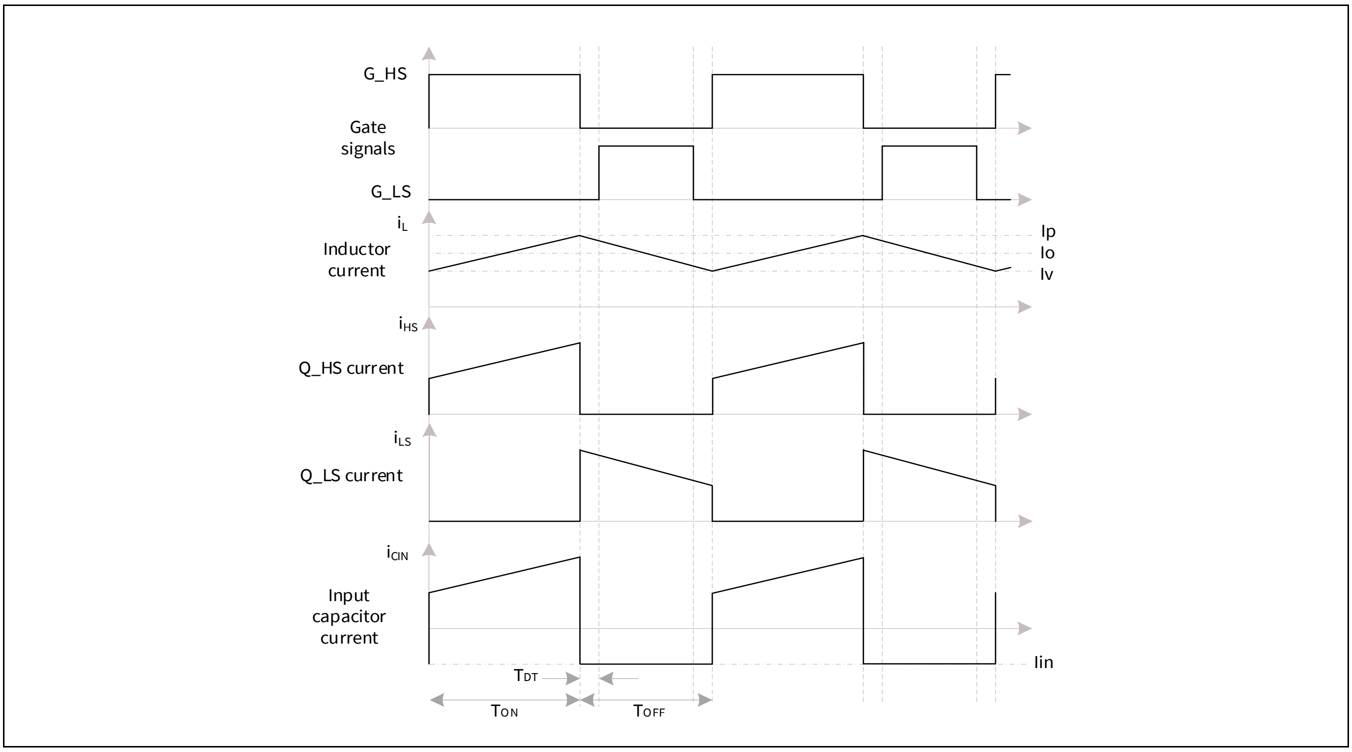


Figure 6 **Buck converter steady-state waveforms for CCM/FCCM operation**

2.1.1 Inductance requirement and selection

The inductance value for the buck power stage is set to keep the converter in CCM at full load. The inductance value is computed as follows:

$$L = \frac{V_{in}D(1-D)}{F_S \Delta i_L}$$

Where:

V_{in} – input voltage

D – buck operating duty cycle

$$D = \frac{T_{ON}}{T_{ON}+T_{OFF}} = T_{ON}F_S = \frac{V_O}{V_{in}}$$

F_S – switching frequency

Δi_L is the ripple current in the inductor and is set to around 50 percent to 70 percent of average inductor current I_O. For high-power applications, Δi_L is set to around 20 percent to 40 percent of I_O, which is useful for reducing EMI levels and current stress on FETs and filter capacitors.

From the inductance equation, the ripple current is at the maximum when the duty cycle is 0.5.

Inductor RMS current – The inductor current contains ripple content on a DC current. The inductor RMS current for design/selection and loss estimations is calculated as:

$$I_{Lrms} = \sqrt{{I_O}^2 + \left(\frac{\Delta i_L}{2\sqrt{3}}\right)^2}$$

Where I_O is the average output current and is the same as the average inductor current.

Inductor peak current – The peak current rating without saturation is based on full load current for 150 percent load (short-term overload expected for a few seconds) and ripple current for the same operating conditions.

$$I_{Lpk} = (1.5 \text{ x } I_O) + \frac{\Delta i_L}{2}$$

Inductor losses – The inductor has a copper loss and a core loss component. The copper loss arises from the DC resistance of the inductor. The AC resistance due to ripple is ignored.

$$P_{Lcu} = {I_{Lrms}}^2 R_{Ldc}$$

The ripple current and associated magnetic flux swing in the inductor core contribute to core losses. The core loss data as a function of flux swing ΔB and frequency is given by the manufacturer:

$$P_{Lcore} = C{F_S}^{\alpha}\Delta B^{\beta}V_e$$

Where the constants C, α and β are specified by the manufacturer, V_e is the core material volume. Alternatively, the manufacturer provides tools for easy computation of losses in the inductor.

Inductor selection guidelines – The selected inductor part should meet the following requirements:

1. Inductance value to satisfy the ripple current requirements for the entire operating range
2. Current rating greater than I_{Lrms} and I_{Lpk}
3. Low DCR for low conduction loss and thermal rise

4. Core material with low core loss at 400 kHz
5. Shielded construction for low radiated emissions
6. SMD type mounting

2.1.2 Buck stage input capacitor

As shown, when the high-side MOSFET is turned on, the MOSFET current is pulsating with peak current equal to the inductor peak current. This pulsating current has higher magnitude than the average input current, causing larger voltage ripple and higher EMI.

Input filter capacitors, placed close to the FETs, provide a low-impedance path for pulsating currents, and clean current is drawn from the source. When Q_HS is turned on, the capacitor current is the difference between input current I_{IN} and inductor current $i_L(t)$. The capacitor discharges in this state and, along with I_{IN}, provides energy to load. When Q_HS is turned off, the input capacitor is charged with a current equal to I_{IN}. As the capacitor charges, there is a ripple ΔV_{in} across capacitor and the magnitude of ripple is dependent on capacitance value and the ESR of the capacitor.

$$I_{IN} = C_{IN}\frac{d\,V_{in}}{dt} = C_{IN}\frac{\Delta V_{in}}{T_{OFF}}$$

$$C_{IN} > \frac{I_{IN}(1-D)}{\Delta V_{in}\,F_S}$$

Where I_{IN} is the input current:

ΔV_{in} is the ripple voltage allowed in input (recommended to be set at less than 3 percent of V_{in}).

The input capacitor RMS current, derived from the waveform in Figure 6**,** is:

$$I_{CIN_{rms}} = \sqrt{\frac{1}{T_S}\int_0^{T_S} i_{CIN}(t)^2\,dt}$$

$$I_{CIN_{rms}} = \sqrt{\frac{1}{T_S}\int_0^{DT_S} (i_L(t)-I_{IN})^2 dt + \int_{DT_S}^{T_S} {I_{IN}}^2 dt}$$

$$I_{CIN_{rms}} = \sqrt{\frac{1}{T_S}\int_0^{DT_S} \left(I_O - \frac{\Delta i_L}{2} + \frac{\Delta i_L\,t}{D\,T_S} - I_{IN}\right)^2 dt + \int_{DT_S}^{T_S} {I_{IN}}^2 dt}$$

$$I_{CIN_{rms}} = \sqrt{D\left({I_O}^2(1-D) + \frac{{\Delta i_L}^2}{12}\right)}$$

Power loss in capacitor – The power loss in the input capacitor is due to the capacitor ESR and the associated ripple current in it.

$$P_{Cin} = \frac{{I_{CIN_{rms}}}^2 R_C}{N_{cap}}$$

Where

R_C – ESR of capacitor part selected

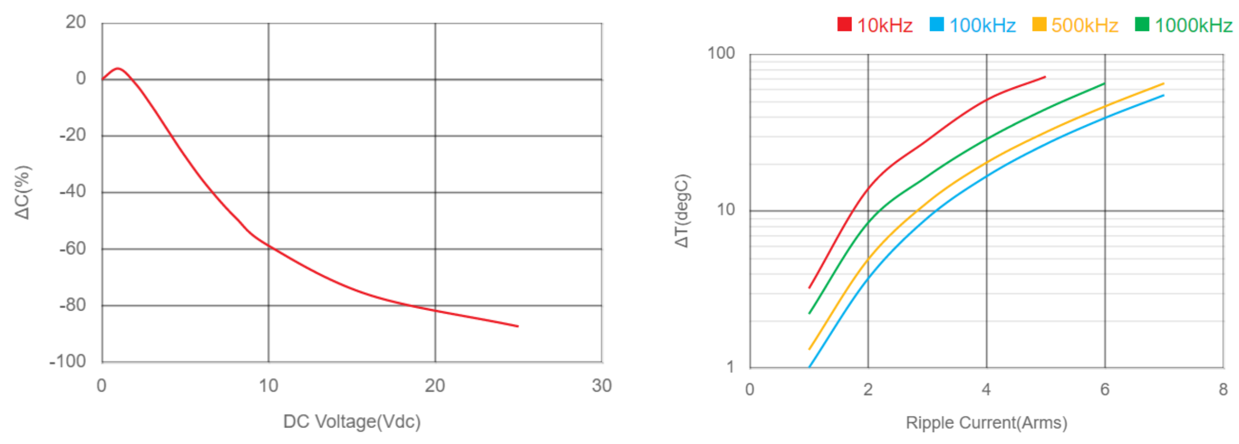
N_{cap} – number of capacitors connected in parallel

The formula is valid under the assumption that the capacitors are identical in value and electrical properties.

Capacitor selection guidelines

- **Capacitor voltage rating** The capacitor should be rated for the withstanding voltage in Table 1. Ceramic capacitors, most suitable for low-voltage DC input, are available with X5R, X6R or X7R dielectric and have a range of capacitance values with applied voltage.

Figure 7 (a) shows capacitance vs. DC bias for a CL31X226KAHN3NE (22 µF 25 V rated) capacitor. At 20 V, the capacitance drops down to 4 µF (82 percent dip). The capacitor bank should be sized based on this bias characteristic. The number of capacitors in parallel should ensure that the effective capacitance value is greater than or equal to C_{IN} for the particular operating input voltage.



(a) Capacitance change with bias (b) Temperature rise with ripple current

Figure 7 CL31X226KAHN3NE characteristics

- **Capacitor ESR** – C_{IN} effective capacitance calculated value only deals with the voltage ripple caused by the discontinuous capacitor current inherent in the switching behavior of the buck regulator. There will be additional voltage ripple caused by the C_{IN} ESR and the buck input capacitor switching current ripple; therefore, the additional input voltage ripple resulting from the current through the input capacitors can be calculated by the following equation:

$$\Delta V_{in} = \frac{I_{IN}(1-D)}{C_{IN}\,F_S} + I_{IN}R_{C_{IN}}$$

The ESR-induced ripple should keep the overall ripple voltage below the desired ΔV_{in}. Paralleling of capacitors will reduce the effective $R_{C_{IN}}$ and hence the ESR induced ripple.

- **Capacitor ripple current rating** – The ripple current, along with capacitor ESR, results in temperature rise inside the capacitor. Temperature rise with RMS ripple current is shown in Figure 7 **(**b) for CL31X226KAHN3NE. The temperature rise at the highest operating ambient should keep the capacitor temperature below its rated operating limits. Paralleling capacitors will divide the current and hence reduce the thermal stress on individual capacitors.

2.1.3 Buck stage output capacitor

The output capacitor is essential to keep the switching voltage ripple within a specified limit and to cater for load-transient response. The feedback control loop adjusts the output voltage for any load transients, but when load step/dump rate is faster than loop response time, the output capacitor has to ensure that output undershoot/overshoot is contained within the specified value.

To maintain the voltage ripple at switching frequency below a specified value (ΔV_O – typically less than 5 percent of output voltage), the minimum output capacitance required is:

$$C_{O1} = \frac{\Delta i_L}{8\ F_S\ \Delta V_O}$$

Output capacitance to meet the transient requirements is:

$$C_{O2} = \frac{I_{O_{Step}}}{V_{Odip}} \frac{1}{2\pi\ F_{BW}}$$

Where:

$I_{O_{Step}}$ is the load current step (worst case is 150 percent of full load current)

V_{Odip} is the allowed dip in output voltage for the load step

F_{BW} is the control loop bandwidth, which is set at less than 1/10 of the switching frequency

The output capacitance required is a maximum of C_{O1} and C_{O2}. The ripple current through the capacitor is the ripple content of inductor current. The RMS capacitor current is:

$$I_{CO_{rms}} = \frac{\Delta i_L}{2\sqrt{3}}$$

The loss in output capacitors is:

$$P_{Co} = \frac{{I_{CO_{rms}}}^2 R_C}{N_{cap}}$$

The capacitor part selection and bank sizing criteria are based on capacitance change with bias and temperature rise due to ripple current (as applicable for an input capacitor).

2.1.4 Power MOSFET selection for buck stage

The MOSFET selection depends on the worst-case operating conditions the converter operates at. The voltage rating should be at least 1.5 times the maximum operating voltage or slightly higher than peak withstanding voltage, whichever is higher. The peak current in the MOSFET is the same as the peak inductor current. The MOSFET current rating at the highest case temperature should be greater than the computed peak current.

$$V_{ds-pk} = \max\left((1.5V_{in-op}), V_{in-withstand}\right)$$

$$I_{ds-pk} = I_{Lpk} = (1.5 \text{ x } I_O) + \left(\frac{\Delta i_L}{2}\right)$$

Power loss is another key parameter for MOSFET part selection. The MOSFET characteristics such as on-state resistance, switching transition times, gate charge, package area, thermal impedance, etc. govern the MOSFET part selection.

2.1.4.1 Conduction loss

The current through the FETs is pulsating, as shown in Figure 6. The RMS current of the high-side or main MOSFET is derived from the current waveform as:

$$I_{Qrms_{HS}} = \sqrt{\frac{1}{T_S}\int_0^{T_S} i_{Q_{HS}}(t)^2\, dt}$$

$$I_{Qrms_{HS}} = \sqrt{\frac{1}{T_S}\int_0^{DT_S} \left(I_O - \frac{\Delta i_L}{2} + \frac{\Delta i_L\, t}{D\, Ts}\right)^2 dt}$$

$$I_{Qrms_{HS}} = \sqrt{D\left({I_O}^2 + \frac{{\Delta i_L}^2}{12}\right)}$$

When Q_HS is turned off, the inductor current freewheels through the diode of Q_LS. Synchronous rectification (SR) MOSFET Q_LS is turned on to give a low impedance path for freewheeling current and hence reduce conduction losses. The SR MOSFET RMS current is computed as:

$$I_{Qrms_{LS}} = \sqrt{\frac{1}{T_S}\int_0^{T_S} i_{Q_{LS}}(t)^2\, dt}$$

$$I_{Qrms_{LS}} = \sqrt{\frac{1}{T_S}\int_0^{(1-D)T_S} \left(I_O + \frac{\Delta i_L}{2} + \frac{\Delta i_L (t - DTs)}{(D-1)Ts}\right)^2 dt}$$

$$I_{Qrms_{LS}} = \sqrt{(1-D)\left({I_O}^2 + \frac{{\Delta i_L}^2}{12}\right)}$$

The conduction loss in the MOSFET occurs due to the on-state resistance $R_{ds(on)_{HS}}$ and $R_{ds(on)_{LS}}$. This resistance is a function of temperature, and the value at the highest operating temperature from the datasheet should be considered for the worst-case scenario. The conduction loss in FETs is computed as:

$$P_{C-Q_{HS}} = {I_{Qrms_{HS}}}^2 R_{ds(on)_{HS}}$$

$$P_{C-Q_{LS}} = {I_{Qrms_{HS}}}^2 R_{ds(on)_{LS}}$$

2.1.4.2 Dead time loss

A dead band is provided between the gate signals of high-side and low-side FETs, as in Figure 6. This dead band ensures that there is no cross-conduction between FETs, causing short of input supply. Also, when Q_HS is turned off, the energy in the inductor will discharge the C_{oss} of Q_LS and start body diode conduction of Q_LS within this dead band before the gate signal is applied. The conduction loss occurring in the body diode is:

$$P_{TD} = F_S V_F\left(\left(I_O + \frac{\Delta i_L}{2}\right)T_{DT1} + \left(I_O - \frac{\Delta i_L}{2}\right)T_{DT2}\right)$$

where:

V_F is the forward drop of body diode of the MOSFET.

T_{DT1} and T_{DT2} are the dead time at turn-off and turn-on of the Q_HS gate, respectively. If the dead times are set as identical at T_{DT}, then the dead time loss is:

$$P_{TD} = F_S\, V_F T_{DT}\, (2I_O)$$

2.1.4.3 Switching losses

High-side MOSFET switching losses

The high-side MOSFET has switching losses when the gate is toggled. The losses are dependent on the MOSFET parasitic capacitances and the gate resistance. Figure 8 shows typical MOSFET switching characteristics, and the region where switching losses occur are shaded in gray.

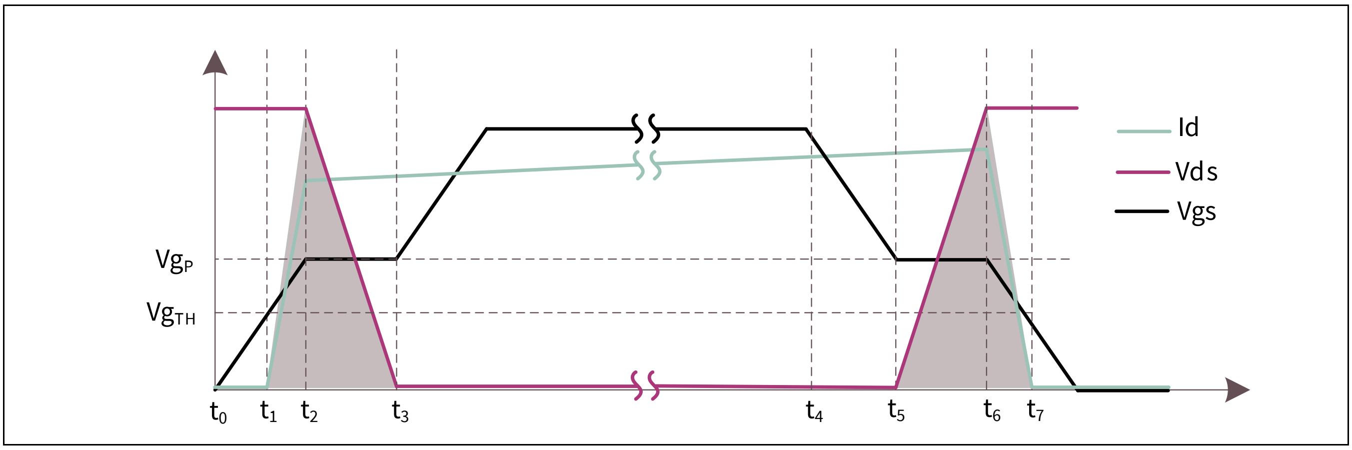


Figure 8 MOSFET turn-on and turn-off characteristics

The MOSFET turn-on loss is the shaded area between t_1 and t_3, and is given by:

$$P_{SW-ON} = \frac{1}{2} V_{IN} \left(I_O - \frac{\Delta i_L}{2}\right) t_{ON} F_S$$

$$t_{ON} = (t_2 - t_1) + (t_3 - t_2)$$

$$t_{ON} = \left(R_{GON} C_{iss} \ln\left(\frac{V_{dr} - V_{gth}}{V_{dr} - V_{gp}}\right)\right) + \left(\frac{R_{GON}}{V_{dr} - V_{gp}} V_{IN} C_{rss}\right)$$

where:

R_{GON} is the gate resistance for rising gate voltage (sum of MOSFET internal gate resistance, driver pull-up and external gate resistor)

C_{iss} and C_{rss} are MOSFET parasitic capacitors specified in the datasheet

V_{dr} is the gate driver supply voltage

V_{gth} and V_{gp} are MOSFET gate threshold and gate plateau voltage specified in the datasheet.

Similarly, the MOSFET turn-off loss is the shaded area between t_7 and t_5, and is given by:

$$P_{SW-OFF} = \frac{1}{2} V_{IN} \left(I_O + \frac{\Delta i_L}{2}\right) t_{OFF} F_S$$

$$t_{OFF} = (t_6 - t_5) + (t_7 - t_6)$$

$$t_{OFF} = \left(R_{GOFF} C_{iss} \frac{V_{gp}}{V_{gth}}\right) + \left(\frac{R_{GOFF}}{V_{gp}} V_{IN} C_{rss}\right)$$

In the switching loss equations, the V_{DS} rise and fall is assumed to be linear and constant C_{rss}, which is non-ideal as shown in Figure 9 for BSZ0910ND, and it is difficult to incorporate the non-linearity in computations.

One method to include non-linearity is to take the average of C_{rss} at turn-on and turn-off voltage [4].

$$C_{rss} = \frac{Cgd2 + Cgd1}{2} = \frac{C_{rss}@0V + C_{rss}@V_{IN}}{2}$$

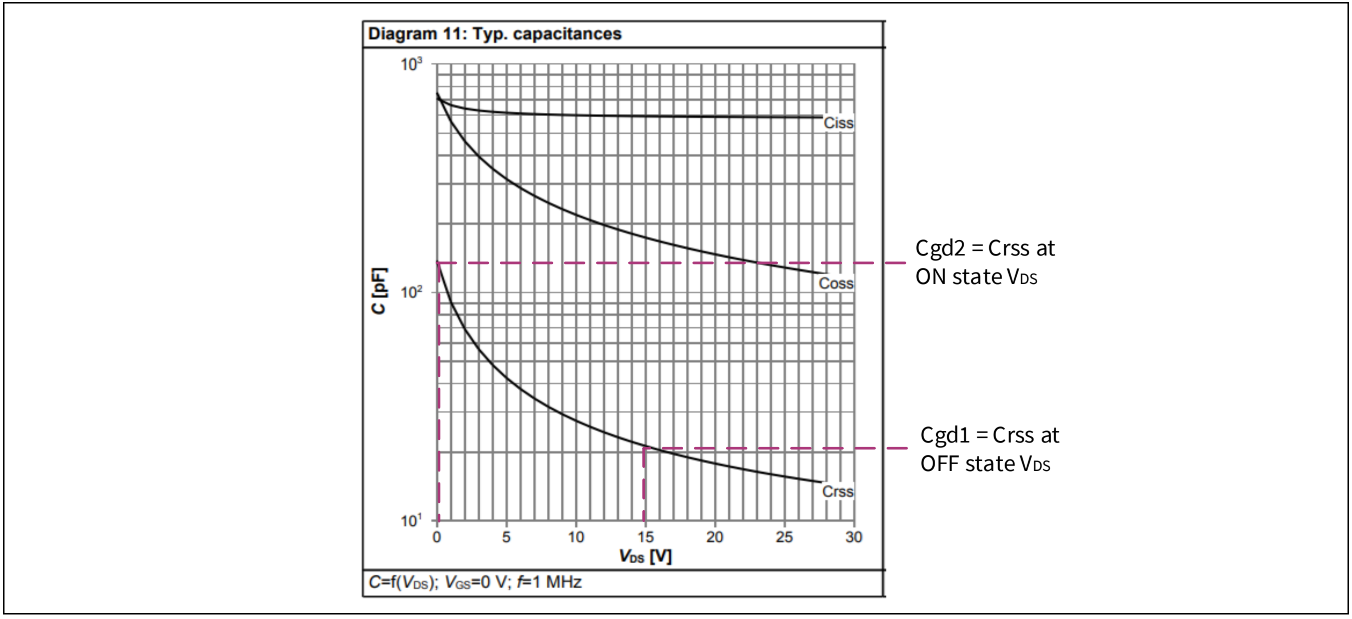


Figure 9 C_{rss} **variation with** V_{DS} **and identifying Cgd1 and Cgd2**

Reverse recovery losses

When the high-side MOSFET turns on, the reverse recovery phenomenon is seen in the body diode of the low-side MOSFET. The reverse recovery loss of the bottom-side MOSFET will occur in the high-side MOSFET and adds to the turn-on losses.

$$P_{DRR} = Q_{rr} V_{IN} F_S$$

Where Q_{rr} is the reverse recovery charge of the body diode of Q_LS and is provided in the datasheet. Q_{rr} is also a function of diode forward current and the current slope in the diode during turn-off [5].

Other switching losses

Furthermore, the high-side MOSFET output capacitance must be charged during switching, and the associated loss is:

$$P_{COSS} = \frac{1}{2} C_{oss} {V_{IN}}^2 F_S = \frac{1}{2} Q_{oss} V_{IN} F_S$$

where:

C_{oss} is the MOSFET output capacitance provided in the datasheet. Some manufacturers also provide the information as output charge Q_{oss}.

The steady-state MOSFET currents for a buck converter operating in FCCM are shown in Figure 10 for full-load and light-load conditions. When the inductor valley current is positive, which is typically case for inductance design for CCM, the high-side MOSFET will have a hard turn-on and turn-off switching. For FCCM operation at light loads, the Q_HS body diode conducts when Q_LS is turned off, and so turn-on of Q_HS is with zero voltage switching (ZVS). Also, when Q_LS is turned off, the current in Q_LS body diode is not interrupted and so there is no recovery loss.

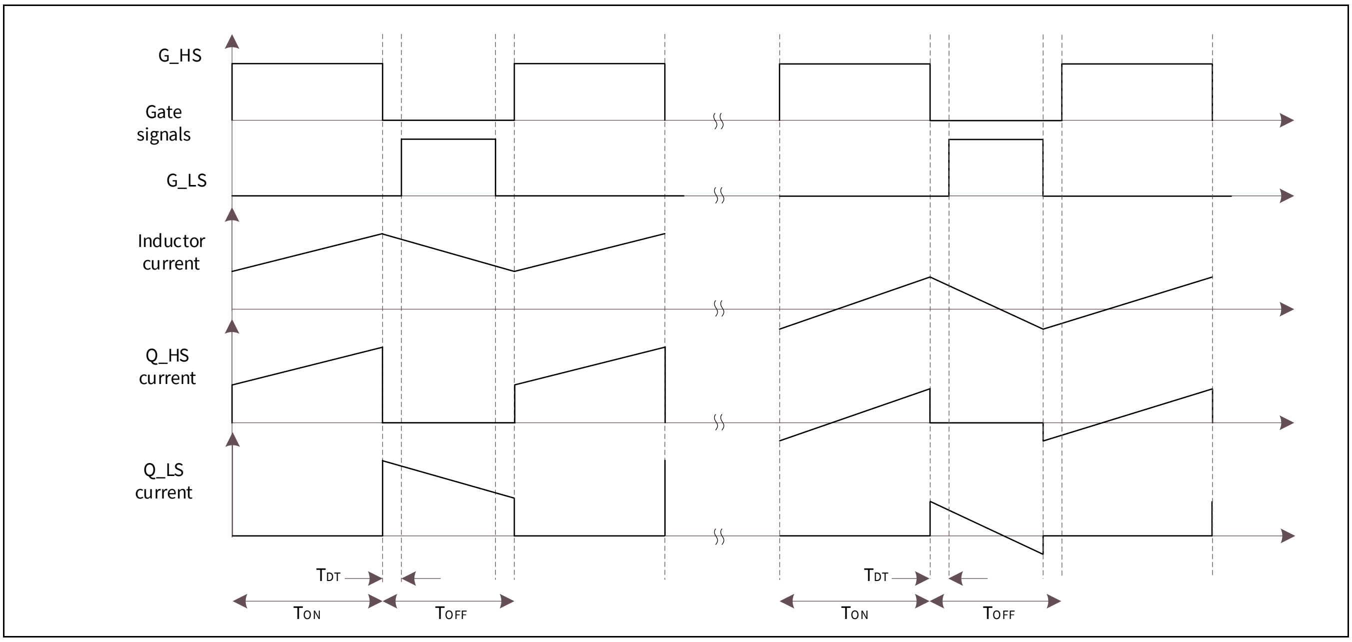


Figure 10 **MOSFET currents in FCCM operation: (a) full load; (b) light load**

Low-side MOSFET switching losses

As shown in Figure 10**,** the inductor current is always positive when Q_HS is turned off, which will forward bias the body diode of Q_LS before the gate of Q_LS is applied. Thus, Q_LS always turns on with ZVS. For CCM operation at full load, the Q_LS gate pulse is removed but the drain source voltage is still tied to the forward drop voltage of the body diode, resulting in nearly zero turn-off loss as well. There will be reverse recovery-related losses associated with Q_LS turn-off, but since the reverse current will be supplied by Q_HS, the corresponding losses appear in Q_HS in the form of higher turn-on losses.

When inductor valley current is negative, at light load or in the case of a large ripple, Q_LS will turn on with ZVS, but turn-off is hard with a loss:

$$P_{D-OFF} = \frac{1}{2}V_{IN}\left|I_O - \frac{\Delta i_L}{2}\right|t_{OFF}$$

2.1.4.4 Gate drive power

The gate charging and discharging consumes a certain amount of power, which is supplied from the gate driver supply. The gate power is a function of total gate charge and switching frequency:

$$P_{GATE} = Q_G V_{dr} F_S$$

where:

V_{dr} is the driver supply voltage

Q_G is the gate charge.

The value is available in the datasheet and must be selected for V_{dr} level.

MOSFET selection guidelines for buck stage

1. The selected part should be rated for V_{ds-pk} and I_{ds-pk} over the entire operating temperature range specified in the datasheet.
2. Select a part with low $R_{DS(on)}$ for lower conduction losses. For FCCM operation, there will be circulating current at light load, and low $R_{DS(on)}$ helps in reducing light power losses.
3. For Q_HS, low C_{rss} and C_{oss} parts will give low switching losses. For Q_LS, select the part whose body diode has low reverse recovery charge, preferably less than 5 nC.
4. The integrated gate drivers in WLC1115 drive the MOSFET gate with 5 V. The selected MOSFET part should be logic-level driven (should have the specified RDS(on) at gate voltage of 4.5 V).
5. WLC1115 has integrated gate resistance, the value of which can be firmware-configured to up to 33 Ω, and internal pull-down resistors. There is no need for external gate resistors.
6. MOSFETs with SMD package are preferred. Avoid using a through-hole part because the lead inductance will add to switching losses and emissions.
7. The MOSFET package should be such that the thermal management is manageable with natural cooling, without occupying much PCB area. Refer to section 4.4 for thermal management for MOSFETs.

2.1.5 Bootstrap circuit

The buck stage FETs are driven using inbuilt gate drivers of WLC1115. The high-side MOSFET requires a voltage supply referenced at the switching node or source of Q_HS. A bootstrap circuit built using C_{boot} and D_{boot} is used (refer to Figure 11) to generate the supply for Q_HS.

The C_{boot} must be able to supply a charge (= 2*gate charge) and retain its full voltage. If that does not happen, there will be a significant amount of ripple on the Q_HS gate drive supply.

$$C_{boot} \gg 20C_g$$

$$C_g = \frac{Q_g}{\mathrm{VDDD} - V_{F-Dboot}}$$

$\mathrm{VDDD} = V_{dr}$ is the supply voltage and is the same as the Q_LS gate drive supply.

Q_g is the gate charge of the MOSFET.

$V_{F-Dboot}$ is the forward drop of bootstrap diode D_{boot}.

The chosen bootstrap capacitor (C_{boot}) should be able to withstand switch node voltage (SW1_0) + VDDD.

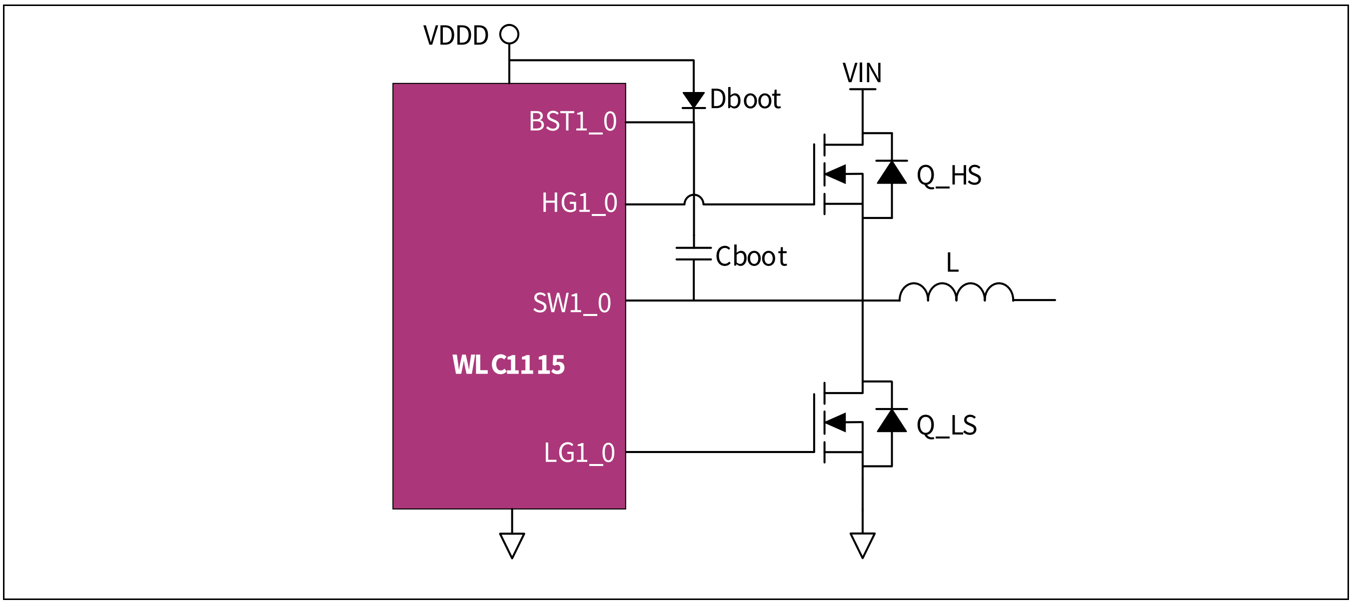


Figure 11 Bootstrap circuit

The bootstrap diode (D_{boot}) needs to be able to block the full-power rail voltage, which is seen when the high-side MOSFET (S1) is switched on. It must be a fast recovery diode to minimize the amount of charge fed back from the bootstrap capacitor (C_{boot}) into the VDDD supply, and similarly the high temperature reverse leakage current will be important if the capacitor must store charge for long periods of time. The current rating of the bootstrap diode is the average gate current:

$$I_{Dboot} = \frac{P_{GATE}}{\mathrm{VDDD}} = Q_G F_S$$

2.1.6 Current sense resistor selection

WLC1115 uses internal high-side current sense amplifiers (CSAs) for input current and load current. The input current feedback is mainly for PCMC and is not the same as the DC input current. The output current feedback in wireless charging is used for inverter power measurement for power loss calibration and FOD. The value of the external CS resistors is critical to the control of the buck converter and reliable FOD.

For the input CS resistor $R_{sh_{in}}$, WLC1115 requires a 5 mΩ CS resistor. For output CS resistor R_{sh_o}, WLC1115 requires a 10 mΩ CS resistor for a good sensing range and ADC resolution.

Sense resistor part selection

Sense resistor losses and ease of routing determine the selection of the resistor package. The resistor losses are:

$$P_{Rsh_{in}} = I_{Rsh_{in}}{}^2\, R_{sh_{in}}$$

$$I_{Rsh_{in}} = I_{Qrms_{HS}}$$

$$P_{Rsh_o} = I_{Rsh_o}{}^2\, R_{sh_o}$$

$$I_{Rsh_o} = I_O$$

For a 15 W design, the losses are 0.02 W and 0.06 W in input and output shunt resistors, respectively. Going by loss numbers, a resistor package of 0603 would be sufficient. But the feedback traces from the sense resistor should be taken as shown on the right-hand side of Figure 12. Considering the routing guidelines in 0 and associated creepage requirements between traces and pads, the 1206 package is most suitable for CS resistors.

Part	Res. Range	P	W	D
LVT04	R0025~R020	0.40mm	0.60mm	0.60mm
LVT06	R002	0.50mm	0.92mm	1.35mm
LVT06	R003~R020	0.60mm	0.92mm	1.30mm
LVT08	R002	0.50mm	1.44mm	1.55mm
LVT08	R003~R020	0.80mm	1.44mm	1.40mm
LVT12	R002	0.60mm	1.84mm	2.10mm
LVT12	R003~R020	1.20mm	1.84mm	1.80mm

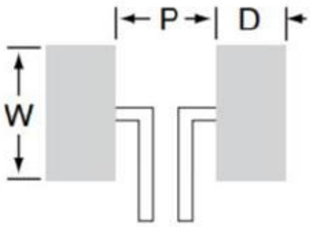


Figure 12 **Typical SMD resistor packages and land patterns**

2.1.7 Type 2 compensator for buck stage

For the MP-A11 coil-based wireless transmitter, WPC recommends control of DC voltage to inverter bridge to regulate the power delivered to receiver. The buck stage constant voltage (CV) feedback loop with an external compensation network regulates the buck output voltage with 20 mV step size for reference. The control-loop architecture for the buck stage is shown in Figure 13.

WLC1115 incorporates PCMC for the buck stage, using the output voltage and high-side MOSFET current feedback for CV mode operation. Slope compensation for PCMC is built into WLC1115 along with high-side CSAs and a voltage feedback network. A Type 2 compensation network for the loop is set using external components Rz, Cz and Cp. The choice of external compensation network components is based on cross-over frequency of control-loop bandwidth F_{BW}, buck converter plant transfer function (dependent on power stage components like inductance, output capacitance, ESR, etc.) and the transconductance amplifier gain g_m.

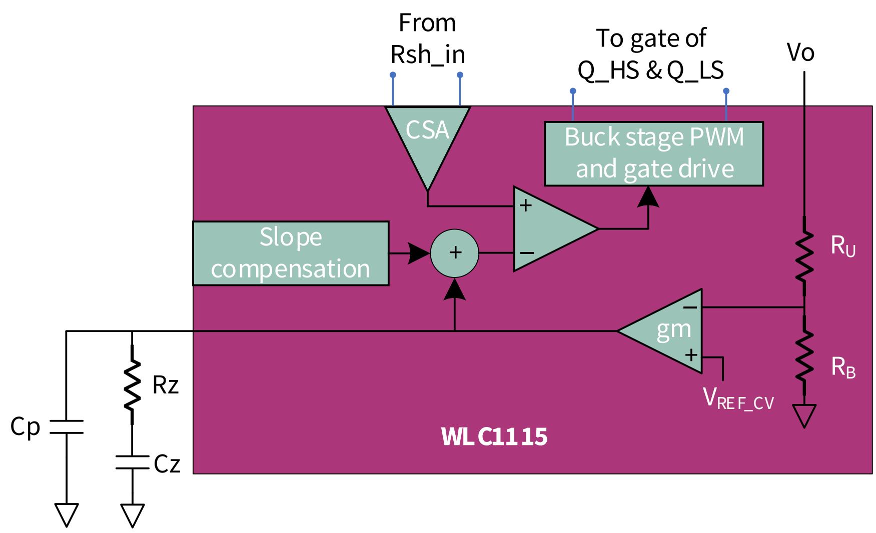


Figure 13 **Control-loop architecture for buck stage**

The plant transfer function for PCMC of the buck converter is given by:

$$G_{VC}(s) = \frac{k\ R_O}{R_i} \frac{(1 + sR_{CO}C_O)}{(1 + sR_O C_O k)} F_n(s)$$

$$k = \frac{1}{1 + \frac{T_S R_O}{L}(m_C(1 - D) - 0.5)}$$

$$m_C = 1 + \frac{S_e}{S_n}$$

$$F_n(s) = \frac{1}{1 + \left(\frac{s}{\omega_n}\right)^2 + \frac{s}{Q\omega_n}}; \qquad \omega_n = \pi F_S$$

where:

R_O is the load resistance (V_O/I_O)

R_i is the CS feedback gain – the product of shunt resistance value and CSA gain

R_{CO} is the equivalent ESR of the output capacitor

S_e is the external slope added for slope compensation (50 percent to 100 percent of $\frac{V_O}{L}$)

S_n is the input slope of the inductor current

The feedback network gain is:

$$G_{div}(s) = \frac{R_B}{R_B + R_U}$$

where $R_B = 34.5\ k\Omega$ and $R_U = 200\ k\Omega$ are the voltage feedback network divider resistors built into WLC1115.

The compensation networks transfer function is:

$$G_{EA}(s) = \frac{1}{sC_Z} \frac{(1 + sR_Z C_Z)}{(1 + sR_Z C_P)}$$

For the compensation network:

1. The crossover frequency F_{BW} is usually set at 1/10 of the switching frequency as a good balance between feedback noise and transient response.
2. The compensator zero is placed at the plant dominant pole.
3. The compensator pole is set to cancel the plant zero formed by the output capacitor and its ESR. The compensation network components are:

$$R_Z = \frac{2\pi(R_U + R_B)R_i C_O F_{BW}}{R_B g_m}$$

$$C_Z = \frac{R_O C_O}{R_Z}$$

$$C_P = \frac{R_{CO} C_O}{R_Z}$$

The open-loop transfer function of the converter with compensation is:

$$H_{OL}(s) = G_{VC}(s)\, G_{EA}(s)\, G_{div}(s)$$

The stability margins are evaluated by plotting the frequency response of the transfer function and determining the gain margin and phase margin. The frequency response for the 15 V input and the 9 V output at 15 W is shown in Figure 14, or the buck converter in REF_WLC_TX15W_C1. As the buck converter will operate for a large range of input and output voltages, stability at all operating points should be ensured.

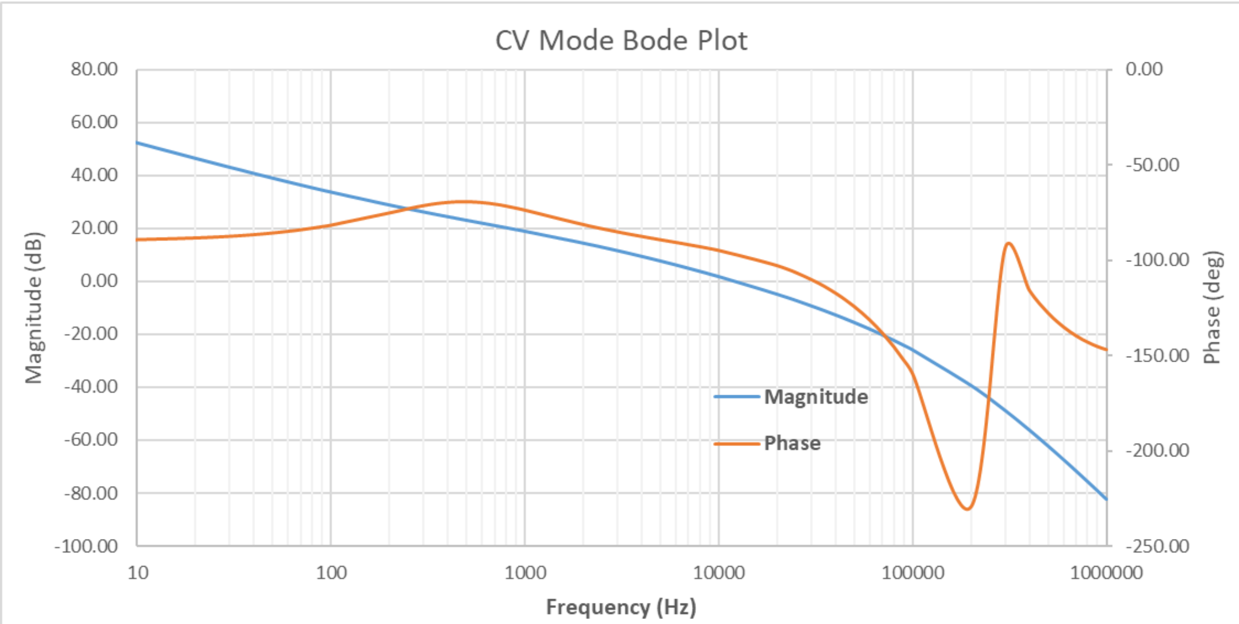


Figure 14 Stability plot for 15 V input, 9 V output and 15 W load in REF_WLC_TX15W_C1

2.2 Inverter power stage

The inverter stage in REF_WLC_TX15W_C1 is shown in Figure 15. The power stage consists of a filter capacitor at input, and a full-bridge inverter power stage feeding a resonant tank made up of transmitter coil and resonant capacitor. The input to the inverter is from the buck stage output after the buck output shunt resistor. The four MOSFETs form a full-bridge inverter as recommended for the MP-A11 coil. The snubber capacitors C_S on each switching node aid in reducing dV/dt during MOSFET turn-on/-off. With proper tuning of snubber capacitor and dead-time, the ZVS turn-on of FETs with minimal body diode conduction can be achieved.

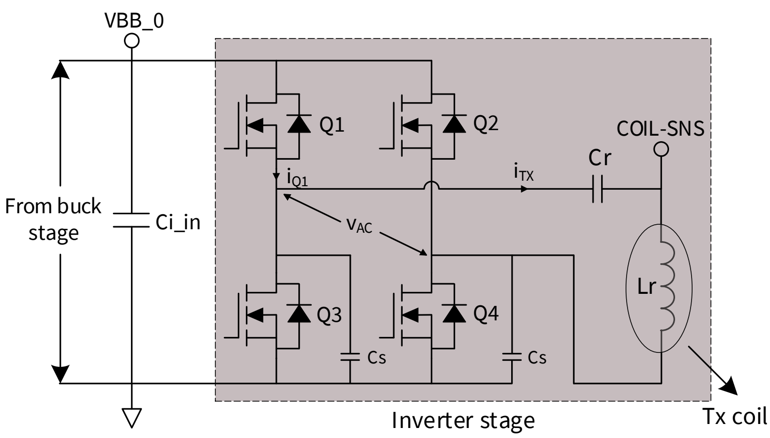


Figure 15 Inverter stage in REF_WLC_TX15W_C1

The steady-state waveforms for the inverter stage are shown in Figure 16. The waveforms represent the converter state in normal operating range, i.e., after the resonant peak in frequency characteristics. The impedance seen by the bridge is inductive and so the tank current i_{TX} is lagging behind the tank voltage V AC.

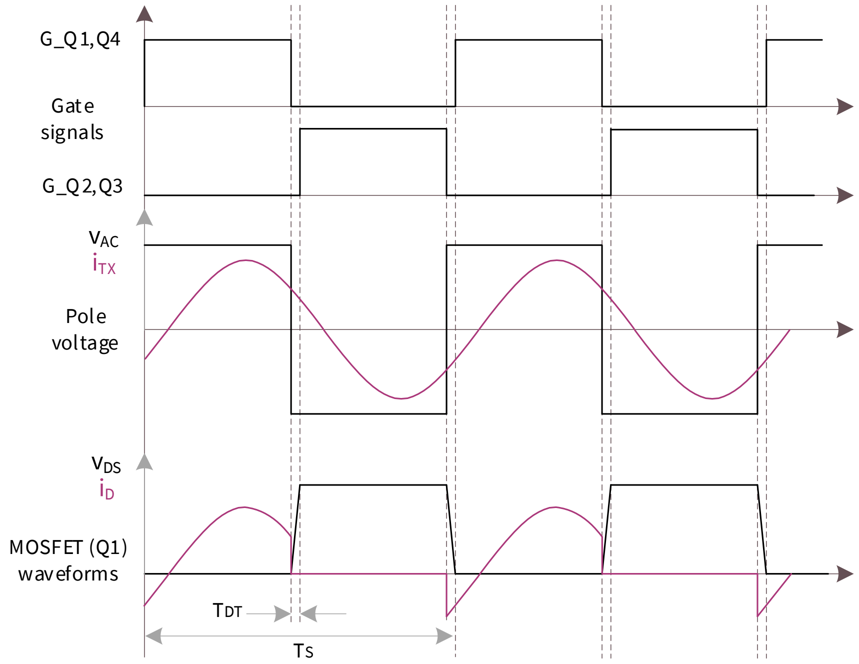


Figure 16 Inverter steady-state waveforms

2.2.1 Transmitter coil selection

The transmitter coil parameters (inductance, ferrite shield construction) for the MP-A11 coil are from the Qi specifications. The parameters for the MP-A11 coil from [1] are summarized in Table 2.

Table 2 MP-A11 transmitter coil parameters

Parameter	Value	Tolerance
Self-inductance	6.3 µH	± 10%
Coil outer diameter	44 mm	± 1.5 mm
Coil inner diameter	20.5 mm	± 0.5 mm
Number of turns	10	–
Number of layers	1 or 2	–
Ferrite shield thickness	0.5 mm	–
Coil to shield minimum gap	1 mm	–
Coil top surface to interface surface gap (dz)	3.5 mm	± 1 mm
Shield extension beyond coil	2 mm	–

While most of the parameters of the transmitter coil are already taken care of by the manufacturer, the dz gap must be set using the right combinations of spacers and acrylic. The coil assembly used in REF_WLC_TX15W_C1 is shown in Figure 17. The coil assembly is mounted on the coil PCB using double-sided tape. The interface surface is an acrylic sheet, and the gap between the sheet and coil is set using four nylon spacers. The spacer height is selected so that the dz gap is close to the Qi-recommended nominal value.

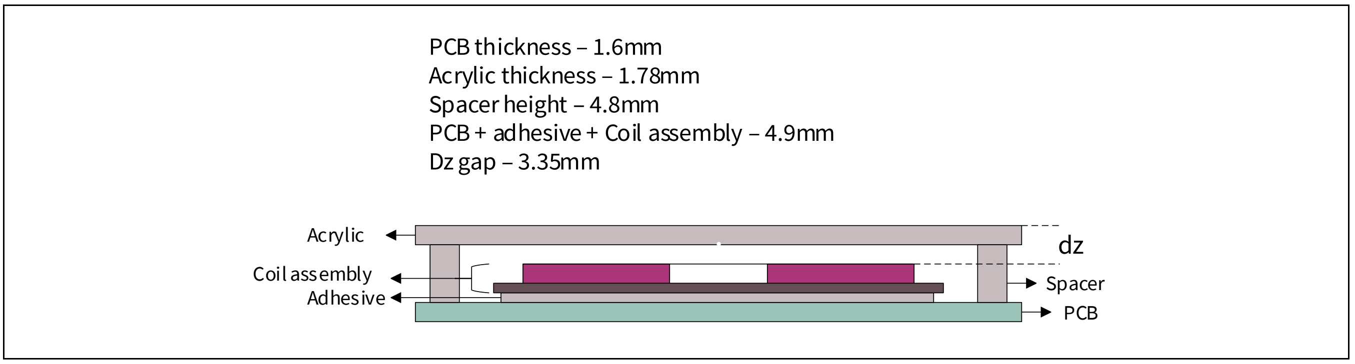


Figure 17 MP-A11 coil assembly and associated measurements in REF_WLC_TX15W_C1

Transmitter coil losses

The coil losses consist of conduction losses in windings and core losses in the ferrite shield. For conduction losses, the coil resistance, both DC resistance and skin-effect induced AC resistance, come into the picture. To precisely predict conduction losses, use the Q factor curve provided by the manufacturer and compute the total resistance at the operating frequency. Alternatively, use an impedance analyzer to obtain the total coil resistance at operating frequency (Figure 18).

$$P_{coil-cond} = I_{TXrms}{}^{2} R_{total}$$

$$R_{total} = \frac{Q_{Fs-inv}}{2\pi F_{Sinv}\ L_{tx}}$$

where I_{TXrms} is coil RMS current and R_{total} is the sum of AC and DC resistance of the coil.

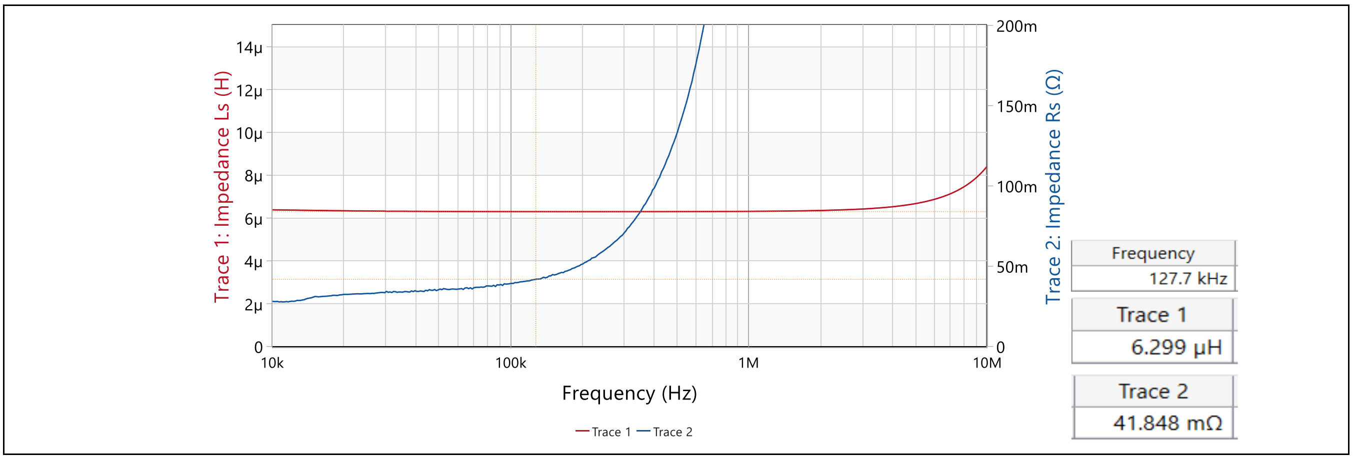


Figure 18 Impedance measurements on MP-A11 coil used in REF_WLC_TX15W_C1

Qi recommends use of a Ni-Zn or Mn-Zn ferrite core for shielding of the coil. The ferrite core will have alternating magnetization, resulting in core losses. The core loss computation is similar to that of the buck inductor:

$$P_{Core} = C F_{S-inv}{}^{\alpha} B_{pk}{}^{\beta} V_e$$

$$B_{pk} = \frac{L_r\, I_{TXpk}}{N\, A_C}$$

where the constants C, α and β are specified by the manufacturer:

V_e is the core material volume

B_{pk} is the peak flux in the core

A_C is the core cross-section area (product of the ferrite width and thickness).

Transmitter coil part selection guidelines

- The selected part should match the Qi requirements for the MP-A11 coil (electrical design, ferrite shield design, etc.).
- Inductance value tolerance should not be more than ±10 percent.
- A high Q-factor coil (low total resistance for the 120 kHz to 130 kHz range) is favorable for low losses.

2.2.2 Resonant capacitor selection

The Qi-recommended resonant capacitor value to be used with the MP-A11 coil is 500 nF ±5 percent. As the capacitance value should not vary throughout the operating frequency and voltage range, a capacitor with C0G-type dielectric should be used. Another criterion for capacitor bank sizing is the RMS current rating. The capacitor bank RMS current rating should not result in temperature rise beyond the capacitor rating.

The voltage rating of the resonant capacitor must ensure failsafe operation for all phases in the Qi state machine. During power transfer, the capacitor voltage is low (less than 25 V for 15 W with WRM483265-10F5-12V-G). However, sudden change in coupling when delivering power to load can momentarily increase the load voltage, tank current and hence the capacitor voltage. Though the control loop will eventually bring down the current, the capacitor should not fail for this momentary rise in voltage.

Another scenario to be considered is the capacitor voltage during selection or analog ping. In the selection phase, the tank is excited with pulses at a frequency close to resonant frequency. Though the excitation is of short duration (to ensure the receiver doesn’t wake up), the impedance seen by the tank is only coil resistance and capacitor ESR, which could take capacitor voltage to a high value for a short duration. To prevent capacitor failure from voltage stress, the voltage rating should be 100 V. This is in line with data in the Qi specification, where the capacitor voltage is predicted to reach 200 V pk-pk.

The loss in resonant capacitor or capacitor bank is from capacitor ESR:

$$P_{Cr} = I_{TXrms}{}^2 \frac{R_{Cr}}{N_{Cr}}$$

Where R_{Cr} is the ESR of the individual capacitor and N_{Cr} is the number of capacitors in the bank.

2.2.3 MOSFET selection for inverter stage

The MOSFET voltage rating should be higher than the maximum output of the buck stage output, which includes the buck output OVP level. The current rating should be greater than the peak transmitter coil current value. The MOSFET current rating at the highest case temperature rating should be considered for reliable operation.

$$V_{ds-pk} = \max\left(\left(1.5 \text{ x } V_{O,buck}\right), \text{Buck OVP level}\right)$$

$$I_{ds-pk} = I_{TX-pk}$$

Power loss in the MOSFET is another key parameter that governs the MOSFET part selection. As shown in Figure 16**,** the MOSFET current is negative during turn-on before applying gate pulse resulting in ZVS turn-on.

However, the MOSFET turn-off is hard, and is the dominant switching loss. Also, each MOSFET conducts for half of the switching period, based on which the MOSFET parameters for losses are as follows:

$$I_{Qrms} = \frac{I_{TX-pk}}{2}$$

$$P_{cond} = I_{Qrms}{}^{2} R_{ds(on)}$$

$$P_{SW} = P_{SW-OFF} = \frac{1}{2} V_{O,buck}\, I_{SW,off}\, t_{OFF}\, F_{S-inv}$$

The t_{OFF} computation method remains the same as for the buck converter in section 2.1.4.3. The turn-off current $I_{SW,off}$ is the coil current at the instant when the bridge voltage changes polarity. Refer to Figure 19 for identification of MOSFET currents during turn-on and turn-off from the coil current. The current can be predicted from the model using the tank current magnitude and impedance angle.

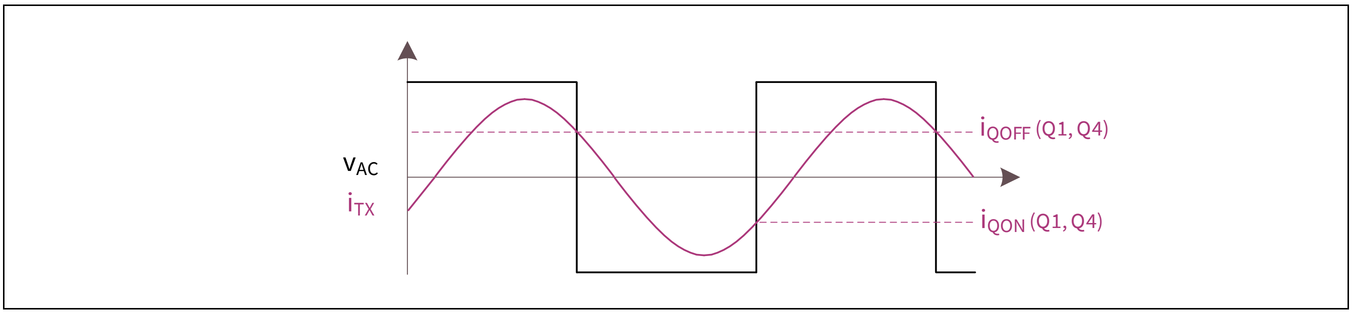


Figure 19 Identifying MOSFET turn-on and turn-off from coil voltage and current waveforms

The turn-on switching losses and C_{OSS} losses are zero due to ZVS action. The time taken to discharge the MOSFET C_{OSS} depends on the transmitter coil current magnitude at the instant of turn-off of the complementary MOSFET. The dV/dt will be dependent on turn-off current and C_{OSS} value.

$$\frac{dV}{dt} = \frac{I_{SW,off}}{C_{OSS}}$$

When the dead time is fixed, the $I_{SW,off}$ quickly discharges the device C_{OSS} capacitance and the MOSFET body diode conduction starts. The MOSFET is turned on with ZVS when the gate signal is applied. The dead time between gate signals should be large enough to ensure that the drain voltage has discharged C_{OSS} completely and initiate the body diode conduction.

If the settable dead time is high relative to dV/dt, there will be a period where the body diode conducts for a short duration. There is a dead time loss in four MOSFETs, and for power levels like 15 W, the dead time loss has an impact on efficiency. A snubber capacitor (C_S) in parallel with one half-bridge device will slow down the dV/dt and ensure minimal body diode conduction, as illustrated in Figure 20.

The introduction of C_S has two advantages. It slows down the dV/dt of MOSFETs thereby reducing emissions, and ensures minimal body diode conduction period for good efficiency.

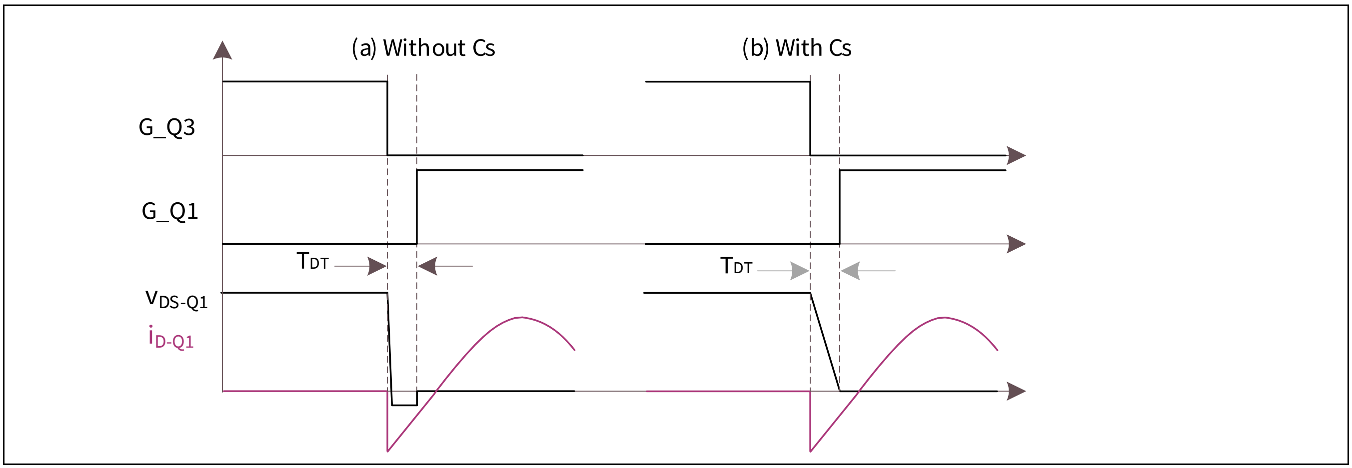


Figure 20 Impact of snubber capacitor (C_S) on switching performance

The snubber capacitor value is computed so as to bring the switch voltage to zero within the minimum settable dead time for the maximum turn-off current magnitude.

$$C_S = \frac{I_{SW,off-max}\,T_{DT}}{V_{O,buck}}$$

Gate drive power

The gate charging and discharging consumes a certain amount of power, which is supplied from the gate driver supply. The gate power is a function of total gate charge and switching frequency:

$$P_{GATE} = Q_G V_{dr} F_S$$

Where:

V_{dr} is the driver supply voltage

Q_G is the gate charge.

The value is available in the datasheet and must be selected for the V_{dr} level.

2.2.4 Decoupling capacitors

The buck output capacitors are the main DC-link capacitors for the inverter stage. In addition, there are bulk capacitors after buck output CS resistors, and high-frequency noise decoupling capacitors close to the inverter bridge.

The bulk capacitors ensure that the reactive current in the inverter bridge is contained within the inverter stage and is not seen by the buck output capacitors. In this way, the buck output CS resistor sees only the active current drawn by the inverter.

2.3 Control section

WLC1115 in wireless transmitter application for MP-A11 requires minimum external circuitry. In the control section, signal conditioning circuits are required for Q factor estimation and the ASK demodulator along with coil temperature measurement. The WLC1115 requires a standard decoupling capacitor network and bootstrap circuit components to drive the power stage.

2.3.1 Q factor estimation with WLC1115

WLC1115 uses the coil voltage information to compute the coil Q factor. The presence of Rx or FO or a combination of both before power transfer is reflected in the form of lower Q factor and change in resonance frequency. The primary resonant tank is excited with few pulses and the Q factor and resonant frequency are estimated using the decaying coil voltage waveform, as shown in Figure 21. The coil voltage after excitation decays more slowly in the case of no Rx than in the case of Rx or FO present on the interface surface.

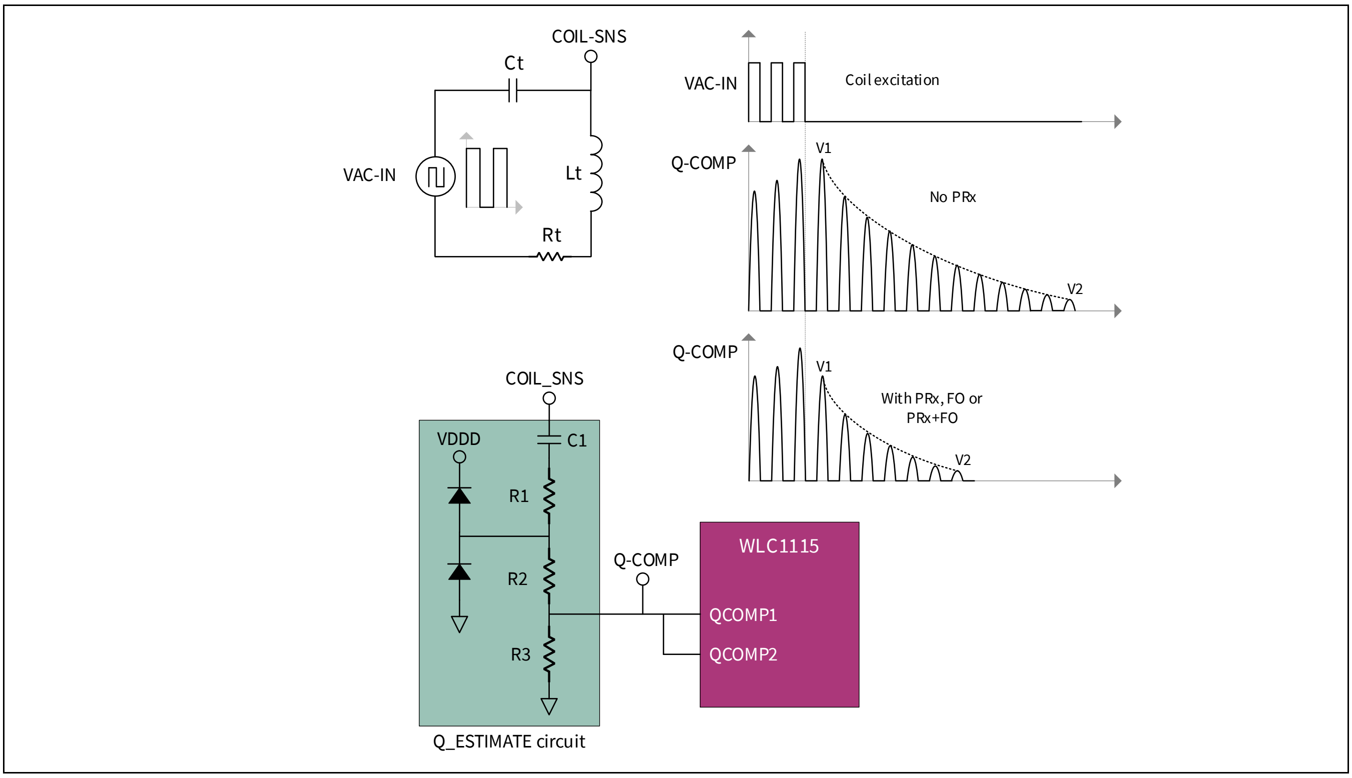


Figure 21 Q factor estimation using WLC1115

The Q factor is calculated from the decaying voltage waveform as:

$$Q = \frac{\pi\,(t_2 - t_1)\,F_r}{\ln\left(\frac{V_1}{V_2}\right)} = \frac{\pi\,N}{\ln\left(\frac{V_1}{V_2}\right)}$$

N is the number of cycles of the decaying waveform between intervals t_1 and t_2, where V_1 and V_2 are captured and F_r is the resonant frequency of the primary tank under the influence of the receiver or FO, or both.

The Q factor estimation performed by WLC1115 uses the coil voltage and two comparators. The ZCD comparator produces toggles that are used for resonant frequency calculation.

Refer to the REF_WLC_TX15W_C1 schematics for the Q factor estimation circuit recommended to use with WLC1115. The selection criteria for the components of the Q factor estimation circuit in REF_WLC_TX15W_C1 are as follows:

1. The clamping diodes should be of low leakage and low forward drop type. The leakage current of less than 100 nA at the highest operating ambient temperature is ideal. Standard recovery-type diodes rated for more than 100 V suit the application.
2. The diode clamping clamps the entire negative half of the coil voltage. The clamping current flows through the diode and R1. Set R1 to have less than 1 mA at the highest operating coil voltage for a low-loss circuit.

3. The WLC1115 has an internal pull-down resistor that is disabled only during analog ping and enabled for the rest of the duration.
4. R3 value should be approximately half of (R1 + R2).
5. R2 value should be slightly lower than (R3 || R_D).
6. C1 along with R1, R2 and (R3||R_D) forms a high-pass filter. Filter bandwidth should be less than the natural resonant frequency.

2.3.2 ASK demodulator

The ASK demodulator circuit makes use of coil voltage and inverter bridge input current (or buck output current) to demodulate the data from receiver. The bridge input current feedback is routed to WLC1115 for current measurement. The information from the coil voltage, taken to WLC1115, is derived through some signal conditioning. The demodulated information from both paths is processed through a gain stage followed by a comparator to generate digital data. The configuration used in REF_WLC_TX15W_C1 is shown in Figure 22.

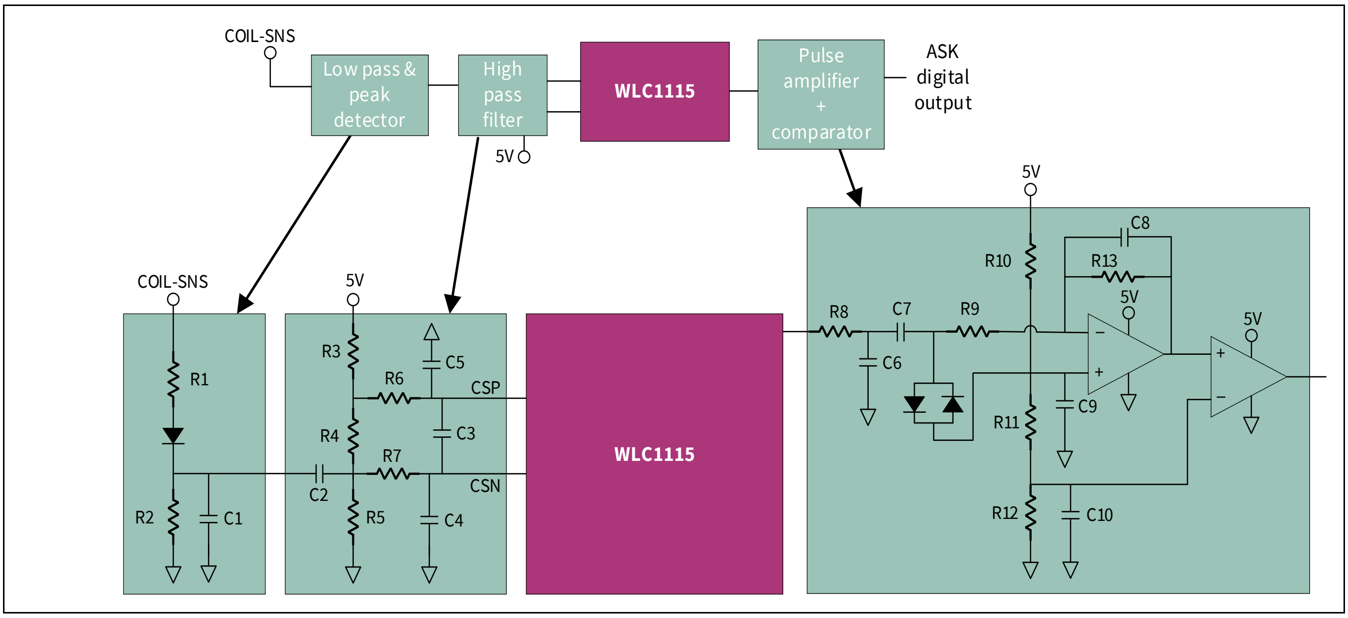


Figure 22 ASK demodulator circuit using WLC1115

The component values are tuned with the following considerations for the REF_WLC_TX15W_C1 and are recommended to use with WLC1115:

- Front-end low-pass filter and peak detector
  - The negative blocking diode should be rated for the same voltage as the capacitor voltage rating; also, the diode should be of the fast recovery type
  - The peak charge hold capacitor should also be rated for 100 V
- High-pass filter
  - The DC blocking capacitor C2 forms a high-pass filter with R5||(R4+R3), and the filter bandwidth should be much lower than the ASK communication rate (2 kHz)
  - Resistor ladder R3, R4 and R5 are selected to ensure >3 V at the CSP and CSN pins
  - The differential voltage across R4 should be greater than 5 mV and less than 50mV
  - The differential filter formed by (R6 + R7) and C3 should have a bandwidth lower than the switching frequency

- WLC1115 gain settings
  - For bridge current, the gain is set at 40
  - For voltage path, gain options range from 40 to 110; set the gain such that the input to amplifier stage is at (VDDD/2) which gives enough headroom for ASK-related swing
- Pulse amplifier and comparator stage
  - R8 and C6 forms a low-pass filter; the bandwidth should be less than inverter switching frequency but greater than ASK communication frequency
  - Amplifier gain is set by R9 and R13
  - Offset to the gain output is set across C9 using R10, R11 and R12; the offset value should be well within the common mode range of the op-amp
  - The reference to comparator across C10 is also set using R10, R11 and R12; the reference should be slightly lower than the offset added to the gain stage output, which reduces toggles in comparator output when there is no modulation happening for ASK

2.3.3 WLC1115-related circuitry

The WLC1115 is a highly integrated controller with inbuilt peripheral and programming flexibility to implement Qi wireless power transmitter design along with USB-PD compatibility. The controller also has an inbuilt low-dropout (LDO) regulator to generate the logic supply (VDDD) and core supply (VCCD), eliminating the need for an auxiliary power supply unit.

Detailed pin descriptions and external requirements for each pin are listed in the datasheet [2].

2.3.4 NTC feedback

The NTC monitors the transmitter unit temperature and is placed close to the coil. The NTC, when mounted on the interface surface, can be used to detect temperature rise in the interface surface from the heat radiated from the FO. The NTC feedback interface to WLC1115 ADC is a simple divider network with a filter, as shown in Figure 23**.** The NTC resistance is a function of temperature, and the accurate NTC resistance temperature characteristics are provided by the manufacturer (the characteristics can also be generated from NTC parameters, but the manufacturer-provided values account for non-linearities). The feedback to WLC1115 for the REF_WLC_TX15W_C1 is shown in Figure 23**.**

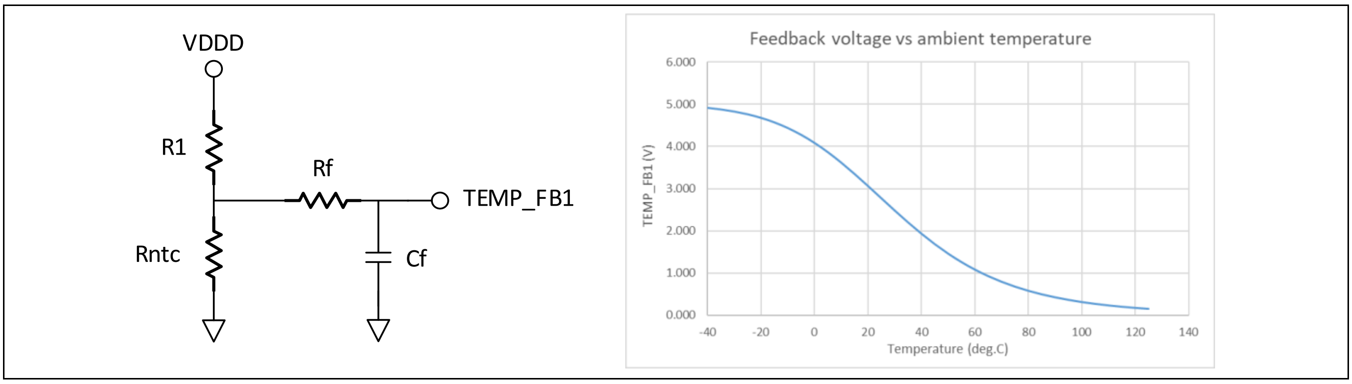


Figure 23 NTC interface to WLC1115 and NTC feedback value with temperature for REF_WLC_TX15W_C1

Design considerations:

1. The series resistor should ensure that the current in NTC at any temperature doesn't lead to a power loss greater than NTC specified value
2. The low-pass filter in the feedback path should have bandwidth low enough to discard the switching noise and ASK modulator frequency
3. Good resolution in feedback around required trip and recovery points

2.3.5 System configuration for PD sink compliance

WLC1115 has an integrated USB Type-C PD controller and complies to the latest USB Type-C and PD specifications. The bulk capacitance between the USB input (also referred to as VBUS) and ground result in large inrush current. The USB-PD specifications mandate the sink to limit the input inrush current at attach. To comply with the inrush current requirements of the transmitter unit, WLC1115 has an integrated high voltage gate driver to drive a consumer NFET on VBUS. The gate driver has a slow turn-on feature, which can be used to avoid a sudden inrush of current.

Select a low $R_{DS(on)}$ MOSFET for low conduction losses. This MOSFET works as a load switch and will not have any switching losses. Use the NFET_CTRL_1 pin of WLC1115 (pin 35) to drive the consumer NFET.

2.3.6 Other circuits

The authentication requirements for Qi v1.3.2 is realized using a security controller from Infineon. The OPTIGA™ Trust comes with full system integration for simple and cost-effective deployment of authentication. The OPTIGA™ Trust (U2) interface with WLC1115 is through I²C protocol (Figure 24**)** along with a control line for OPTIGA™ chip reset. The SCL and SDA have pull-up resistors for the I²C lines.

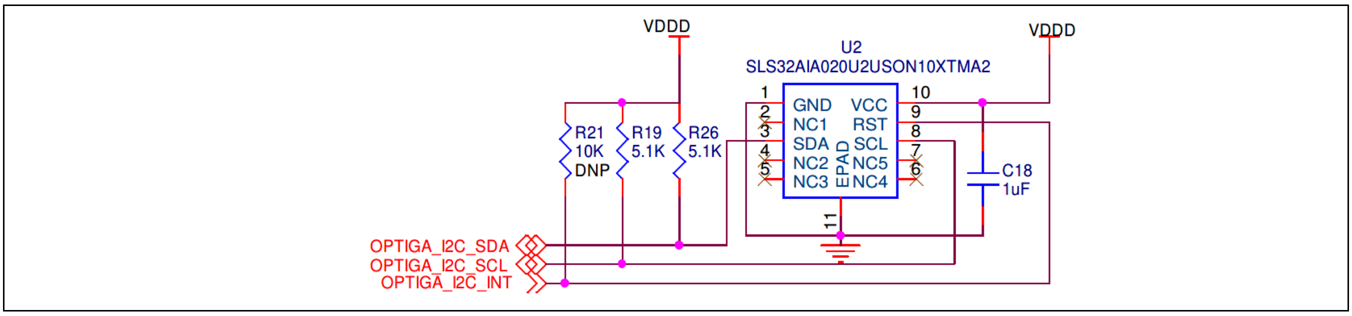


Figure 24 Authentication IC interface

WLC1115 has an internal oscillator whose tolerance meets the Qi requirements for FSK. An optional external oscillator (for more accurate clock or any proprietary FSK implementation) can be interfaced to WLC1115 through pin 60. The oscillator needs to operate at VDDD level and should be placed close to WLC1115. To reduce standby power, the bias to the oscillator can be disconnected through Q1, which is driven directly by WLC1115.

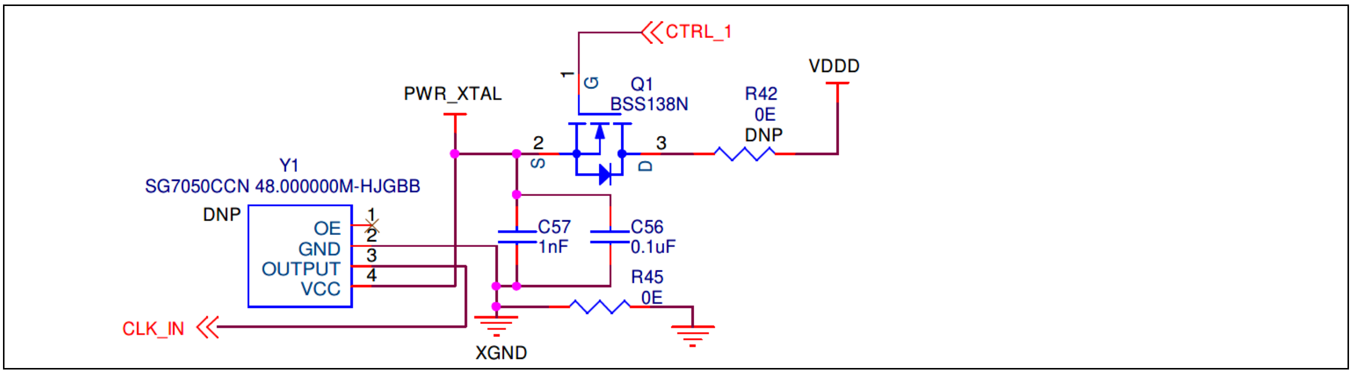


Figure 25 External oscillator interface (optional)

3 Design example – 15 W transmitter board

This section presents a design example for the 15 W wireless charger transmitter board, the specifications of which match the REF_WLC_TX15W_C1. The design example assumes buck stage operation with variable input control. The input voltage is configurable to three voltages on buck output voltage reference. The behavior is captured in Figure 26.

The key specifications of the power stage are as follows:

- Input voltage: 9 V, 15 V or 20 V during PD; 5 V during ping stage
- Buck stage output voltage: Up to 18 V
- Receiver output power: Maximum 15 W
- Buck stage switching frequency: 400 kHz
- Inverter stage switching frequency: 127.7 kHz

Design parameters

- Buck inductor ripple current: 1.5 A peak to peak
- Overload factor: 150 percent
- Input voltage ripple: 1 percent
- Buck output voltage ripple: 2 percent
- Allowed dip in buck output voltage: 5 percent of output
- Buck control-loop bandwidth: 25 kHz

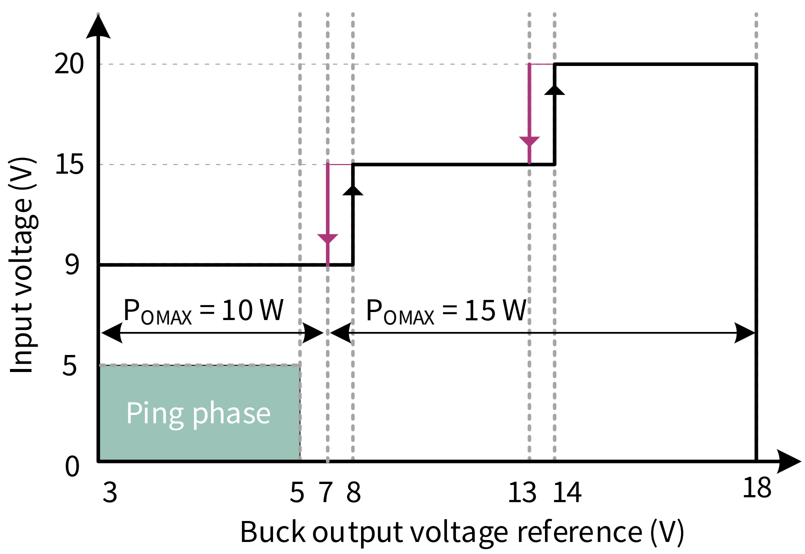


Figure 26 Variable PD input scheme for the buck stage

The buck power stage components calculation is listed in Table 3. Based on the computed values, the BOM for key components is listed in Table 6**.** For the Q factor estimation and ASK demodulator circuit, refer to the component values from REF_WLC_TX15W_C1 schematics in [3].

Table 3 Buck and inverter power stage component calculation

Parameter	Formula	Calculated value	Remarks
Inductance value	$L = \frac{V_{in} D(1-D)}{F_S \Delta i_L}$	7.58 µH for 20 V input	Maximum inductance value across the operating points
Inductor current	$I_{Lrms} = \sqrt{{I_O}^2 + \left(\frac{\Delta i_L}{2\sqrt{3}}\right)^2}$ $I_{Lpk} = (1.5 \text{ x } I_O) + \frac{\Delta i_L}{2}$	$\boldsymbol{I_{Lrms} = 2.51\ A}$ $\boldsymbol{I_{Lpk} = 4.12\ A}$	The currents are for 6.8 µH standard inductance value and maximum value across the working conditions
Input capacitor	$C_{IN} > \frac{I_{IN}(1-D)}{\Delta V_{in}\ F_S}$ $I_{CIN_{rms}} = \sqrt{D\left({I_O}^2(1-D) + \frac{{\Delta i_L}^2}{12}\right)}$	15.43 µF for 9 V input 8.89 µF for 15 V input 3.28 µF for 20 V input $\boldsymbol{I_{CIN_{rms}} = 1.19\ A}$	$\boldsymbol{C_{IN}}$ computed for$\boldsymbol{\Delta V_{in}}$ of 1 percent of $\boldsymbol{V_{in}}$ Ripple current is the maximum across the operating points
Output capacitor	$C_{O1} = \frac{\Delta i_L}{8\ F_S\ \Delta V_O}$ $C_{O2} = \frac{I_{O_{Step}}}{V_{Odip}} \frac{1}{2\pi\ F_{BW}}$ $C_O = \max(C_{O1}, C_{O2})$ $I_{CO_{rms}} = \frac{\Delta i_L}{2\sqrt{3}}$	C_O values 53.05 µF for 6 V output 15.92 µF for 12 V output 9.55 µF for 15 V output 7.96 µF for 18 V output $\boldsymbol{I_{CO_{rms}} = 0.48\ A}$	$\boldsymbol{C_{O1}}$ computed for $\boldsymbol{\Delta V_O =}$ 2 percent of $\boldsymbol{V_O}$ $\boldsymbol{C_{O2}}$ values computed for $\boldsymbol{F_{BW}}$ of 25 kHz, $\boldsymbol{V_{Odip} = 5\ percent}$ of V_{OUT} and $\boldsymbol{I_{O_{Step}} = 1.5 \text{ x } I_O}$ Ripple current is the maximum across the operating points
Buck stage MOSFETs	$V_{dspk} = \max\left((1.5V_{in-op}), V_{in-withstand}\right)$ $I_{ds-pk} = I_{Lpk} = (1.5 \text{ x } I_O) + \left(\frac{\Delta i_L}{2}\right)$	$V_{dspk} = 30\ V$ $I_{dspk} = 4.12\ A$	Values are the worst-case across the operating points
Input CS shunt	$R_{sh_{in}} = 0.005\Omega$ $P_{Rsh_{in}} = {I_{Qrms_{HS}}}^2\ R_{sh_{in}}$	$P_{Rsh_{in}} = 0.021\ W$	Shunt value as per WLC1115 requirement Computed loss is the worst-case value across the operating points
Output CS shunt	$R_{sh_o} = 0.010\Omega$ $P_{Rsh_o} = {I_O}^2\ R_{sh_o}$	$P_{Rsh_o} = 0.063\ W$	
Transmitter coil	$L_{tx} = 6.3uH$	$I_{TXrms} = 3.66$ A	Inductance and capacitance values as per Qi standard [1] Values based on actual measurements from three test receivers
Resonant cap	$C_r = 500nF$	$I_{Cr,rms} = 3.66$ A	
Inverter stage MOSFETs	$V_{ds-pk} = \max\left((1.5 \text{ x } V_{O,buck}), \text{Buck OVP}\right)$ $I_{ds-pk} = I_{TX-pk}$	$V_{ds-pk} = 27$ V $I_{ds-pk} = 5.45\ A$	Values based on actual measurements from three test receivers
Snubber capacitors	$C_S = \frac{I_{SW,off-max}\ T_{DT}}{V_{O,buck}}$	$C_S = 10.8\ nF$	Maximum value from data of three receivers

Table 3 sets out the values and requirements for the power stage components. The selection of parts depends on factors such as performance, losses, cost, etc., and might also need a few iterations. As an example, part selection for buck stage input capacitor and buck stage MOSFETs is shown in Table 4 and Table 5**,** respectively. Based on a similar approach for other components, a high-level BOM for the design example is captured in Table 6.

Table 4 Part selection example – buck stage input capacitor

Capacitor requirements	Voltage rating – 25 V or above Capacitance value and ripple current rating as in Table 3.
Option 1	CL31X106KAHNNNE Rating – 10 µF 25 V Number of capacitors required – **5** (to meet C_{IN} and $I_{CIN_{rms}}$ across the operating points) Capacitor bank capacitance value – 22.02 µF at 9 V, 10.61 µF at 15 V and 8.77 µF at 20 V input capacitor bank ripple current rating – 11.9 A_{RMS} for 10°C temperature rise
Option 2	CL31X226KAHN3NE Rating – 22 µF 25 V Number of capacitors required – **2** (to meet C_{IN} and $I_{CIN_{rms}}$ across the operating points) Capacitor bank capacitance value – 20.45 µF at 9 V, 10.49 µF at 15 V and 8.09 µF at 20 V input Capacitor bank ripple current rating – 5.6 A_{RMS} for 10°C temperature rise
Selected part	CL31X226KAHN3NE – considering the part count and associated impact on cost and area occupied in PCB

Table 5 Part selection example – buck stage MOSFETs

MOSFET requirements	Voltage rating – 30 V Current rating – 4.12 A
Option 1	BSZ0910LSATMA1 Rating – 30 V, 40 A, 5.7 mΩ Power loss (from equations in sections 2.1.4.1 to 2.1.4.4) for 15 V input 7 V output 15 W load on buck converter Q_HS losses – 165 mW (inclusive of conduction, switching and recovery), 17 mW gate drive Q_LS losses – 38 mW (inclusive of conduction, switching and dead time losses) 17 mW gate drive
Option 2	ISZ065N03L5S Rating – 30 V, 40 A, 8.6 mΩ Power loss (from equations in sections 2.1.4.1 to 2.1.4.4) for 15 V input 7 V output 15 W load on buck converter Q_HS losses – 174 mW (inclusive of conduction, switching and recovery), 10 mW gate drive Q_LS losses – 54 mW (inclusive of conduction, switching and dead time losses) 10 mW gate drive
Selected part	BSZ0910LSATMA1 – considering the losses, which is a key aspect of buck stage

Table 6 Key components BOM for the design example

Function	Qty	Description	Part number	Manufacturer
Wireless controller	1	Wireless transmitter with integrated USB Type-C PD controller 68-pin QFN	WLC1115-68LQXQ	Infineon Technologies
Buck and inverter stage MOSFETs	6	N-channel 30 V 18 A (T_a), 40 A (T_c) 2.1 W (T_a), 37 W (T_c) surface-mount PG-TDSON-8 FL	BSZ0910LSATMA1	Infineon Technologies
Buck stage inductor	1	Fixed inductor 6.8 µH 6.5 A 23.3 mΩ	PA4342.682NLT	Pulse Electronics Power
Buck stage current shunt	1	Resistor 0.005 Ω 1% 1 W 1206	LVT12R0050FER	Ohmite
Buck stage input bulk capacitors	2	Ceramic capacitor 22 µF 25 V X6S 1206	CL31X226KAHN3NE	Samsung Electro-Mechanics
Buck output bulk capacitors	4	Ceramic capacitor 22 µF 25 V X6S 1206	CL31X226KAHN3NE	Samsung Electro-Mechanics
Inverter stage current shunt	1	Resistor 0.01 Ω 1% 1 W 1206	LVT12R0100FER	Ohmite
Inverter input bulk capacitors	2	Ceramic capacitor 22 µF 25 V X5R 0805	CC0805MKX5R8BB226	Yageo
Transmitter coil	1	1 coil, 1 layer 6.3 µH wireless charging coil transmitter 45 mΩ max.	IWTX5050CZEB6R3KF1	Vishay Dale
Resonant capacitors	5	Ceramic capacitor 0.1 µF 100 V C0G/NP0 1206	GRM31C5C2A104JA01L	Murata Electronics
Inverter MOSFET snubber capacitor	2	Ceramic capacitor 0.01 µF 25 V X7R 0603	CC0603KRX7R8BB103	Yageo
Op-amp in amplifier and comparator	1	IC opamp GP 2 circuit 8-VSSOP	LMV358AQDGKRQ1	Texas Instruments
Authentication IC for Qi v1.3.2 support	1	Enhanced wireless charging authentication solution	SLS32AIA020U2USON1 0XTMA2	Infineon Technologies
Crystal oscillator (optional)	1	External oscillator XO 48.0000 MHz CMOS SMD	SG7050CCN 48.000000M-HJGBB	Epson
NTC	1	NTC thermistor 100k	NXFT15WF104FEAB021	Murata Electronics

4 PCB layout guidelines

This section explains the schematic and layout design requirements of the WLC1115 solution based on the reference board REF_WLC_TX15W_C1.

The WLC1115 wireless power transmitter consists of power circuits, digital circuits, an Arm® Cortex®-M0 CPU and analog circuitry. The mixed-signal system solution requires special attention when placing and routing the design to maximize the performance of all functions. In Figure 27 the dashed circles in red represent the power sections, those in green indicate precision analog components, and those in purple cover the digital section of the application. When designing an Infineon WLC1115 based EPP Tx, the following order of block-level component placement should be followed:

- Power section – buck, inverter, gate drivers
- Analog section – demodulator, current sensing, Q factor
- Digital section – USB communication, OPTIGA™ Trust, GPIOs, external clock (optional)

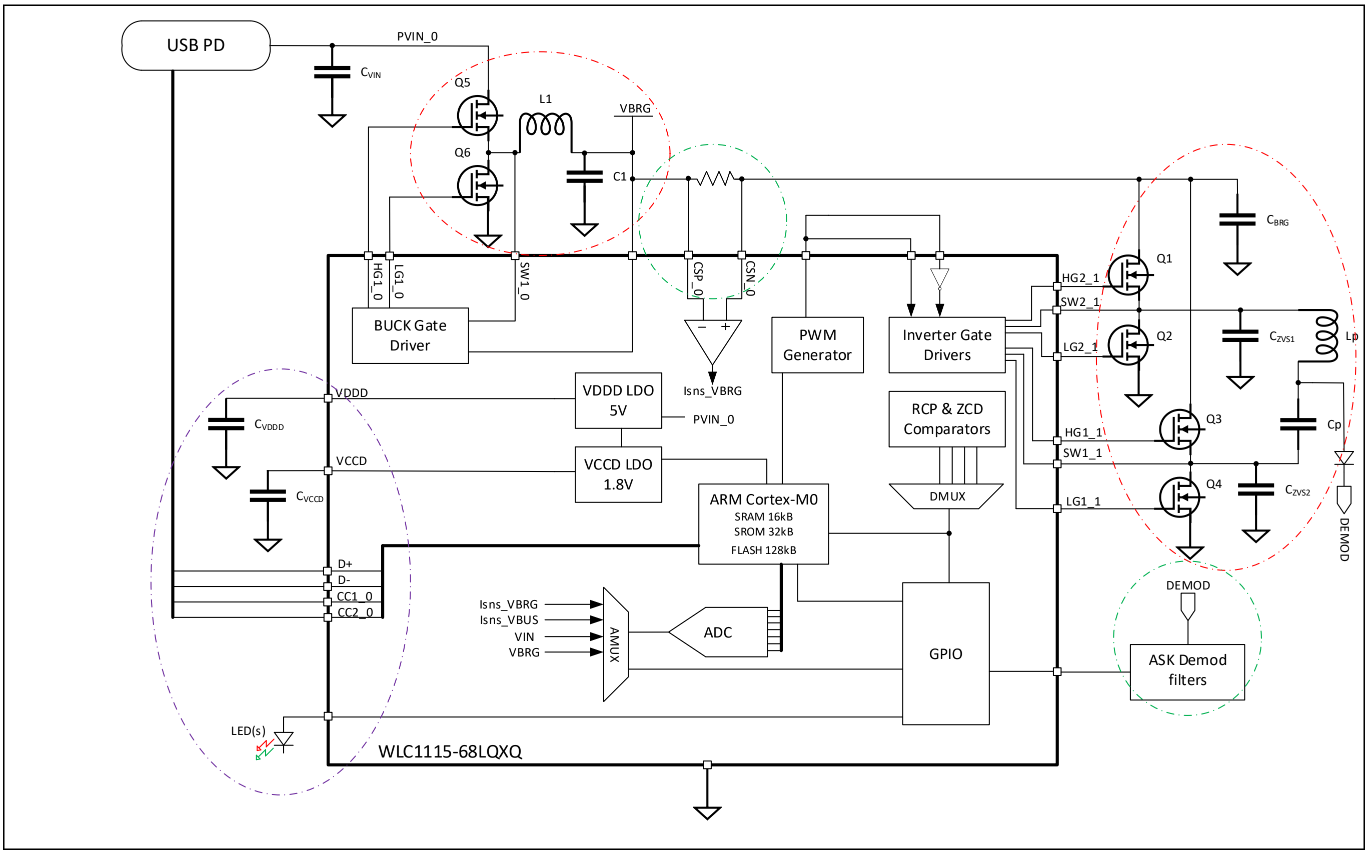


Figure 27 WLC1115 wireless power Tx simplified diagram

4.1 Power section

The power section is the most critical for maintaining high efficiency, providing sufficient thermal management and reducing the EMI. Consideration of the power path should be the first decision, followed by the location of the USB connector and Tx coil location, buck regulator and inverter MOSFETs. The critical power circuits are the buck regulator and inverter bypass capacitors, bootstrap capacitors and ZVS capacitors.

The power path can be described as the main current path from the input connector to the Tx coil and the GND return current back to the USB connector. The optimal design is to minimize this path length to reduce conduction losses and the current loop area.

In Figure 28 the positive current path is highlighted by the blue arrows and drawn on the PCB top layer; the main GND return path is shown in green. The power path is intentionally placed and routed such that the high currents do not need to pass under the WLC1115 (U3) controller IC to supply power to the Tx coil and back. A second path should exist from the WLC1115 IC to the USB connector for the controller quiescent currents (shown by the thinner arrows).

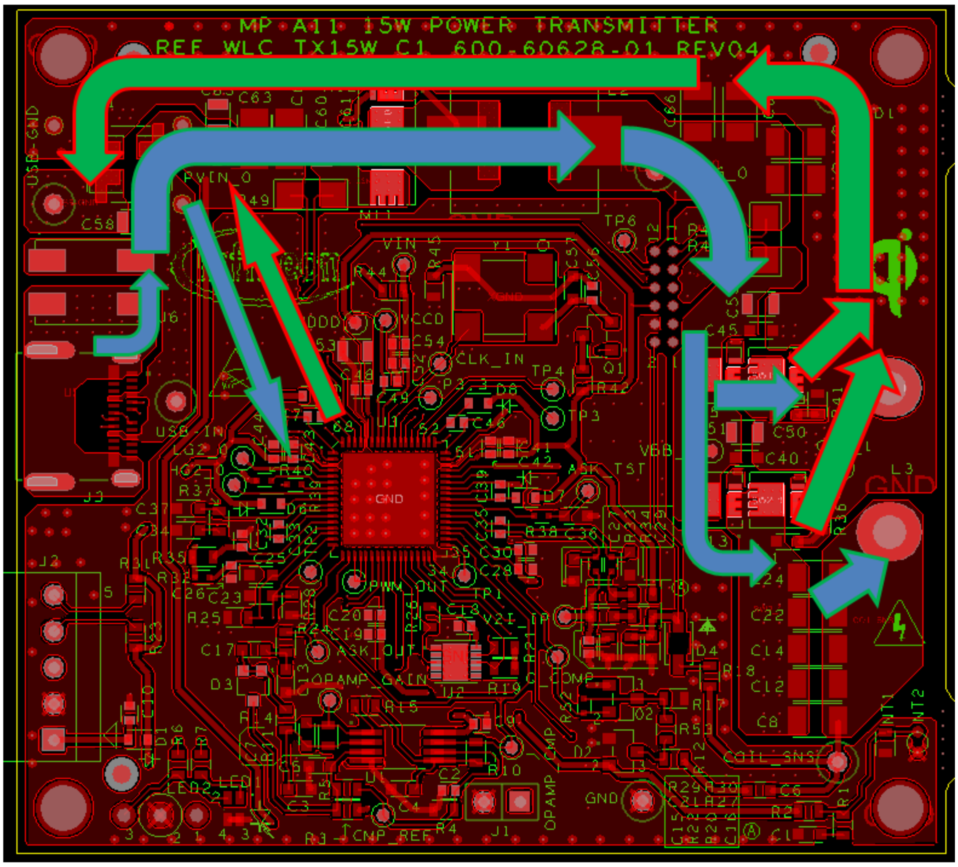


Figure 28 MP-A11 reference design wireless power current paths

4.1.1 Buck regulator

The following section focuses on the buck regulator, with the schematic snippet in Figure 29 and the layout in Figure 30 used as reference. Note that not all components and connections are shown in the snippet.

The most critical current loop for a buck regulator is the area from the input bypass capacitors (C60, C61, C63, C64) to the M11 high-side MOSFET drain and then back to the same capacitors from the M12 low-side MOSFET source-to-GND connection. It is important to provide thermal vias and sufficient copper planes to dissipate the generated heat from the MOSFETs (M11, M12) and the inductor (L2). Finally, the output capacitors should be placed such that the GND reference is a wide copper plane.

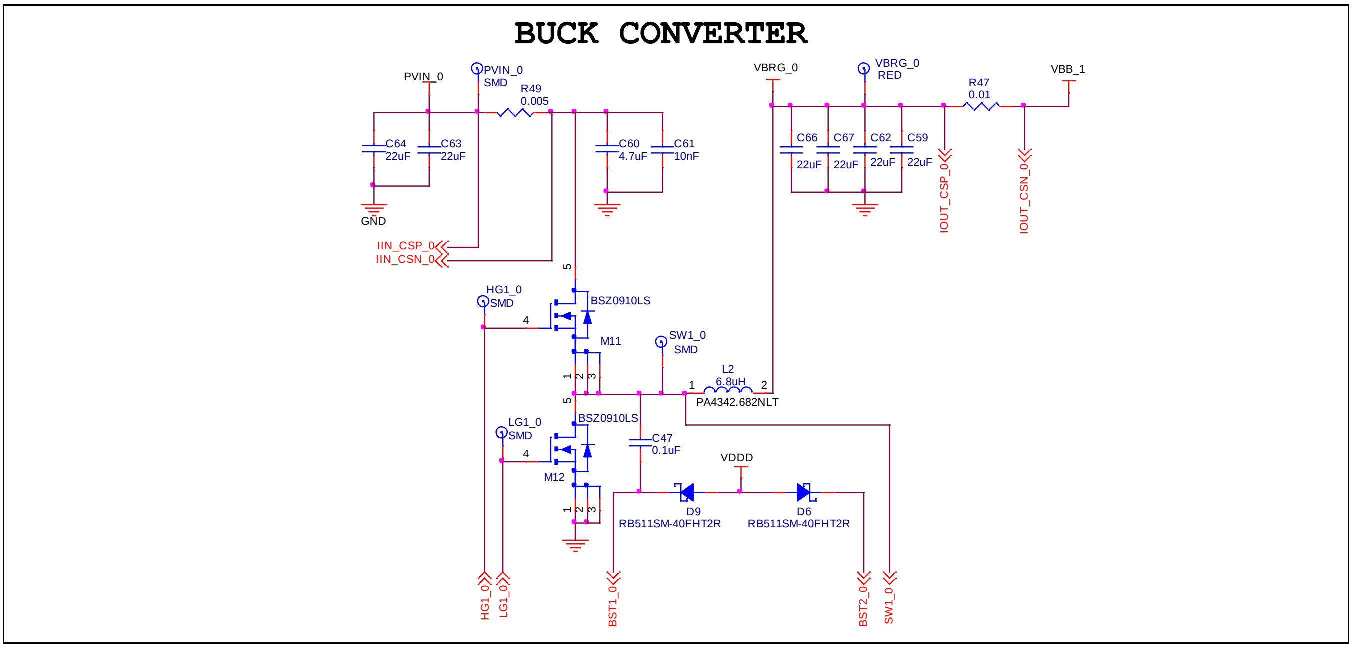


Figure 29 **Buck regulator schematic for inverter supply rail (VBRG)**

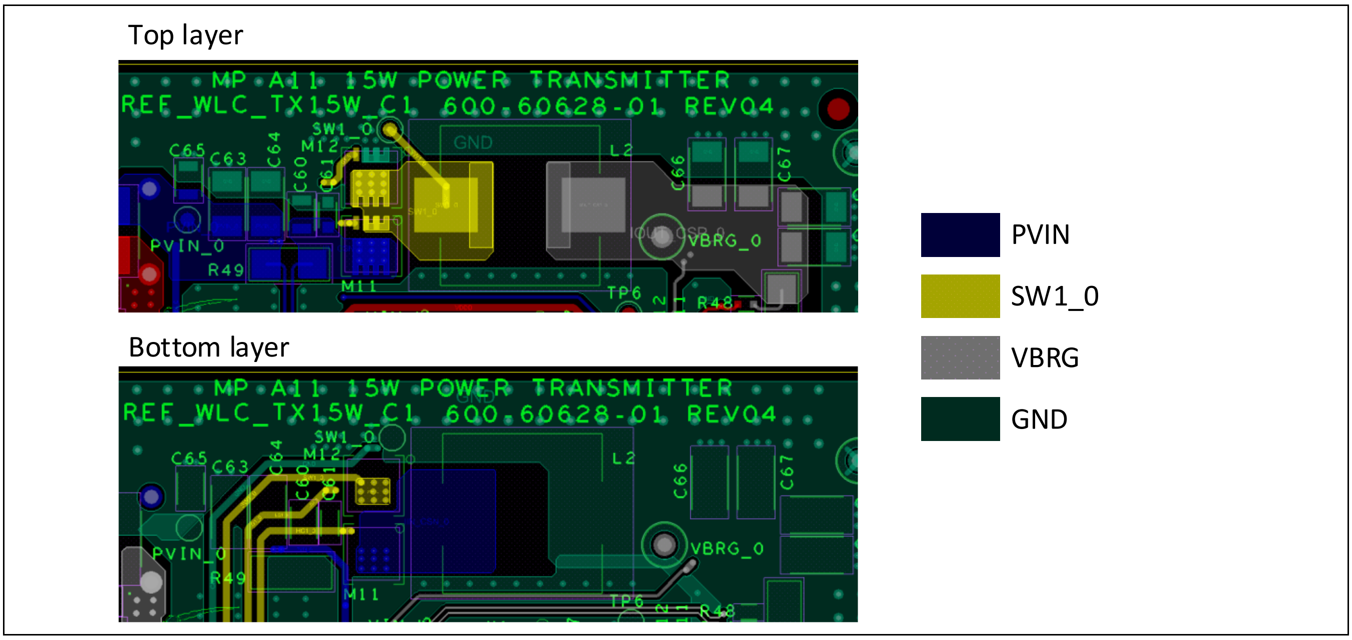


Figure 30 **Buck regulator layout (top and bottom layers)**

4.1.2 Inverter

The full-bridge inverter is the next power section that will be examined in detail. The schematic and layout snippet in Figure 31 and Figure 32 show the reference schematic for the inverter.

The placement of bypass capacitors (C40, C45, C51, C55) is critical to performance. The switching nodes (SW2_1, SW1_1) should be routed wide to reduce impedance and skin effects, and to improve heat dissipation. The ZVS components (C31, R36, C50, R41) should be next to the respective MOSFETs (M14 and M16). The BST capacitors (C39, C46) should be placed next to the WLC1115 IC (U3). Use of multiple vias (six to eight, at least) for layer transitions is required for all connections.

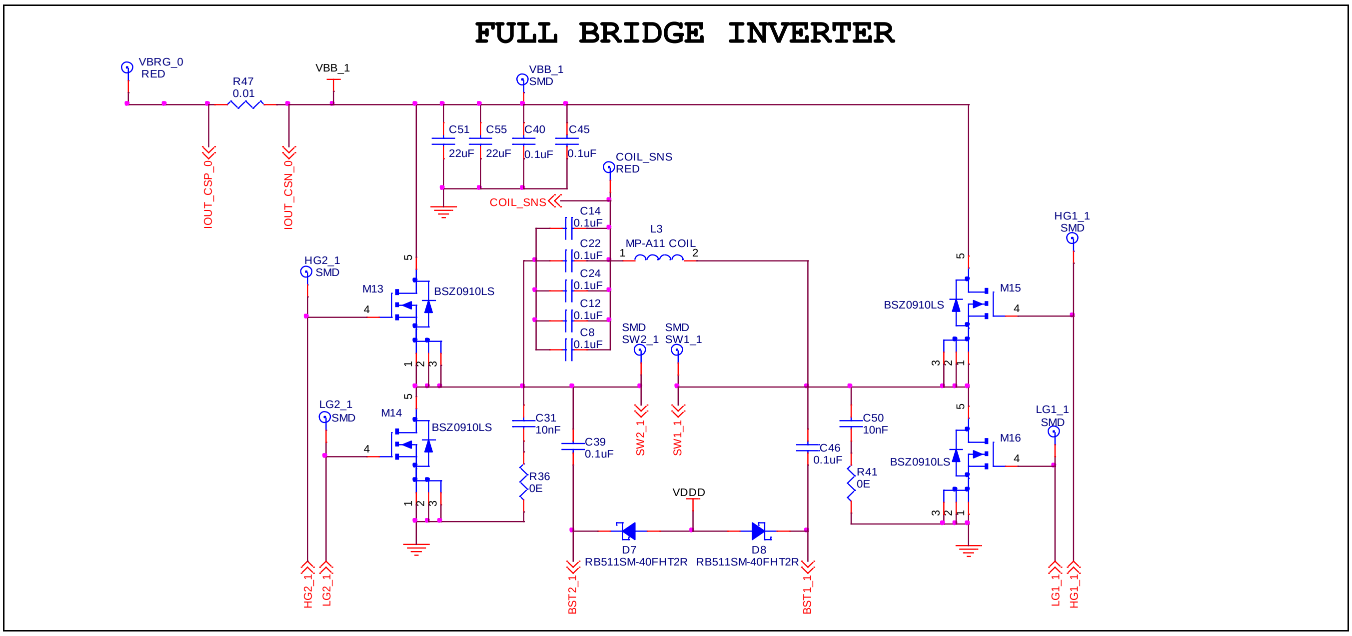


Figure 31 Inverter stage schematic

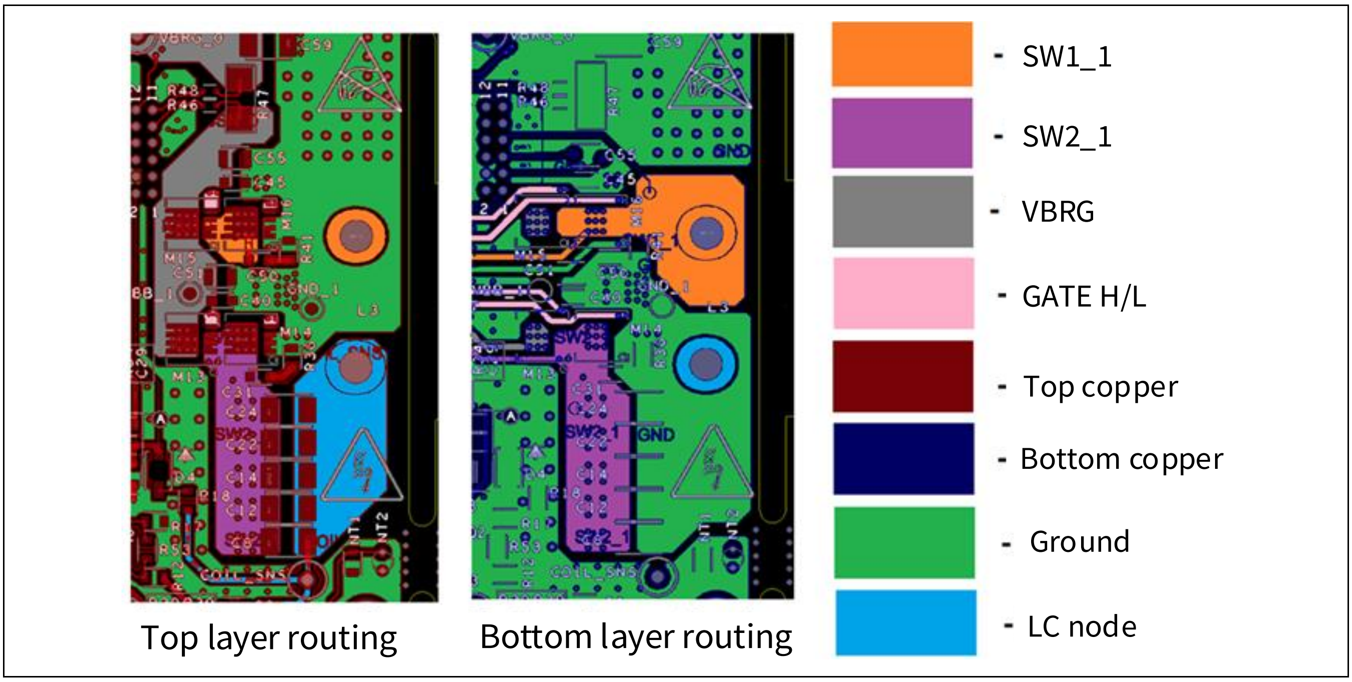


Figure 32 Inverter placement and layout (top and bottom layers)

4.1.3 Gate drivers, BST, bypass capacitors

The connection to the gates and the switching nodes (SW1_1 and SW2_1) to the WLC1115 should be at least 20 mil wide and routed as directly as possible. In addition, a GND signal returns the gate drive current to the device. Use of two vias for each connection layer transition is recommended. The BST capacitors should be located next to U3 and placed so they straddle the respective SW and BST pins.

The following are the minimum number of power-related components necessary for proper operation of the WLC1115 IC (U3): These should all be placed next to U3.

- BST capacitors (C39, C46, C47)
- Bypass capacitors
  - VIN (C28, C30, C52, C54)
  - VDDD (C19, C20, C41, C42, C43, C44, C48, C53)
  - VCCD (C49)
  - VBRG (C26, C32)

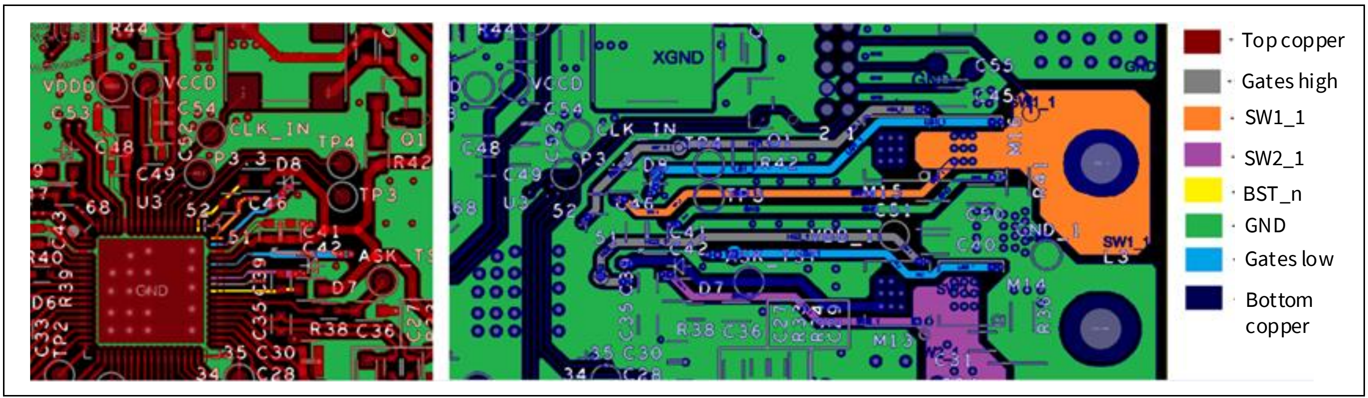


Figure 33 **Routing from the WLC1115 device to the inverter gates and SWx nodes**

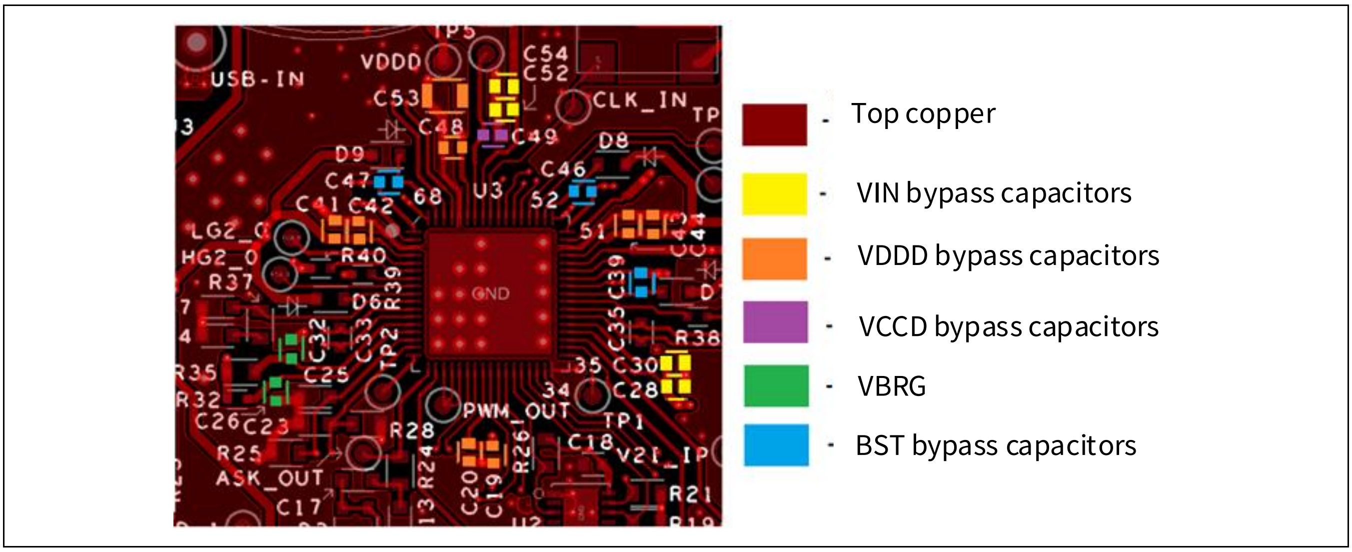


Figure 34 **WLC1115 bypass and BST capacitors placement**

4.2 Analog section

The precision analog circuits are composed of the DEMOD filter, the buck compensation network, the CS filters and the Q factor circuit. In addition, a thermistor input should be considered in the analog domain; this would need filtering before being digitized by the ADC.

4.2.1 Demodulator (voltage path and gain stage)

It is important to avoid the ground connections for each DEMOD component being in the main return path, as shown in Figure 28**.** After component D4, the voltage sensing path becomes relatively high-impedance; therefore, it should not run in parallel with either AC node when being routed unless there is a GND shielding plane between the nets. Both the voltage and current DEMOD sense filters should have a direct GND connection for each reference to the E-PAD of the WLC1115 IC.

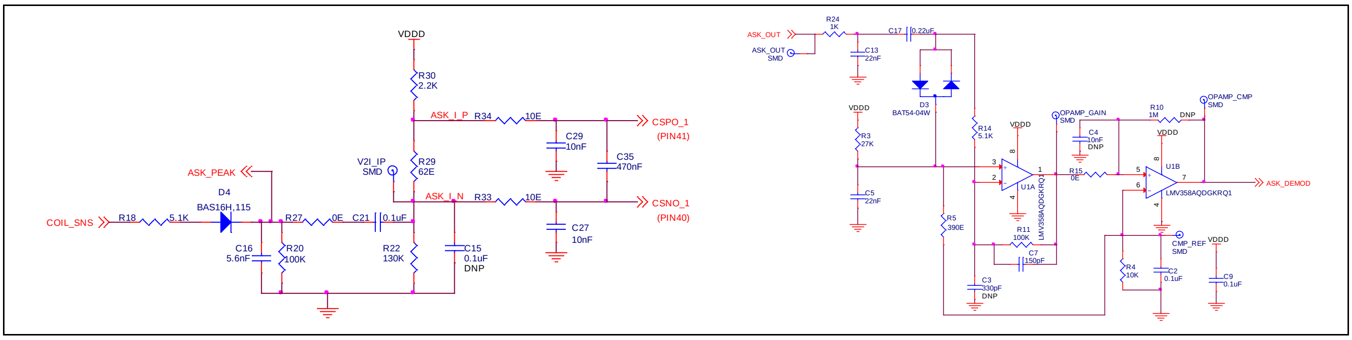


Figure 35 WLC1115 ASK demodulator; voltage path (left); amplifier and comparator stage (right)

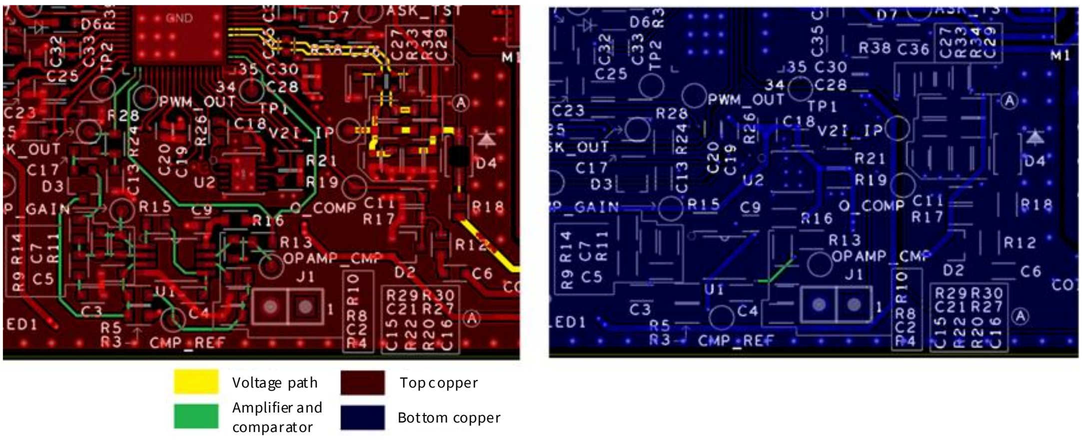


Figure 36 Demodulator filter component placement and routing

4.2.2 Current sensing

Current sensing must use Kelvin sense connections to properly detect the voltage drop across each CS resistor. The input current is measured for buck fault protection and to control the travel adaptor (TA) output power. The VBRG CS resistor (R47) is used to calculate the Tx power for FOD comparison and has an additional differential input filter (R46, R48, C33).

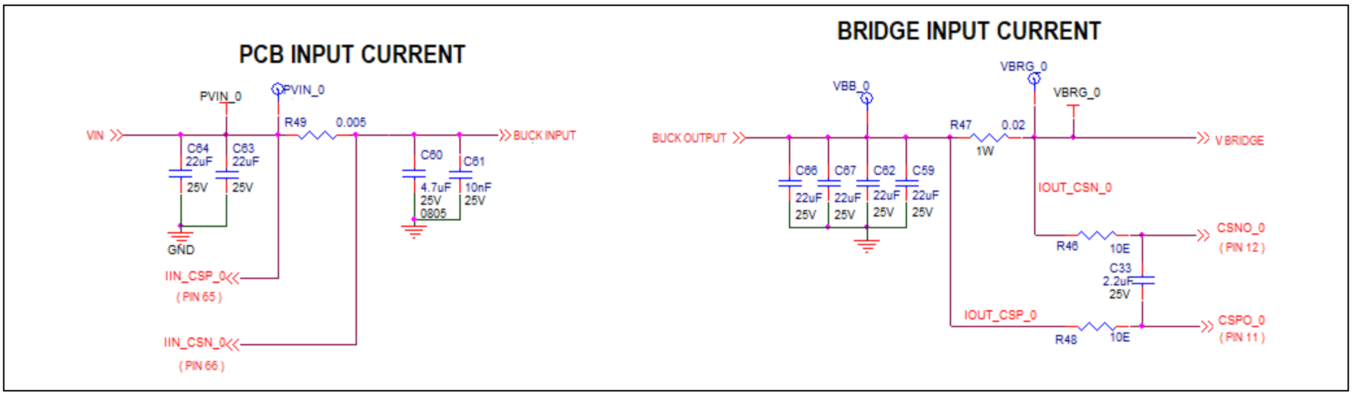


Figure 37 WLC1115 CS resistors schematic

In Figure 38**,** note that the input and bridge CS resistors are Kelvin-sensed from the inside of the component pads. In addition, the CSN and CSP lines are routed from the CS resistors to the WLC1115 IC as a differential pair to avoid common-mode noise being picked up by the signals. Finally, the bridge CS lines are routed between the buck and the XTAL without crossing under either. Capacitor C33 should be placed next to the WLC1115 IC, straddling pins 11 and 12:

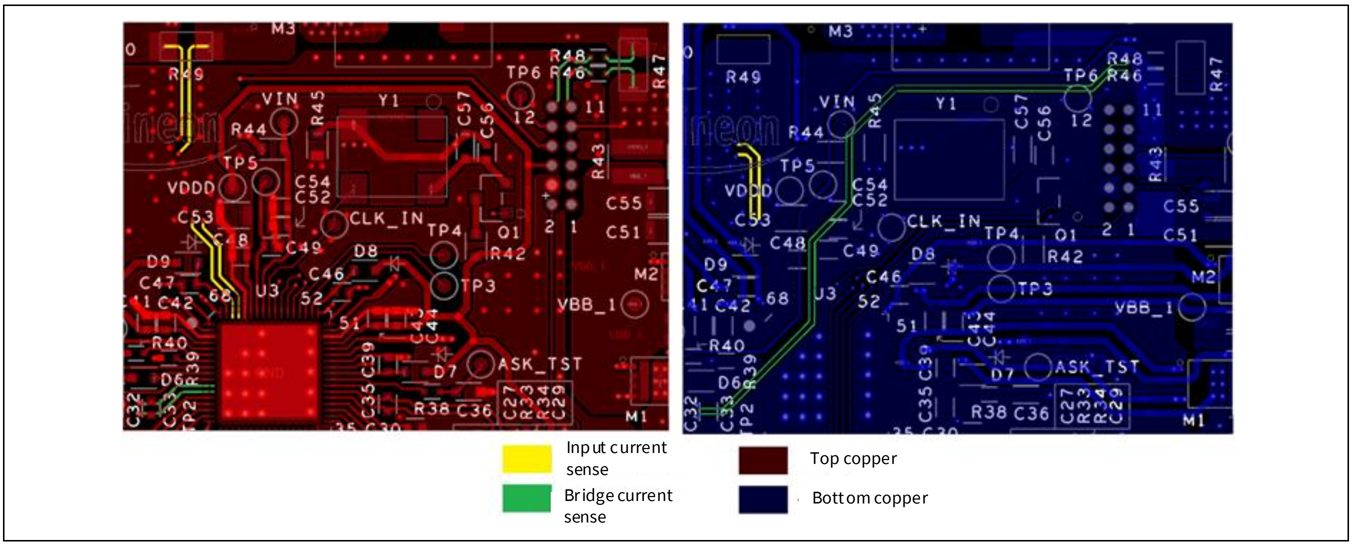


Figure 38 CS resistor connections and routing

4.2.3 Q factor and buck compensation

The Q factor circuit is necessary for EPP-compliant designs and uses the LC decay of the resonance tank to measure the quality factor of the LC tank (wireless Tx coil (L3) and resonance capacitors (C8, C12, C14, C22, C24)). The common node between these components is often referred to as the “COIL_SNS”; together they make up the LC tank. The Q factor and buck regulator compensation component should be placed near the WLC1115 IC and outside the main power path. They should be placed after the previously mentioned components.

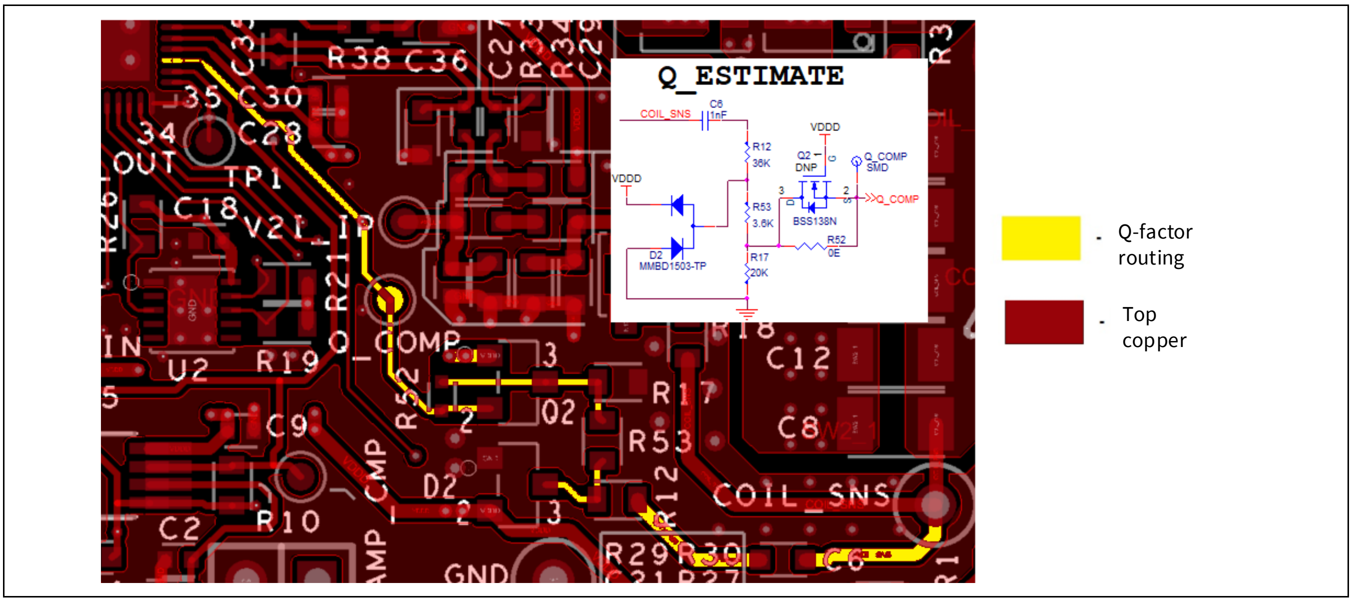


Figure 39 Q factor measurement circuit schematic, placement and routing

The buck compensation components (COMP_0) should be placed next to the WLC1115 IC after all the bypass and previously mentioned components are placed with a direct connection to the E-PAD GND:

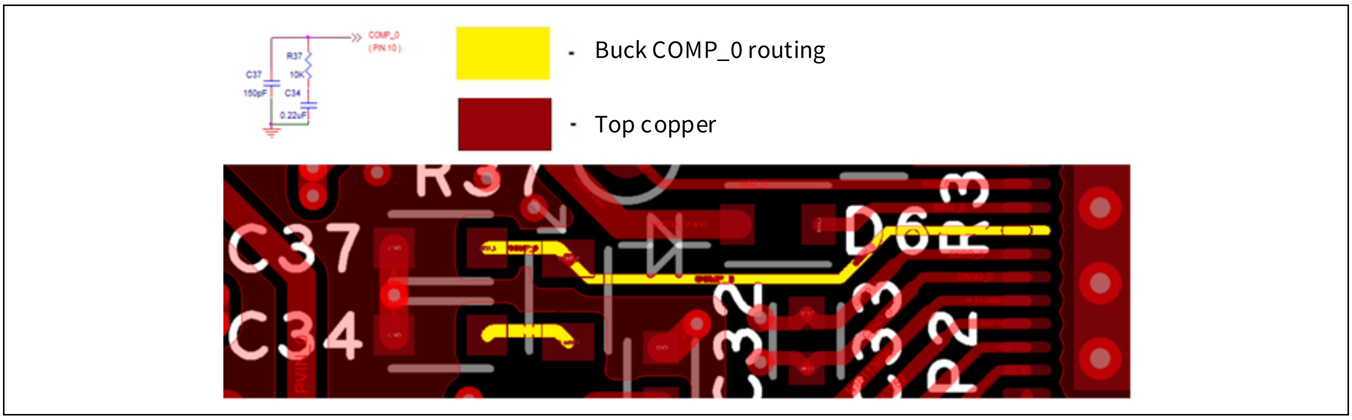


Figure 40 Buck compensation schematic, placement and routing

4.3 Digital section

The following sections are considered digital circuits: GPIOs, clock, OPTIGA™ Trust IC, and the USB communication lines (D+, D-, CC1, CC2). Any GPIOs not mentioned here are low power and relatively low frequency; they are not considered critical and may be routed as convenient. The GPIOs are powered by the VDDD 5 V supply for the digital logic-level reference.

The OPTIGA™ Trust IC is necessary for Qi v1.3.2 authentication. It is recommended to place this component near the WLC1115 wireless controller IC and route the I^2C lines on the inner layers if possible. The clock circuit operates at a relatively high frequency, so these elements should be placed close to the WLC1115 IC when used and have a robust GND connection from the clock circuit to the E-PAD. Q1 allows a disconnect power option to reduce the power consumption when precise timing is not required.

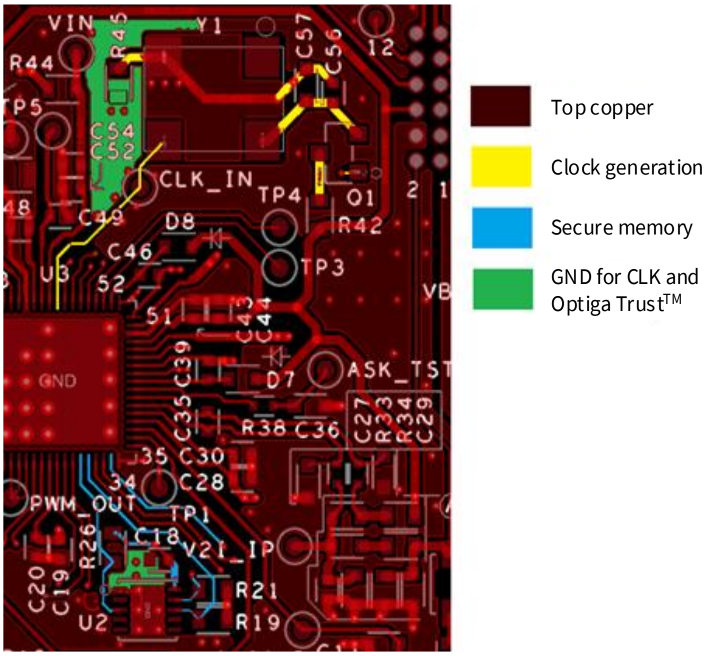


Figure 41 OPTIGA™ Trust memory IC (U2) and clock generation (Y1) circuit

The D+_0, D-_0, CC1_0, and CC2_0 lines should be routed as directly as possible to the USB Type-C connector; they should be routed together similar to differential pairs to reduce the noise interference from coupling or distortion. Avoid routing the traces under the buck or inverter portions of the PCB (if necessary, be sure to use a solid GND plane to shield these from any switching regulator). The D+ and D- and the CC1 and CC2 traces should be routed next to each other, respectively, and should be of the same length to within 5 mm. Avoid unnecessary layer transitions and vias when routing these lines.

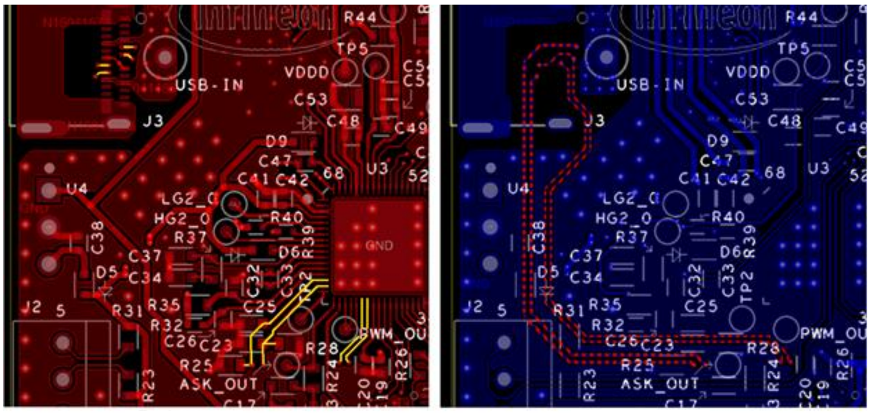


Figure 42 **WLC1115 USB routing (D+ and D-, CC1 and CC2)**

4.4 Thermal management

Thermal management of the solution is critical for high performance and reasonable operating temperatures. In order to improve thermal performance, the use of multiple vias and large surface areas in the form of copper planes are highly recommended. The critical components for adding thermal management provisions are the buck regulator FETs (M11, M12), L2, and the inverter FETs (M13, M14, M15, M16).

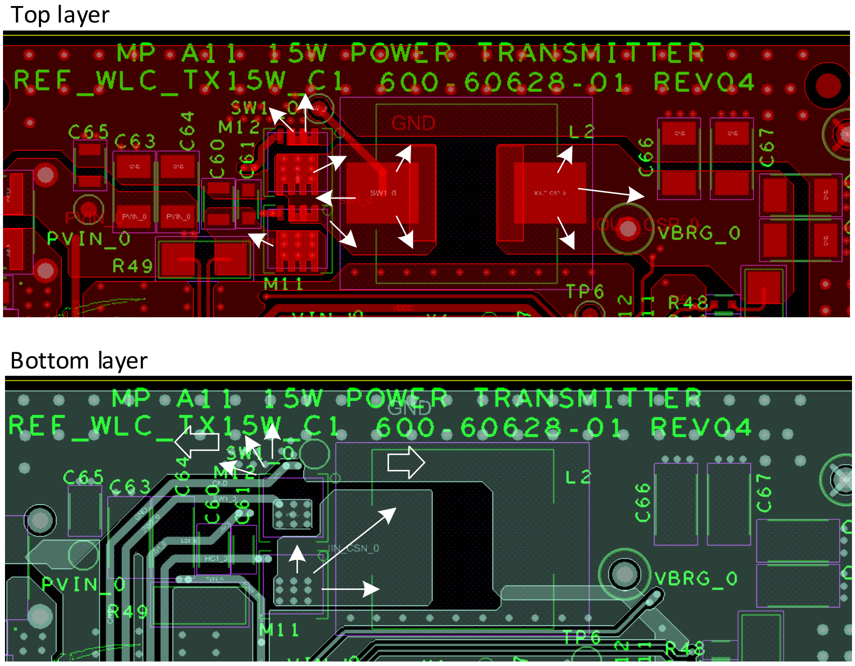


Figure 43 **Buck regulator thermal planes and heat flow (top and bottom layers)**

The WLC1115 IC also needs to have at least 15 thermal vias in the E-PAD and should have direct GND plane access for electrical and thermal conduction. The ZVS components (C31, R36, C50, R41) are also exposed to high current, and should be connected to large copper planes. Thermal performance is improved by using multiple layers with multiple vias to transfer the heat between layers, using heavier copper foil weights and making thinner PCBs. Large continuous planes connected directly to heat sources are the most effective method to reduce the operating temperature of power management components.

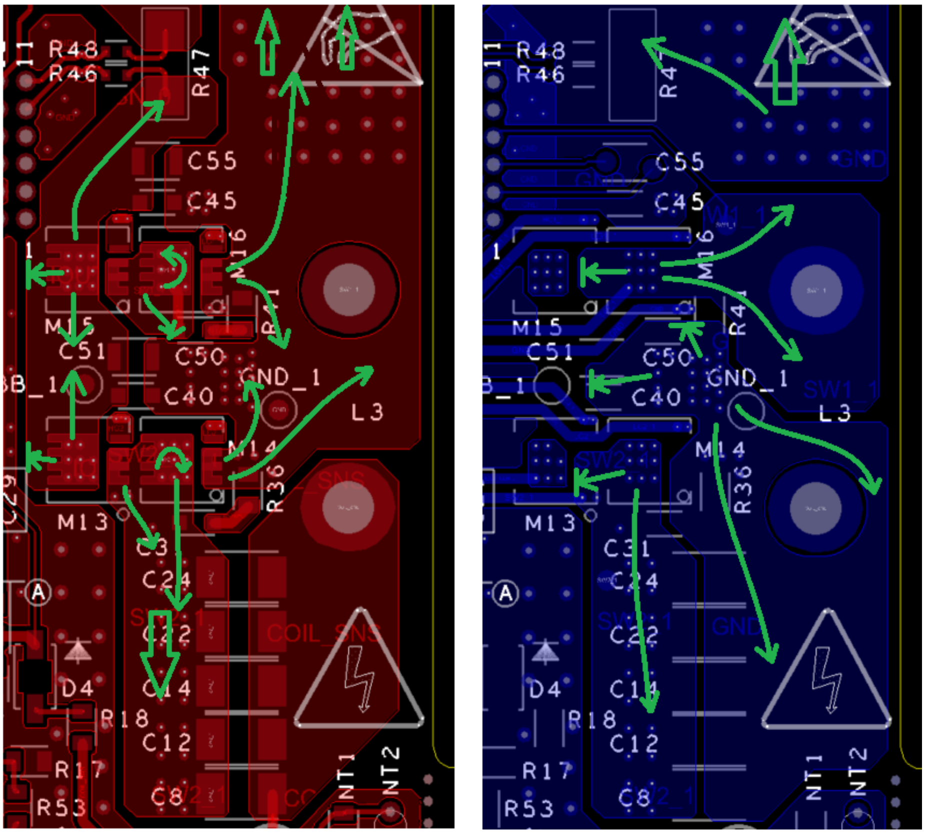


Figure 44 Inverter thermal planes and heat flow (top and bottom layers)

When using parallel planes add vias evenly spaced across each surface for maximum heat transfer to each plane to achieve the lowest possible operating temperature. In the reference design, some signals pass under the WLC1115 IC. E-PAD thermal vias are separated and used to connect the bottom-layer GND planes together.

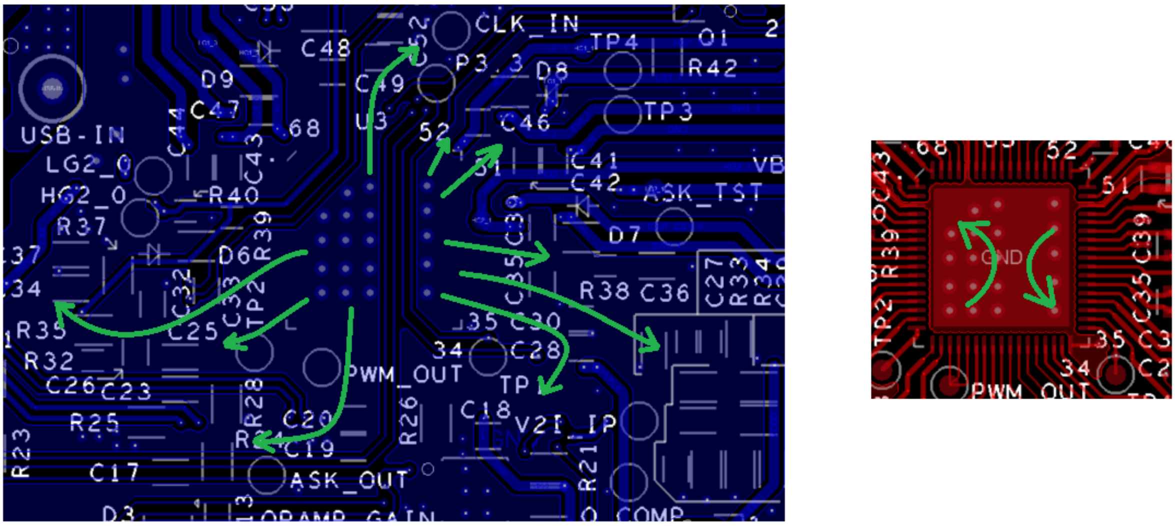


Figure 45 WLC1115 thermal paths and heat flow and thermal vias in E-PAD

4.5 Package footprint design guidelines

For the exact package dimensions, refer to the WLC1115 datasheet [2]. For proper operation, at least 15 thermal vias should be spread across the E-PAD. The solder mask should extend at least 2.5 mils beyond each copper pad opening and the paste mask should be the same dimension as each pin. Designing to the typical dimension is sufficient for proper installation.

5 Schematic and PCB layout review checklist

The schematic entry checklist is captured in Table 7, including the component selection guidelines in section 2.

Table 7 Schematic checklist

Priority	Item	Yes/No/NA
1	The components are well derated for the required operating temperature	–
2	Selected buck inductor part fulfills the ripple current requirement over the entire operating range of the converter	–
3	The selected inductor saturation current rating is well within the peak current that can appear during transients or overload	–
4	The selected inductor is magnetically shielded (full shielding)	–
5	The selected inductor SRF is much greater than (at least 10 times) buck operating frequency	–
6	The inductor part has a tolerance not more than 20 percent	–
7	The buck input and output filter capacitor ESRs do not cause substantial rise in ripple voltage	–
8	The buck input and output filter capacitors have tolerance not more than 10 percent	–
9	The temperature rise caused by ripple currents in capacitors is well within the capacitor-rated operating temperature	–
10	The selected MOSFET current ratings are within the calculated peak current value even at case temperature of 100°C	–
11	The MOSFETs are logic-level type, the gate threshold voltages are below 5 V and low $R_{DS(on)}$ is achievable with 5 V gate drive	–
12	The MOSFET has low parasitic capacitances (in comparison with the part used in REF_WLC_TX15W_C1) for low switching losses	–
13	The transmitter coil part has inductance as specified by Qi	–
14	The transmitter coil Q factor is high or the effective coil resistance at inverter operating frequency is less than 50 mΩ	–
15	The resonant capacitor part in the inverter stage meets Qi recommendations for the MP-A11 coil	–
16	The capacitor part for the resonance capacitor has a stable capacitance over its operating voltage and temperature range (C0G or NP0-type dielectric)	–
17	The capacitor voltage rating covers Qi recommendations for peak voltage	–
18	The Type-C USB connector at input has the necessary pins for power, CC lines and D+ and D- lines	–
19	Any common-mode filter at input, if used, has a DCR less than 20 mΩ	–
20	There is 5.1 kΩ pull-down and 330 pF capacitor-to-ground for both CC lines	–
21	The CC1, CC2 connections and D+, D- connections are correctly mapped at the USB connector pins and the WLC1115 pins	–
22	The CS resistors for buck stage input and output side have a tolerance no less than 1 percent and temperature coefficient less than or equal to 50 ppm	–

Priority	Item	Yes/No/NA
23	There are low-value (less than 100 nF) low-ESL type decoupling capacitors placed close to the buck switching leg and the two inverter switching legs	–
24	The WLC1115 VIN pin has decoupling capacitors as per datasheet recommendations	–
25	The VDDD and VCCD pins have decoupling capacitors as per WLC1115 recommendations and the effective capacitance of these capacitors at 5 V yields the recommended capacitance value	–
26	The WLC1115 pins where pin voltage is expected to go beyond absolute maximum value (during transients or faults) have necessary clamping	–
27	The diodes used for clamping of QCOMP1 and QCOMP2 pins have low leakage (less than 100 nA) at 5 V operation	–
28	The CSPO and CSNO pins have filter capacitors	–
29	The I^2C lines used for interface with the authentication IC have the necessary pull-up to VDDD	–
30	The VBRG, VBRG_DIS and VBUS_IN pins have 0.1 µF decoupling capacitors close to WLC1115	–
31	The unused pins of WLC1115 are terminated as recommended in the WLC1115 datasheet	–
32	The VTARG pin of the programming connector is connected to VDDD with a series diode as in the REF_WLC_TX15W_C1 schematic	–
33	The op-amp part used in the ASK demodulator section is of rail-to-rail output type with a slew rate less than 1 V/µs	–
34	The bootstrap capacitor has 0.1 µF capacitance at the maximum input voltage	–
35	The chosen bootstrap diode forward voltage is small to ensure lower conduction losses	–
36	The mechanical accessories used around the transmitter coil (spacers, acrylic, tapes) do not contain any metallic elements	–
37	The chosen combinations of tapes, spacers and acrylic for coil mounting gives a dz height as recommended by Qi (refer to Figure 17**)**	–
38	The chosen NTC has an operating range of at least -20°C to +100°C	–
39	The chosen NTC for coil temperature measurement has a long lead for placement of the sensing element near the coil and soldering of leads on the PCB	–
40	The NTC feedback to WLC1115 has a low-pass filter with bandwidth lower than ASK modulation frequency	–
41	The series resistance with NTC ensures that the current in NTC results in a power loss lower than the NCT-rated value even at the highest NTC-rated temperature	–
42	The components are well derated for the required operating temperature	–
43	The schematic is identical to the schematic of REF_WLC_TX15W_C1 in [3]	–

Table 8 Layout checklist

Priority	Item	Yes/No/NA
1	The power path is direct from the input power connector to the Tx coil with wide copper and direct GND connection	–
2	Buck input bypass capacitors are placed next to the buck MOSFETs and straddle VBUS to GND	–
3	The buck inductor is placed near the buck MOSFETs, and buck output capacitors are placed next to the inductor with GND return to low-side MOSFET and input bypass capacitors	–
4	The buck MOSFET gates, SW1_0 and GND node are routed directly to the WLC1115 device without any other high-frequency trace in other layer(s)	–
5	The IIN_CSP_0 and IIN_CSN_0 traces from input 5 mΩ should be guarded with GND and should have a GND plane in other layer(s)	–
6	Ensure that IIN_CSP_0 and IIN_CSN_0 have identical numbers of vias in each trace to keep the impedance change minimal	–
7	Inverter input bypass capacitors are placed next to each half-bridge and straddle VBRG to GND	–
8	Inverter ZVS capacitors are placed next to the LS MOSFETs and switch node (but not blocking the power path)	–
9	Additional copper and vias are added for heat dissipation near all MOSFETs and under WLC1115 E-PAD	–
10	All BST capacitors are placed next to the WLC1115 device	–
11	All PVDD, VDDD, VCCD and VBRG bypass capacitors shown in Figure 34 are placed next to the WLC1115 device	–
12	The bootstrap capacitor and diodes are placed close to WLC1115	–
13	DEMOD filters are placed outside the power path and near the WLC1115 device	–
14	CS resistors are Kelvin-sense connected and routed to the WLC1115 device as differential pairs	–
15	The CC lines and DP, DM lines are routed differentially for most of the trace lengths, do not overlap with any high-frequency nodes and are guarded with GND on either side	–
16	If an external oscillator is used, the oscillator part has a separate GND plane below the part in all layers	–
17	The clock signal from the external oscillator has only GND on other layer(s) and no other signal or power trace	–

The following guidance should be used when routing the following nets from the evaluation board. These are minimum values and routing wider than listed is recommended when space permits.

Table 9 Minimum routing guide

Net name	Minimum routing width*
VBRG, SW0, SW1_0, SW1_1, SW2_1, COIL_SNS (Tx coil to resonance capacitors only)	2.54 mm (100 mils)
VIN	2 mm (78 mils)
VDDD, VCCD	0.75 mm (30 mils)
BST nodes, gate drive lines	0.5 mm (20 mils)
COIL_SNS (to ASK filter and Q factor circuit)	0.2 mm (8 mils)
CS signals (CSP_N, CSN_N), routed as differential pairs	0.127 mm (5 mils)
GPIOs, I^2C, interrupts, ASK DEMOD, clock	0.127 mm (5 mils)

* - Using 1-oz copper

6 Acronyms/abbreviations

Acronym/abbreviation	Definition
ADC	analog-to-digital converter
Arm®	advance RISC machine, a CPU architecture
ASK	amplitude shift keying
BOM	bill of materials
BPP	baseline power profile
CC	configuration channel
CCM	continuous conduction mode
CPU	central processing unit
CSA	current sense amplifier
CSN	current sense negative
CSP	current sense positive
CV	constant voltage
DCR	direct current resistance
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EPP	extended power profile
ESD	electrostatic discharge
ESR	equivalent series resistance
FCCM	forced continuous conduction mode
FOD	foreign object detection
FSK	frequency shift keying
GPIO	general-purpose input/output
HBM	human body model
IC	integrated circuit
IDE	integrated development environment
I^2C	inter-integrated circuit, a communication protocol
I/O	input/output
LDO	low-dropout regulator
MCU	microcontroller unit
MOSFET	metal oxide semiconductor field-effect transistor
NC	no connect
OCP	overcurrent protection
OTP	overtemperature protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PDO	power delivery objects

Acronym/abbreviation	Definition
PPS	programmable power supply
POR	power-on-reset
PCMC	peak current mode control
PWM	pulse-width modulator
QFN	quad-flat no-lead, a type of IC packaging
Qi	pronounced “chee”
RAM	random access memory
ROM	read-only memory
R_D	pull-down resistor on Type-C CC lines
R_P	pull-up resistor on Type-C CC lines
Rx	receiver
SCB	serial communication block
SCL	I^2C serial clock
SCP	short-circuit protection
SDA	I^2C serial data
SMD	surface-mount device
SPI	serial peripheral interface, a communication protocol
TA	travel adaptor
TCPWM	timer/counter pulse-width modulator
Tx	transmitter
UART	universal asynchronous receiver transmitter
USB	universal serial bus
ZVS	zero voltage switching

References

[1] Qi specifications, WPC knowledge base, https://www.wirelesspowerconsortium.com/knowledge-base/specifications/download-the-qi-specifications.html

[2] WLC1115 – Wireless charging IC (WLC) – Transmitter 15W with integrated USB Type-C PD controller datasheet

[3] REF_WLC_TX15W_C1 design files, http://www.infineon.com/ref-wlc-tx15w-c1

[4] D. Graovac, et al., MOSFET power losses calculation using the datasheet parameters/Infineon Application Note 2006-07 V1.1 – Infineon Technologies AG

[5] Alan Huang, Hard commutation of power MOSFET OptiMOS™ FD 200 V/250 V/Infineon Application Note 2014-03 V1.0 – Infineon Technologies AG

[6] SangCheol Moon, et al., “Analysis and design of a wireless power transfer system with an intermediate coil for high efficiency”, IEEE Transactions on Industrial Electronics, Vol. 61, No. 11, Nov. 2014

Revision history

Document revision	Date	Description of changes
**	2022-05-03	New application note.
*A	2022-05-12	Updated WLC1115 logic block diagram and REF_WLC_TX15W_C1 power transmitter board brief specification.
*B	2023-02-24	Updated specifications table in Table 1 Updated the design steps in section 2.3.2 Updated the schematic snapshot in Figure 35 Updated Table 6 to match REF_WLC_TX15W_C1 BOM

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