Hardware design guide for the XMC7000 family

About this document

Scope and purpose

This application note describes how to set up a hardware environment for XMC7000 MCU family.

Intended audience

This application note is intended for hardware designers.

Associated part family

XMC7000 family XMC7100/XMC7200 series of **XMC™ industrial microcontrollers**.

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1 Introduction

This document describes how to set up a hardware environment for the XMC7000 MCU family.

Design restrictions and recommendations on signal wiring and the electrical power system of the MCU are considered. For more details on the device features and its relevant settings, see the **XMC7000 Architecture Technical Reference Manual (TRM)** and the **device datasheet**.

This application note answers most of frequent questions. It is not intended to replace the designer's responsibility.

2 Package selection

First, decide the package you want to use for your design. Several considerations drive this decision, including number of I/O pins required, PCB and product size, PCB design rules, and thermal and mechanical stresses.

The device families have a very large selection of devices to help match your exact needs in any situation with an efficient and cost-effective solution. Packaging solutions range from the ultra-small wafer scale packages to high-pin-count ball grid array packages. Easier to layout on lower layer counts and lower cost PCBs are the Thermally Enhanced Quad Flat Pack (TEQFP). TEQFP packaging options range from 100-pin devices to 176-pin devices for example.

2.1 TEQFP

- Easier to route signals due to large pitch and the open area below the part
- Less mechanical rigidity for more protection against vibration and mechanical stress
- Disadvantage: larger package

2.2 BGA

- Small-scale package offering high pin counts in larger lead pitches, which significantly reduce the manufacturing complexities for high-I/O devices. BGA packages are used in applications requiring:
  - Faster circuitry speed because the terminations are much shorter and therefore less inductive and resistive
  - Better heat dissipation
- Conventional surface mount technology (SMT) production technologies such as stencil printing and component mounting can be used.
- Robust reflow processing, due to a higher pitch (1.27 mm, 0.050”, typical), better lead rigidity, and self-alignment characteristics. Self-alignment during reflow is beneficial and opens the process window considerably.
- Disadvantage: X-ray is needed for solder joint inspection.

3 Power supply

3.1 Power domains

The MCU power system is based on separate analog and digital supplies as listed in **Table 1**.

Table 2 describes the functionality of each power supply pin.

Table 1 Power domains

Power domain	Associated pins
	XMC7100/7200 Series
Analog	VDDA, VSSA
Digital	VCCD, VSS
I/O	VDDIO, VSSIO
Shared digital and I/O	VDDD

Table 2 Power supply pin description

Pin name	Function	Nominal power domain voltage range
VDDD/VSSD	Shared power supply pins for internal voltage regulator, internal logic, I/O domain with GPIO_STD cells and debug interface	3.3 V–5.0 V
VSSD_1	Only BGA package: Silent ground connection	-
VDDIO_1/VSSIO_1	Power pins for I/O domain with GPIO_STD I/O cells grid	3.3 V–5.0 V
VDDIO_2/VSSIO_2	I/O power pins for GPIO_STD I/O cells	3.3 V–5.0 V
VDDIO_3/VSSIO_3	I/O power pins for HSIO_STD I/O cells for memory interfaces, but also slow signals shared on that domain *Note: Only BGA packages.*	3.3 V
VDDIO_4/VSSIO_4	I/O power pins for HSIO_STD I/O cells for Gigabit Ethernet shared with slow signals *Note: Only BGA packages.*	3.3 V
VDDA/VSSA	Power supply pin pair for analog part of the MCU	Same as VDDIO_2, VDDD, or both depending on the deployed analog pins belonging to the domain
VREFH/VREFL	Reference voltage pins for the A/D converter	Same as VDDA
VCCD	Internal core supply case: Dedicated power supply pin to the internal voltage regulator output to buffer the core voltage with an external smoothing capacitor External core supply case: Depending on the device and the power dissipation of an application, these pins are deployed for connecting the external voltage source to the core supply. General:	1.1 V

Power supply

Pin name	Function	Nominal power domain voltage range
	If a device package has several VCCD pins, all VCCD pins must be shorted together. Therefore, the connections must have low impedance. For a BGA design, a common power island for VCCD is recommended to reduce the EMI.	

To define a single supply rail, all power supplies should be connected to voltages between 3.3 V and 5.0 V. If you need to apply different power supply voltages, such as 5 V to the analog system (i.e., $V_{DDA} = V_{REFH}$) and 3.3 V to V_{DDIO} of the MCU port pins, see the operating conditions in the device datasheet. **Table 1** lists the available power domains on the MCU.

Devices designed for applications with higher power dissipation require an external core supply source, which is controlled by dedicated MCU pins.

3.2 Analog-to-digital converter supply pins

To avoid additional leakage current, connect the analog supply pins (VDDA, VSSA, VREFH, and optionally VREFL), even if the ADC is not used.

3.3 Power supply variants

Although separate power supplies are provided in the MCU, dependencies between each other must be considered. The power domains are independent of each other.

3.3.1 ADC

Analog inputs that are enabled belong to dedicated I/O domains, which means that the applied voltage level of an analog sensor is limited to the I/O domain supply level and the protection diode structure. This implies that the analog supplies and the I/O domains of the selected analog inputs must have the same voltage supply level.

3.3.2 Debug connection

The power supply that you select must allow both the debug hardware tool and the MCU to communicate with each other. See **Debug interface**.

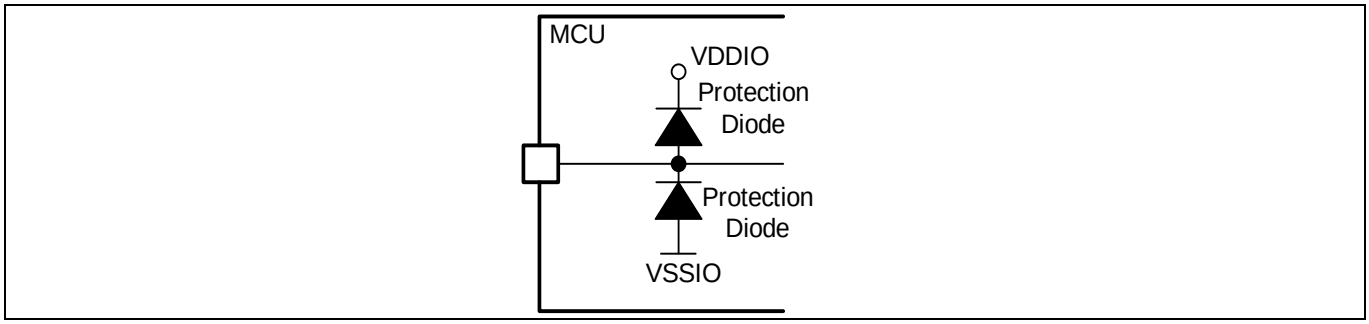


Figure 1 Protection diode structure for all I/O pins

3.4 Power ON/power OFF sequence of power supply domains

Different voltage levels can be supplied to the power rails of the MCU. Therefore, power ON/OFF sequence is not required for power supplies of many devices. When there is no supply voltage at V_{DDD}, but the analog supply

V_{DDA} is powered, a leakage current inside the MCU can occur. However, no port output will be driven. See the **device datasheet** to determine whether the device you selected needs a power sequence.

3.4.1 General

- Disable monitoring features (for example, LVD, BOD, internal supply monitoring via ADC) before disabling related power domains. Otherwise, an unintended reset or fault might occur.
- Disable output pins or tie them to LOW before disabling the power domains.
- Disable input buffers before disabling the power domains.
- Power sequencing requirements and power domain dependencies can differ between power modes. So, when domains need to be switched OFF to reduce the leakage current in power save modes, carefully consider the transition phase for entering and leaving the modes.
- ECU peripherals must be in proper states during the power mode transitions.

3.4.2 External core supply

- XMC7000 MCU devices running with an external core supply have the same power ON/OFF sequence, because the MCU starts in the internal supply mode and the external core supply must be enabled by the application. In power OFF transition, the external core supply is disabled by the MCU.

3.4.3 ADC

- In Active mode, leakage current occurs only when $V_{CCD} > V_{DDA\_ADC.}$
- Many I/O domains with shared analog/digital inputs can be ramped up after VDDA_ADC, as long as the ADC does not start the sampling operation of these domains.
- When the I/O domain is deployed only for digital signaling, many I/O domains can also have voltage operation range different from that of the ADC. See **Clamping the structure of I/O pins with shared analog** function.
- Do not address analog multiplexing bus (AMUXBUS) to unpowered domains.

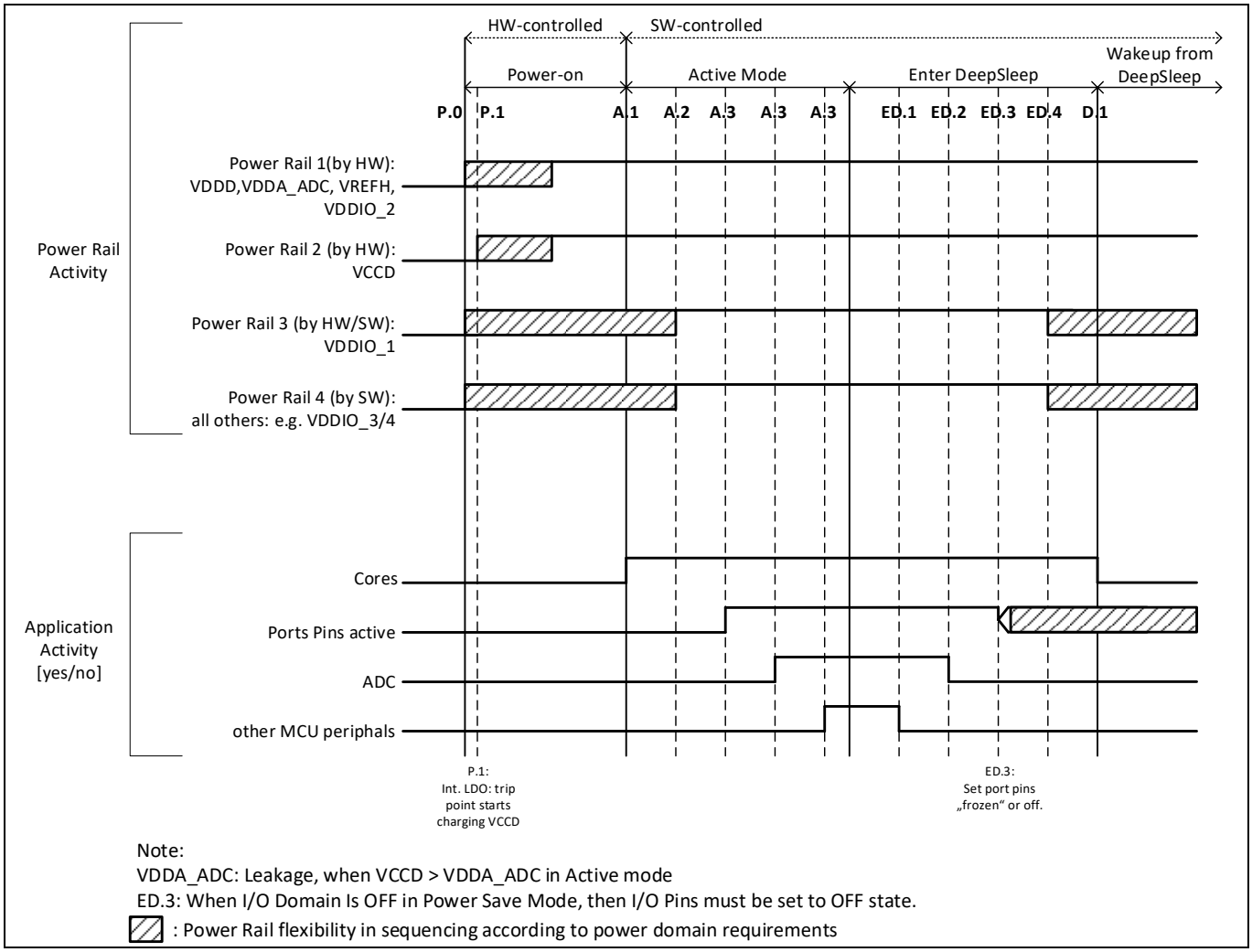


Figure 2 Power sequencing example on XMC7000 series

3.5 Power supply circuit

To meet EMC requirements for the target board, a noise-efficient supply buffering concept is needed. Therefore, the supply should be filtered. To have a minimum noise on the analog supply, it is recommended to use a separate analog and digital power supply.

See **Appendix A - Power supply concept** for power supply concept proposal for different devices.

3.6 External core supply control

The power supply concept description is not part of this document. See the application note corresponding to your device in **Related documents**.

3.7 Unused power domains

Unused power domains are usually considered as a permanent OFF state related to the power domain in the full application lifecycle. However, a temporary state of unused domain is also possible, when some not-always-on power domains stay ON in power save modes. For details on how to handle the I/O port pins of a dedicated domain, see **Port input/unused pins**.

Power supply

In general, the following are the main classes of unused domains:

- Permanent unused domain: Not required in the application
- Temporary unused domain: Disabled in power save mode

See **Appendix E - Unused power domain handling** for details on different devices.

If you do not find information on unused power domains in the device datasheet, contact the Technical Support.

4 Clock sources

The MCU provides several clock sources depending on the system requirements. **Table 3** lists the available clock sources for the MCU system and shows how the clock sources are connected to the MCU internal clock system.

Table 3 Clock sources

Clock source	Oscillator	Int/ Ext	Port pin name (ext. only)	Frequency	Trimmable	Use case
Internal Main Oscillator (IMO)	Yes	Int	-	8 MHz	Yes	LIN
Internal Low-Speed Oscillator (ILO)	Yes	Int		32 kHz	Yes	
External Crystal Oscillator (ECO)	Yes	Ext	ECO_IN ECO_OUT	~4 MHz to 33.33 MHz	Yes	CAN communication
Watch Crystal (WCO)	Yes	Ext	WCO_IN WCO_OUT	32.768 kHz	No	Watch
EXT_CLK pin[1]	No	Ext	Optional on several pins	Note[2]	–	Test
Reference clock for Ethernet PHY and MAC	Yes	Ext	ETHn_REF_CLK	50 MHz	–	Ethernet: RMII
				125 MHz	–	Ethernet: GMII, RGMII

[1] This port pin is bi-directional and can be used as an external clock source for the device and as a clock observation for internal clock signals.

[2] See External Clock Input Specifications in the device datasheet.

5 Reset circuit

To make sure that a MCU operates within the specifications, an external reset signal via the reset input pin (XRES pin) or an internal reset signal can be generated. The implementation of the internal reset circuits has several advantages over the hardware design:

- Reduced bill of material (BOM) cost as the external monitoring ICs are removed
- Detection of MCU internal out-of-range operations, which cannot be monitored externally (for example, MCU internal voltage drops)

Note that external monitoring or resetting ICs might still be needed based on the application requirements.

5.1 Reset pin (XRES)

A switch connects the reset input pin to VSSIO (Ground). An internal pull-up resistor and an internal noise filter of minimum 100 ns are available, to reduce the BOM cost. If an external capacitor is applied for additional filtering, make sure that the EMC requirements are fulfilled. Otherwise, the ESD test pulses might destroy the ESD protection structure inside the MCU.

For details on the reset pin, see the datasheet.

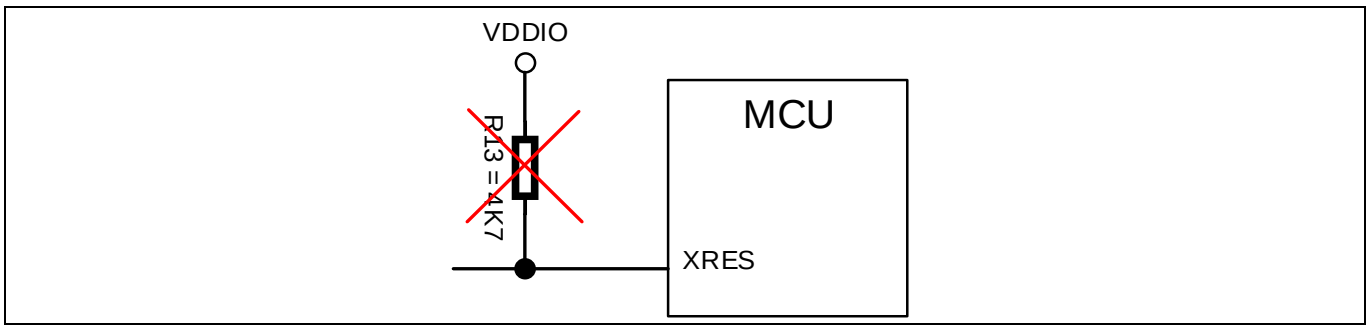


Figure 3 External reset input (XRES)

5.2 Power supply monitoring

To make sure that the MCU is not running out of the operating conditions, a broad range of power monitor circuits is provided by the MCU. See the device **Architecture TRM** and datasheet for more details.

5.2.1 Power-on reset (POR)

Power-on reset (POR) circuits provide a reset pulse during the initial power ramp. Here, only the V_{DDD} power supply rail is observed.

5.2.2 Brown-out detection (BOD)

The brown-out detection (BOD) circuit protects the operating or retaining logic from possibly unsafe supply conditions by applying reset to the device. BOD circuits for the power supply rails VDDD, VDDA, and VCCD are provided. A reset is generated when one of the monitored operating ranges is undercut. This circuit is required to detect a sneaking voltage drop of the battery power supply.

5.2.3 Low-voltage detection (LVD) and high-voltage detection (HVD)

Before the BOD level threshold generates a reset, you might be warned by the configurable circuit for low-voltage detection (LVD) and high-voltage detection (HVD) use case. You can configure the trip point (detection level), which creates an interrupt for possible safety measures. This circuit can oversee faster transitions.

5.2.4 Overvoltage detection (OVD)

Overvoltage detection (OVD) circuit applies a device reset when V_{CCD}, V_{DDD}, or V_{DDA} supply goes above the maximum allowed voltage. This concept is a reverse of BOD circuit.

5.2.5 Overcurrent detection (OCD)

The overcurrent detection circuit monitors the current of the power supply rail V_{CCD} and detects whether the load current of a regulator is higher than expected. If the current is over the regulator limit, the OCD circuit generates a reset to protect the device.

5.2.6 Power domain voltage monitoring by the ADC

The ADC provides the option to monitor several power supply and ground pads. Instead of a reset, an interrupt is generated by the corresponding ADC unit. To keep the CPU load low, the range detection feature can be enabled to generate an interrupt only when a critical range is entered. The pads can be selected by a complex multiplexer structure as shown in **Figure 4**. For more details on this feature, see chapters *Analog Subsystem* > *SAR ADC* > *Reference Buffer* and *Resources Subsystem (SRSS)* > *Voltage Monitoring* > *Voltage Monitoring by ADC* in **Architecture TRM**.

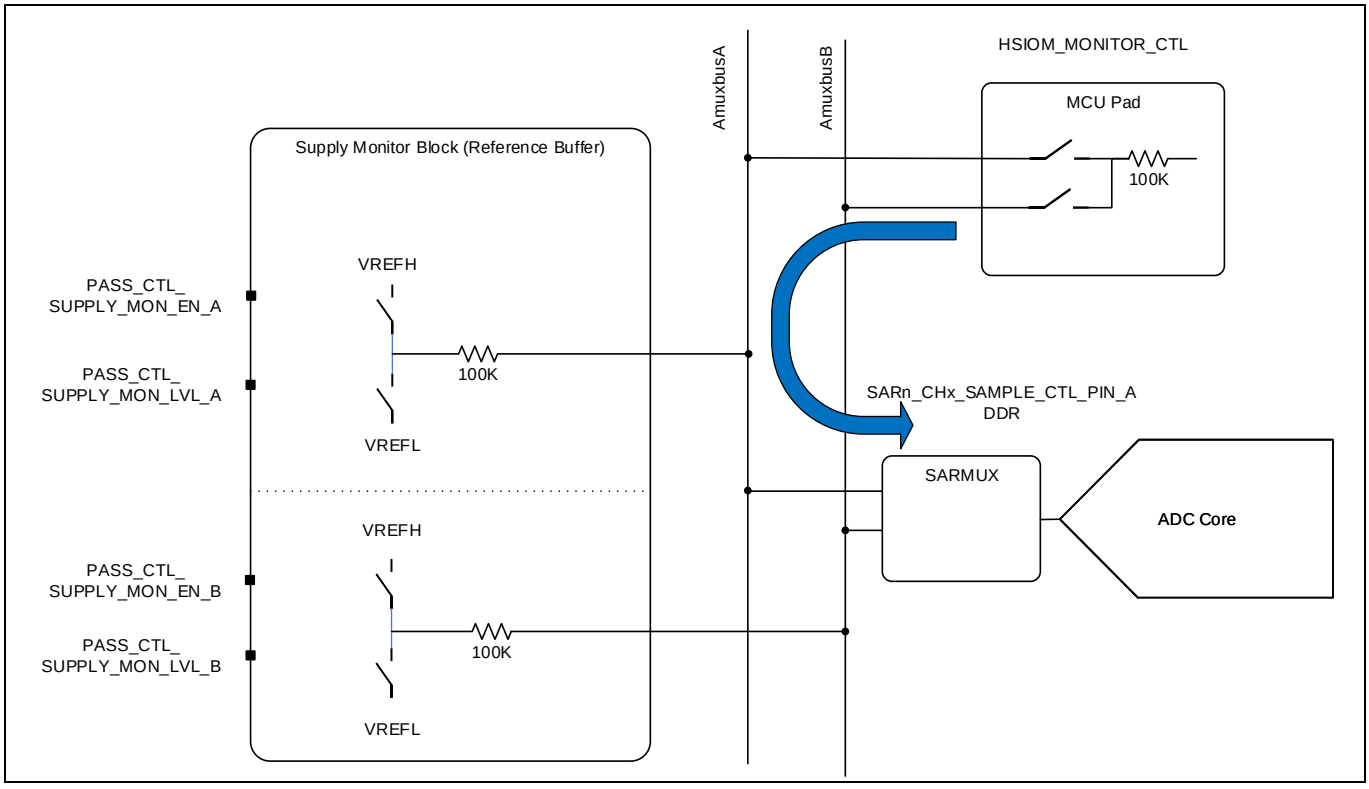


Figure 4 Block diagram of voltage monitoring with ADC

5.3 Watchdog reset

An internal watchdog timer (WDT) within the MCU supports a wide range of capabilities. This WDT circuit can also run in the Hibernate power mode (see “Device Power Modes” in **Architecture TRM**).

6 Ports and non-power pins

6.1 Port input/unused pins

6.1.1 General considerations

This section explains the different methods to handle unused pins and the advantages and disadvantages with respect to the MCU operation. In general, the risk of unused pins is floating inputs and a latch-up effect within the pin structure.

6.1.2 Open pin connection

During and after a POR, by default, the I/O pins are in a high-impedance (High-Z) analog state with disabled input buffers. The advantage of this method is that the current consumption of the MCU is lower when compared to the use of a terminal resistor; and the BOM cost is reduced. The disadvantage is that during an assembly option, a long signal trace is routed to the pin, and the signal trace can take effect as an antenna and a captured noise can cause a latch-up at the pin.

6.1.3 Direct connection to GND or power supply

The I/O pins should not be connected directly to GND or to power supply as the power supply traces can take effect as an antenna to the pin and the captured noise can cause a latch-up effect.

6.1.4 Internal pull-up/down resistor as termination

When there is a risk of a latch-up effect at an unused pin due to the board design (long traces of optional features), terminate the input pin using internal pull-up or pull-down resistance.

The advantage is low current consumption and BOM cost reduction compared to external termination resistors. The disadvantage is that you must configure the port pin state after the reset. Therefore, during reset caused by any disturbance (supply, clock issues, and so on), the internal termination is not available anymore and the system is again vulnerable to a latch-up effect. You can choose this method if there are unused pins without a long trace. In general, the pin state (enabled pull-up or pull-down resistor) must be unchanged when a low-power mode is entered. The reason is that for an external resistor, the internal termination must be available all the time.

6.1.5 External pull-up/down resistor as termination

An external termination resistor can be placed next to the unused I/O pin instead of using the internal ones. In case of an open signal line routed to the pin, any injected noise can be safely terminated even during the device reset. A resistor value between 2.2 kΩ and 10 kΩ can be used. However, you should not connect several unused pins to one common termination resistor because if the unused I/O pins unintentionally drive different output levels against each other, the I/O pins might be permanently damaged.

6.2 Dedicated port pins

For dedicated MCU peripherals, the unused I/O handling is explicitly considered. In most of these cases, the entire MCU peripheral including the power domain pins must be considered to avoid the risk of latch-up (LU). For more details on power domain pins, see **Unused power domains**.

Table 4 Handling of unused dedicated I/O Pins

MCU peripheral	Power domain	I/O pin	I/O function [IN/OUT]	Pin handling (Connect to ...)
Audio-DAC	VDDA_DAC	C_L, C_R	IN	GND
		DAC_L, DAC_R	OUT	(when Mono sound: Open Pin Connection of unused part)

6.3 Pins in lower-power mode

To achieve the lowest possible quiescent current in a low-power mode, the current consumption of I/O pins must be considered. Depending on the low-power mode, the configuration state and the last output state are frozen. In case of input pins, it is forbidden to have floating input levels, because the quiescent current of the MCU increases dramatically.

When an input pin is used as a wakeup pin, do not change the configuration under the assumption that the pin has an internal or external pull-up or pull-down resistor for termination. When an input pin is not required in a low-power mode, it can be configured to High-Z input with disabled input buffer. For details on different low-power modes, see the **Architecture TRM** and the corresponding application note listed in **Related documents**.

6.4 Latch-up considerations (switch)

Pressed switches usually cause a bouncing signal. This can damage the MCU port pin. As a countermeasure, debounce capacitors are deployed. Exercise caution with external switches to V_{CC} or ground together with debounce capacitors connected to port pins.

The following is a typical configuration.

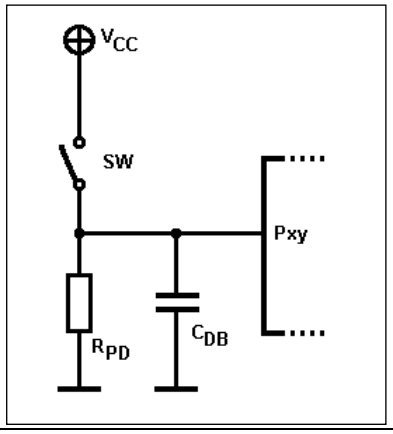


Figure 5 Principle switch circuit

R_{PD} is a pull-down resistor and C_{DB} a debounce capacitor. If the switch SW is open, a “0” is read from the port pin Pxy. When the switch is closed, the input changes to “1”.

From the physical aspect, the switch is often placed at a distance from the MCU by a cable, wire, or circuit path. The longer the circuit path is, the higher will be its inductivity LX (and capacity CX).

Figure 6 shows an equivalent circuit diagram.

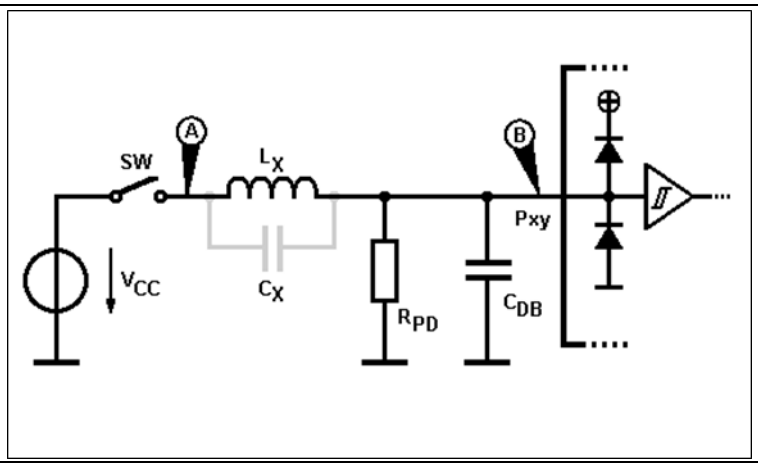


Figure 6 Equivalent circuit of the principal switch circuit

By closing the switch SW at time t_0, as shown in **Figure 7**, the voltage can be measured at point (A).

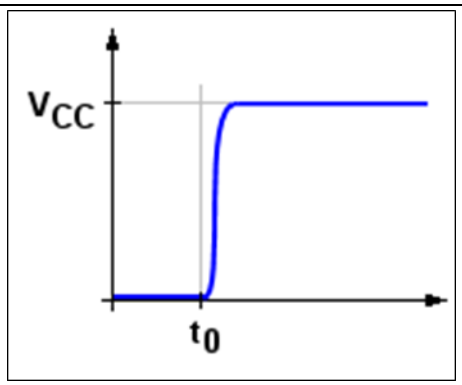


Figure 7 Signal rise after closing the switch at point (A)

However, at the port pin Pxy on point (B), as shown in **Figure 8**, the voltage can be measured.

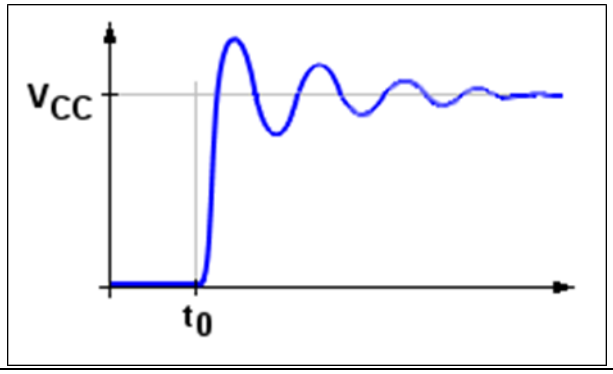


Figure 8 Signal rise after closing the switch at point (B)

By closing the switch SW, the circuit becomes a parallel oscillator with the wire inductivity L_X, debounce capacity C_X, and damping R_{PD} of the pull-down resistor (it is assumed that it is an ideal power supply; that is, it has no internal resistance).

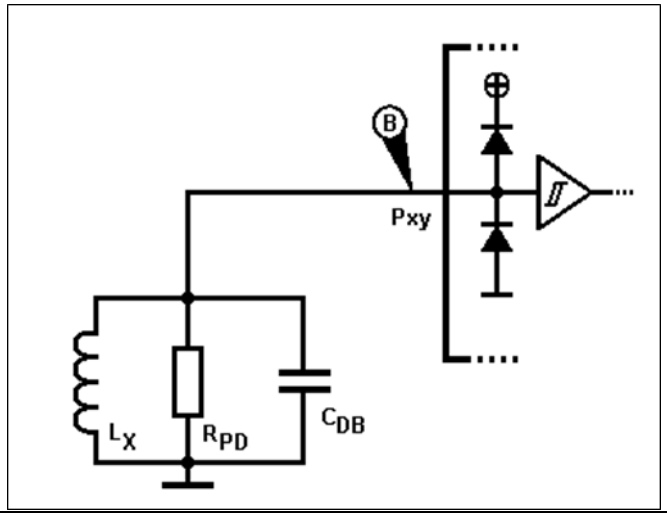


Figure 9 Equivalent circuit when the switch is closed

Because R_{PD} is often chosen as a high value (> 50 kΩ), its damping effect is weak.

This (weakly) attenuated oscillator causes voltage overshoots on the port pin (point (B)), as shown (in red) in **Figure 10**.

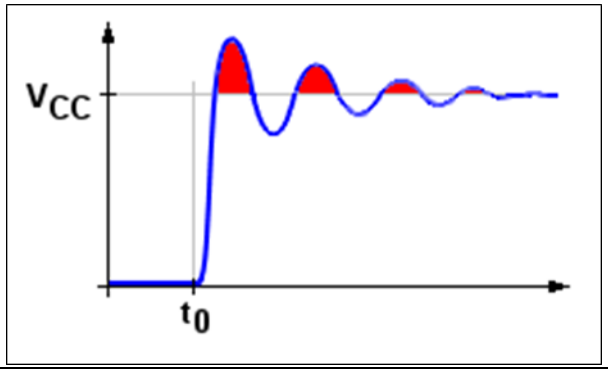


Figure 10 Signal overshoots on port pin after closing the switch

These overshoots may cause an internal latch-up on the port pin, because the internal clamping diode connected to the internal power supply becomes conductive. Similar is the effect if the switch SW is opened. In this case, there are under shoots on the port pin.

The frequency of the oscillation can be calculated by **Equation 1**.

$$f_{OSC} = \frac{1}{2\pi\sqrt{L_X C_{DB}}} \qquad \text{Equation 1}$$

The inductivity LX is an unknown value and depends on the PCB, its routing, and the wire length.

There are two counter measurements to prevent from latch-up.

6.4.1 Solution A: Decrease the debounce capacitor value

Decreasing the capacitance of the debounce capacitor increases the oscillation frequency; thus, the overall energy of the overshoots is lower.

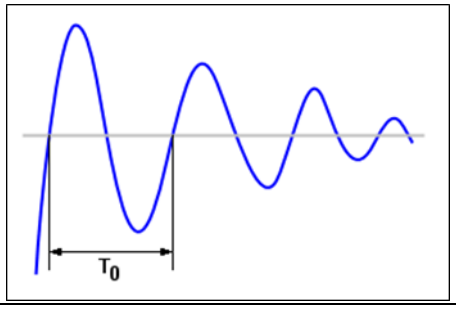


Figure 11 Bounce signal on the pin with a large capacitance

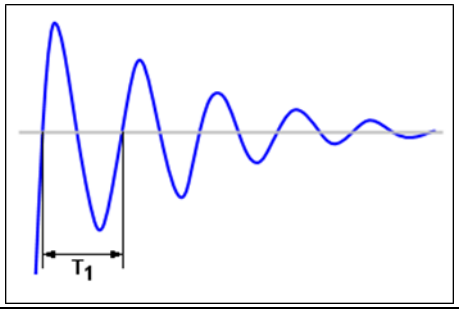


Figure 12 Bounce signal on the pin with a small capacitance

This solution has two disadvantages: the debounce effect decreases and there is no guarantee that the latch-up condition is eliminated.

6.4.2 (Recommended) Solution B: Use a series resistor

The recommended solution is to use a series resistor (R_S) at the port pin as shown in **Figure 13**.

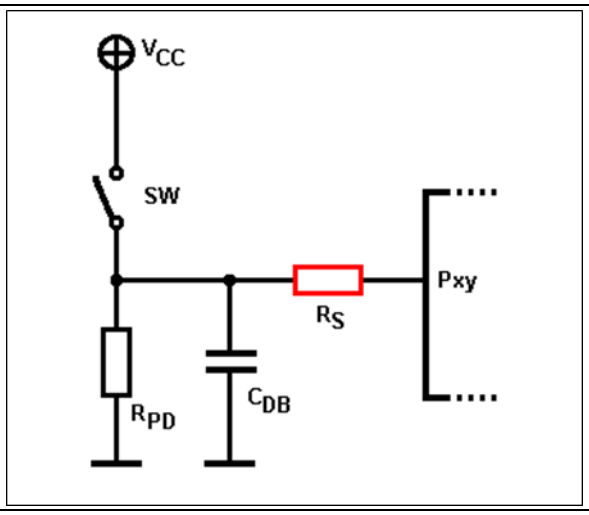


Figure 13 Recommended switch circuit with a series resistor

The series resistor R_S reduces the amplitude of the oscillation and decreases the voltage offset at first. Do not choose a too high resistor—otherwise, the port pin input voltage (V_P) will be below the high input level threshold of the dedicated port pin (for example, CMOS/TTL/Automotive level).

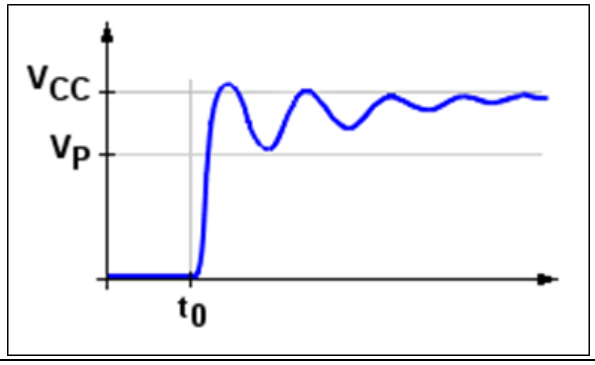


Figure 14 Reduction of the signal bouncing on the pin due to the series resistor

6.5 5-V-tolerant input pins

The MCU does not have 5-V-tolerant input pins if the corresponding I/O domain has a smaller voltage supply (for example, 3.3 V). If an I^2C bus system with 5 V is deployed, and if V_{DDIO} is supplied with 3.3 V, an external level shifter must be added to avoid the latch-up effect on the MCU pin.

6.6 Reset behavior of I/O port pins

During and after the power-on reset (POR), all GPIOs are in high-impedance analog state and the input buffers are disabled. During run time, GPIOs can be configured by writing to the associated registers. The DAP connection can be disabled or reconfigured for general-purpose use only after code execution starts.

6.7 Glitch filtering

The MCU provides the option of internal glitch filtering. As the glitch filters are not available on every port pin, the assignment of wakeup pins must be done with caution. Before assigning wakeup pins, check the number of available glitch filters in the device datasheet.

6.7.1 Analog filter

Every port group has one analog filter, which also works in DeepSleep mode. For details on AC characteristics, see the device datasheet.

6.7.2 Digital-based filter

The smart I/O module in the I/O system can implement one digital-based filter in dedicated ports. In DeepSleep mode, either the internal low-speed oscillator (ILO) or the external crystal oscillator (ECO) clock can be selected as the clock source (see **Clock sources**). This means that the minimum filter period is ~30 µs. Additionally, the current consumption increases because a clock is running. For more information, see the *Smart I/O* section in the "I/O System" chapter in the **Architecture TRM**.

See **Latch-up considerations (switch)** for the latch-up considerations when external filters are deployed.

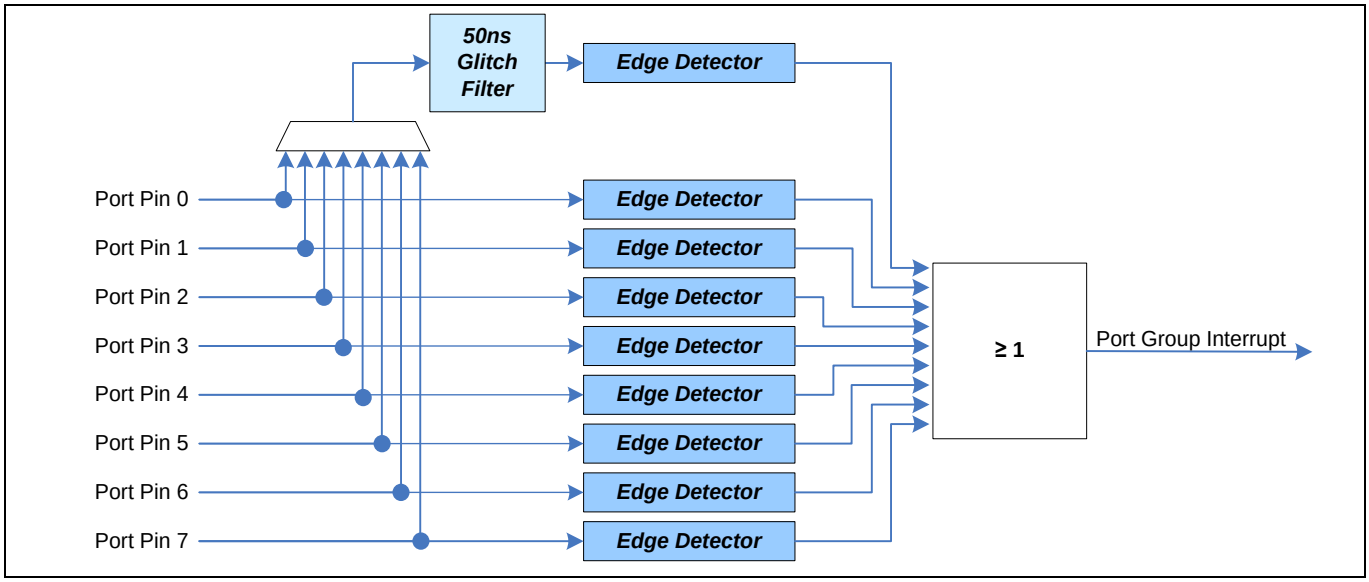


Figure 15 Port glitch filter and interrupt structure

6.8 Mode pin

A dedicated Mode pin is not required to enter the MCU into programming or normal run mode.

6.9 External interrupt input pins

In general, an external interrupt can be captured by edge detection on every general-purpose I/O (GPIO) port pin. See **Glitch filtering**.

Table 5 lists the wakeup sources in different power modes. For more details on the power modes, see the *Device Power Modes* section in the "System Resources Subsystem (SRSS)" chapter in the corresponding **Architecture TRM**.

Table 5 External interrupt/wakeup support in power modes

	External interrupt/wakeup in power mode			
Port pin function	**Active**	**Sleep**	**DeepSleep**	**Hibernate**
GPIO	X	X	X	–
Dedicated peripherals[3]	X	X	X	X
WAKEUP[4]	–	–	–	X

6.10 Clamping the structure of I/O pins with shared analog functions

It is important to identify the power supply domains that must have common supply level in each application. **Figure 16** and **Table 6** provide the overview of the clamping structure and the consequences when an analog input function is used on dedicated power domains. When any port pin of a dedicated power domain (PD) is applied as an analog input, the domain must have the same or lower voltage level than the analog supply VDDA_ADC. **Table 6** lists the special use cases.

[3]Source for the device and as a clock observation for internal clock signals

[4]Supported only a few pins

Ports and non-power pins

General

- Usually the I/O domain deployed (PD_1) is the same as PD_2, but in some cases, there are exceptions for PD_2.
- The power domain dependency PD_1 ≤ PD_2 is especially relevant, when PD_1 is a different power domain when compared to PD_2.
- When VDDA_ADC is only on PD_3, and as long as the pin input has not started to operate as analog input, PD_1 and PD_2 can be greater than VDDA_ADC. See also **Power ON/power OFF sequence of power supply domains**.

Note: Implementation of power rail voltage levels for the dedicated I/O domains and the ADC supply must be compliant with the other power sequencing requirements mentioned in the device datasheet.

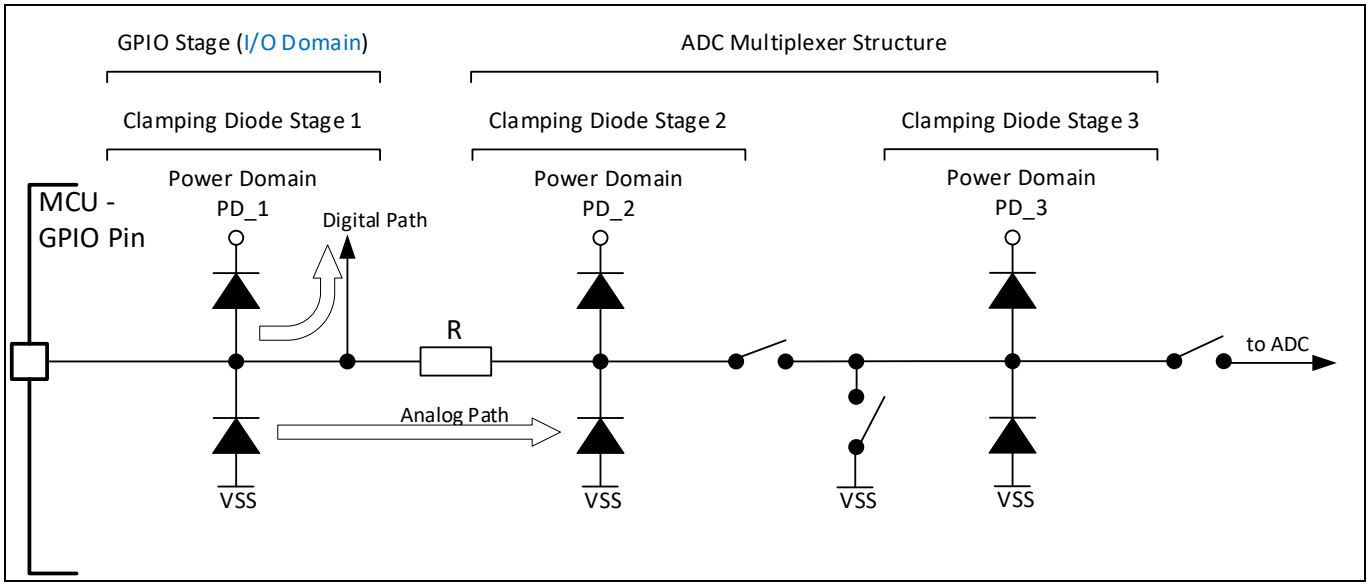


Figure 16 Clamping structure of I/O pins with shared analog functions

Table 6 Clamping structure of I/O pins with shared analog functions within XMC7000

PD_1 port pins used also as analog inputs	Clamping diode stages			Required voltage level of power domain PD_1/2 ≤ VDDA (same as VDDA)[5]
	Power domain PD_1 (GPIO stage)	Power domain PD_2 (ADC MUX stage)	Power domain PD_3 (SAR MUX stage)	
No (only digital)	VDDIO_1	VDDIO_1	VDDA	No
Yes	VDDIO_1	VDDIO_1	VDDA	Yes
No and Port P11 is **not** in use	VDDIO_2	VDDIO_2	VDDA	No
Yes	VDDIO_2	VDDIO_2	VDDA	No
Not on Port P11, but P11 is in use	VDDIO_2	VDDA	VDDA	Yes
Yes, on Port P11, but P11 is in use	VDDIO_2	VDDA	VDDA	Yes
No (digital only)	VDDD	VDDD	VDDA	No
Yes	VDDD	VDDD	VDDA	Yes

[5] Implementation of power rail voltage levels for the dedicated I/O domains and the ADC supply must be compliant with the other power sequencing requirements mentioned in the device datasheet.

6.11 External supply for core voltage

6.11.1 Requirements

- Applications with < 300 mA core current consumption can run with the MCU int. LDO.
- Applications with > 300 mA core current consumption need an external supply for the core voltage.

For the technical requirements of the DC/DC converter and details on how to use it, see AN226698 listed in **Related documents**.

Note: In AN226698, DC/DC converters are termed as PMIC, although only the core voltage regulation handling is considered.

6.11.2 Drive output current of “Enable” control pin

To control the “Enable” input pin of the external DC/DC converter, a dedicated output control pin on the MCU is available. Compared to a standard GPIO pin, the absolute maximum drive current is extremely limited. Therefore, for current limitation, a series resistor is necessary. Otherwise, this MCU control pin might be permanently damaged. For electrical specification, see the device datasheet.

6.12 Audio DAC

6.12.1 Implementation and features

The audio digital-to-analog converter (DAC) is an analog audio block inside the MCU and supports internal cascaded integrator–comb (CIC) filter, finite impulse response (FIR) filter, interpolation filter, and delta-sigma modulator for 10-bit resolution. Both OUT signals (DAC_L and DAC_R) are intended to connect with an external audio amplifier with external output load resistance > 20k and load capacitance < 100 pF. The DAC block consists of several power domains internally. The cut-off frequency of the third-order low-pass filter is 90 kHz. The noise-critical circuitry of the DAC is the VDDA of the analog part. The DC bias output voltage will be generated by internal voltage divider 131.6k/131.6k and external smoothing capacitor at the COM pin (C_{COM}), shown in **Figure 17**.

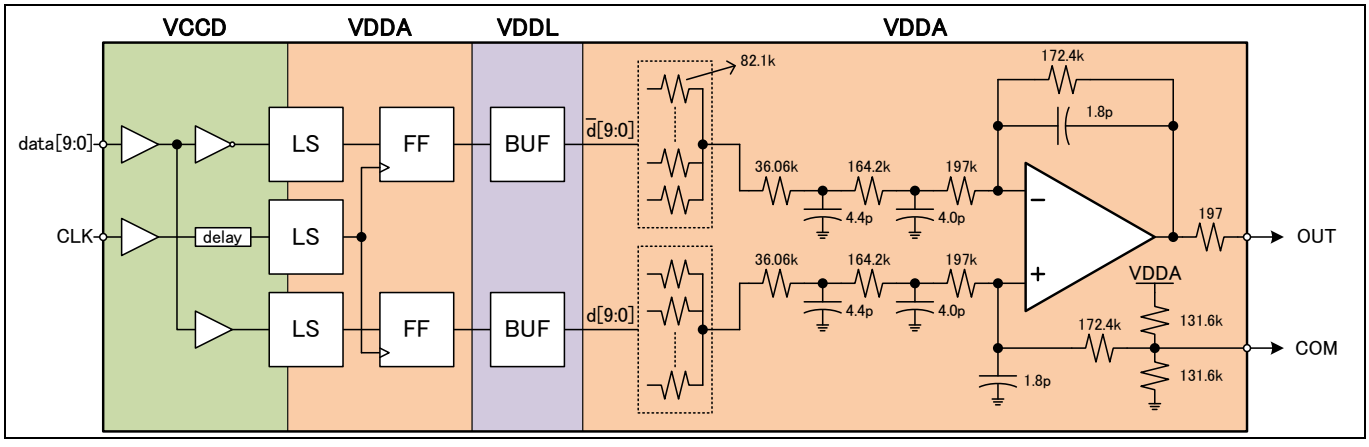


Figure 17 Block diagram of audio DAC output

As shown **Figure 18**, the startup time depends on the selected smoothing capacitor (C_{COM}) value and should be configured with the integrated fast start-up timer to 70 ms at 2.2 µF (low ESR). If a larger capacitor than 2.2 µF is

needed, the timer setting for the *FastRampCount* period and the *CompRampCount* period must be adjusted based on this refence value from the datasheet, as shown in **Figure 18**.

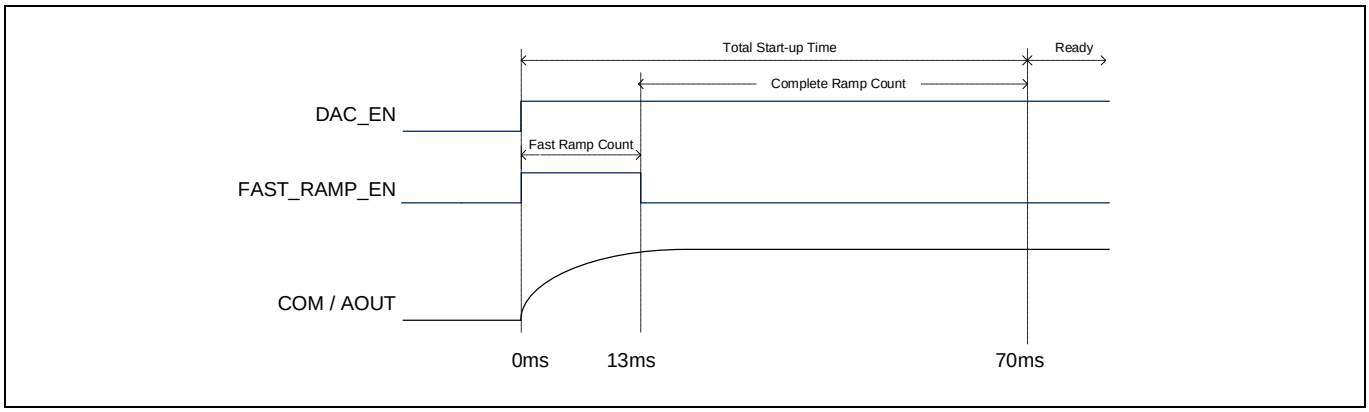


Figure 18 Audio DAC startup time

During the audio-DAC startup time, the external amplifier must be either powered down, or in mute mode (if mute mode is available). The typical COM capacitor value is 2.2 µF. For the typical case, the fast startup timer must be set to 13 ms to ensure that the audio DAC is ready in 70 ms. Maximum supported COM capacitor is 10 µF. For this case, the fast startup timer must be set to 60 ms. **Figure 18** shows the relationship between DAC_EN, FAST_RAMP_EN, and how the COM output behaves during startup.

6.12.2 Power domain filter

The analog block of the audio DAC, which corresponds to the internal “VDDA” block in **Figure 17**, is very noise-sensitive. Each noise on its supply can be heard directly on the audio output. Therefore, either of the following possibility is recommended to create a silent supply at the VDDA_DAC/VSSA_DAC power domain pins:

- Low drop-out (LDO) linear regulator
- Low-pass filter (LPF) for the 3.3-V supply

If using a common 3.3-V supply for digital and analog parts of the application, the potential noise sources listed in **Table 7** must be considered. In this case, a power supply filter in **Figure 19** is recommended for the 3V3 audio power domain.

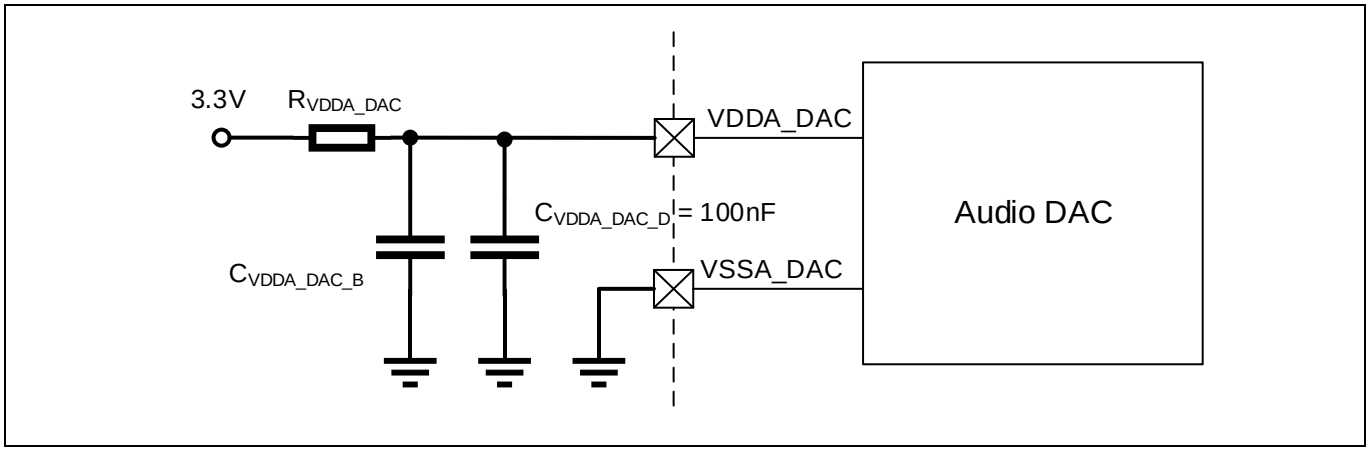


Figure 19 Power supply filter (LPF) for audio DAC

Table 7 Potential noise sources on the 3V3 audio power domain

Domain	Frequency range	Comment
Audio	100 Hz ... 20 kHz	Audio
DC-DC converter (switching regulator)	300 kHz ... 2.2 MHz	Switching frequency
	< 100 kHz	Response time
FPD-Link (I/O domain)	32 MHz … 110 MHz	Bus speed; equivalent frequency range of transitions are not considered
Memory interface	50 MHz … 133 MHz	
Ethernet	50 MHz … 125 MHz	
Communication interface	1 MHz … 10 MHz	

6.12.2.1 Low-pass filter calculation

Figure 20 shows a simple RC LPF for the power supply of audio DAC, which is the responsibility of the user.

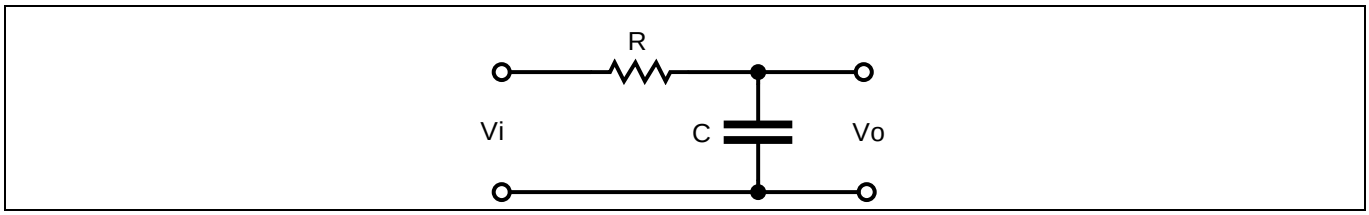


Figure 20 RC low-pass filter (RC LPF)

The cut-off frequency of the filter can be calculated with **Equation 2**.

$$a = \frac{Vi}{Vo} = \frac{1}{\sqrt{1 + (2\pi fRC)^2}} \qquad \text{Equation 2}$$

$$fc = \frac{1}{2\pi RC}$$

Note: RC-Filter −6 dB per octave corresponds to 20 dB per decade.

Equation 3 shows an example calculation for RC low-pass filter.

$$fc(-3dB) = \frac{1}{2\pi * 10\Omega * 10uF} = 1.592\text{kHz} \qquad \text{Equation 3}$$

Table 8 shows the calculated cut-off frequency of the LPF. Default values: C =2.2 µF and R = 10 Ω

Table 8 LPF cut-off frequency

R[Ω]	10	1	0.3
C[µF]	f3dB[kHz]	f3dB[kHz]	f3dB[kHz]
10	1.59	15.9	53.1
4.7	3.39	33.9	112.9
2.2	7.2	72.3	241.1

R[Ω]	10	1	0.3
1	15.92	159.2	530.5
0.47	33.96	338.6	1128.8
0.22	72.34	723.4	2411.4
0.1	159.15	1591.5	5305.2

Table 9 LPF DC power drop estimation

IDD[mA] (SID1318)	R[Ω]	Vdc[mV]
3.2	10	32
	4.7	15.04
	2.2	7.04
	1	3.2
	0.8	2.56
	0.5	1.6
	0.3	0.96
	0.1	0.32

There is an estimated IR drop on the power domain pin, VDDA DC, as shown in **Table 9**, due to the series resistor (Rfilter). The reduction of the series resistor (Rfilter) of the LPF impacts the cut-off frequency. As an alternative for the resistor, a ferrite bead with Rdc ≤ 300 mΩ is recommended. See the example in **Appendix F - Power supply filter characteristics**.

*Note: In the application, to connect to the speakers, small series capacitors are added to the output pins DAC_L/R, as shown in **Figure 22**. This HW setup is not in contradiction to the parameters RL and CL of SID1300 (see **Table 10**). These parameters belong to the test circuit as shown in **Figure 21**.*

Note: For the correct values, see the device datasheet.

Table 10 Audio DAC output load and C_{COM} specification

SID1300	f_{CLKDA0}	System clock frequency	2.048	–	18.432	MHz	All parameters specified f_S = 44.1 kHz, system clock 256 × f_S and 16-bit data, R_L = 20 kΩ, C_L = 100 pF, unless otherwise noted
SID1301	f_S	Sampling clock	8	–	48	kHz	
SID1302	R_L	Analog output load resistance	20	–	–	kΩ	DAC_L, DAC_R
SID1303	C_L	Analog output load capacitance	–	–	100	pF	DAC_L, DAC_R
SID1304	C_{COM}	Com Capacitance	2.2	–	10	µF	C_L, C_R
SID1305	V_{OUT_MAX}	Analog output single-end output range (±full scale)	0.655 × V_{DDA_DAC}	0.673 × V_{DDA_DAC}	0.690 × V_{DDA_DAC}	V_{P-P}	DAC_L, DAC_R, R_L = 20 kΩ, C_L = 100 pF
SID1306	V_{OUT_ZERO}	Analog output voltage (zero)	0.49 × V_{DDA_DAC}	0.5 × V_{DDA_DAC}	0.51 × V_{DDA_DAC}	V	DAC_L, DAC_R

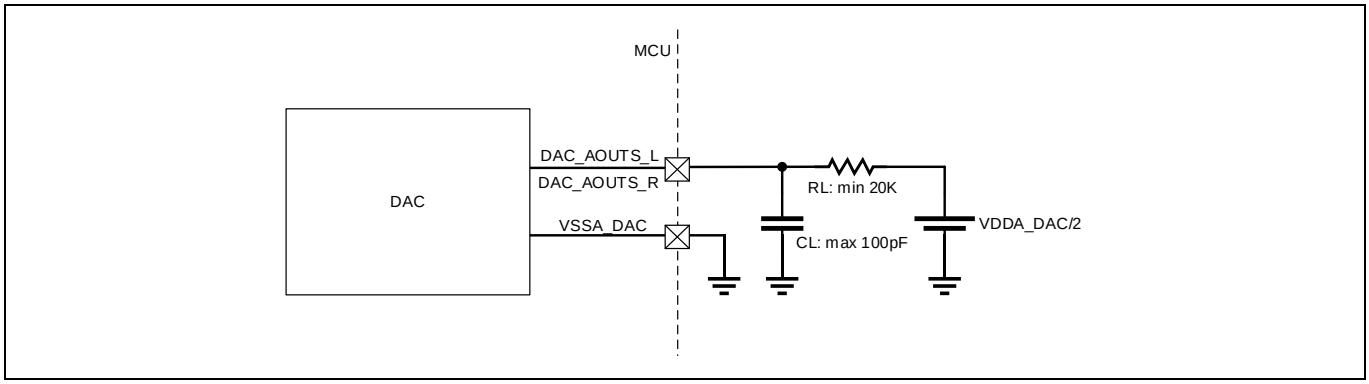


Figure 21 DC coupling connected to VDDA_DAC/2 (test circuit)

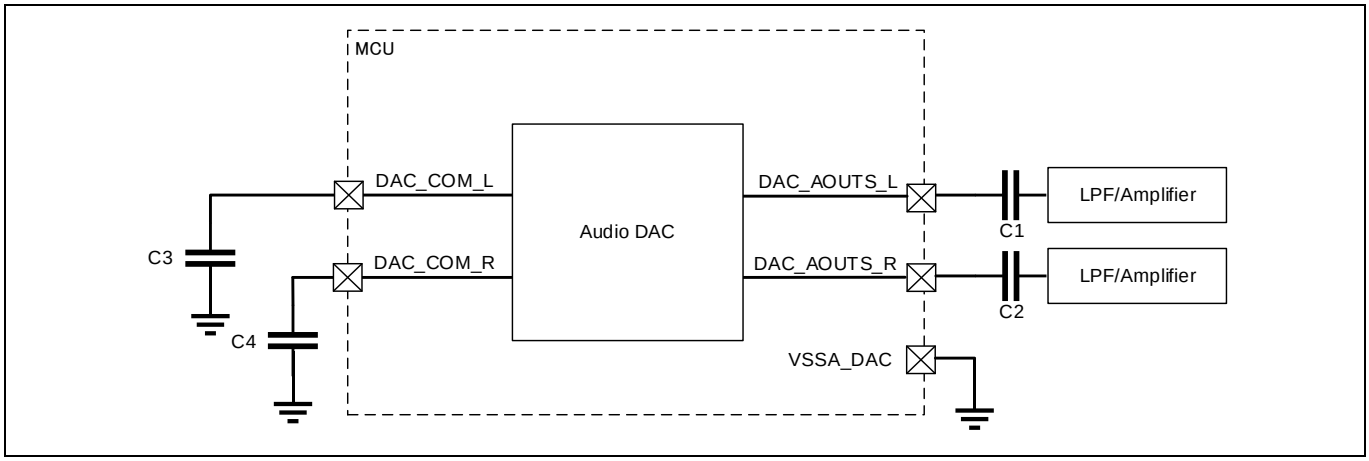


Figure 22 AC coupling connected to LPF and amplifier (application example)

Capacitors:

- C1, C2: 10nF–10 µF AC coupling capacitor
- C3, C3: 2.2 µF–10 µF low-ESR capacitors

6.12.3 Unused audio DAC

When the audio DAC is not used in the target system or is used only as mono sound output, the related audio DAC pins are handled as described in **Unused power domains** and **Dedicated port pins**.

.

6.12.4 Avoiding pop noise at the speaker output

The audio DAC and external amplifier will generate a pop noise when a high-to-low or low-to-high transition occurs on the DAC_EN bit of the DAC0_IF_CTL register during power up or power down.

An external circuitry as shown in **Figure 23** and **Figure 24** is recommended to suppress such pop noises. During audio DAC startup, the external amplifier must be either powered down or in mute mode (if mute mode is available).

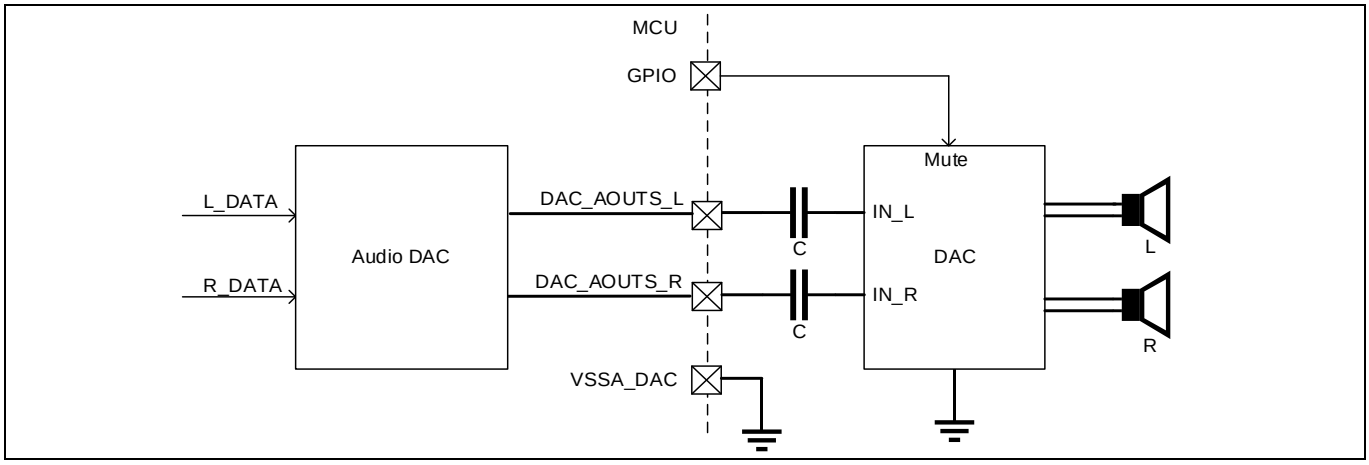


Figure 23 Audio DAC with single-end mono/stereo output

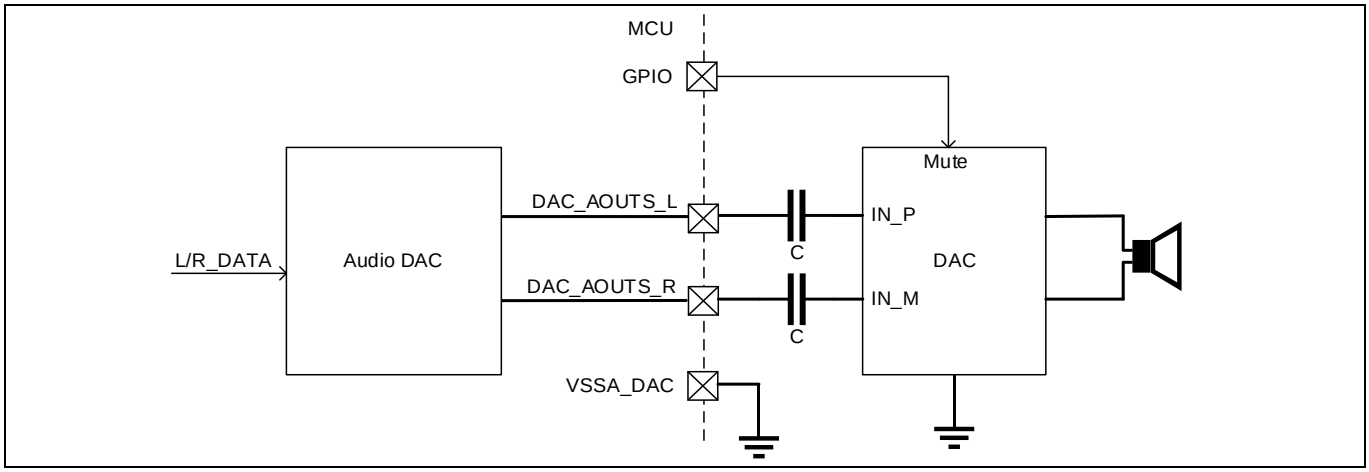


Figure 24 Audio DAC with differential mono output

7 Flash programming connections

Flash programming can be done with the JTAG/SWD connection; therefore, no mode pins are available to switch the device into a programming mode after power-on reset. See **Debug interface** for information on the debug connections. There is also the option to use dedicated CAN channels for mass production programming.

8 Debug interface

There are several options to connect the debug system to the MCU depending on the debug requirements and the tool chain support. The following are the debug connectors:

- Legacy 20-pin IDC JTAG connector
- 10-pin Cortex® debug connector
- 20-pin Cortex® Debug+ETM connector

In all these connectors, the JTAG and SWD signals are shared. The differences are indicated by marking the Serial Wire Debug (SWD) protocol signals in blue. For more information on the interface signals, see Chapter 11 of the **CoreSight Components Technical Reference Manual**. A short overview is given in **Table 11**.

Table 11 Overview of SWD and JTAG interfaces

Item	JTAG	SWD
Pin count	4	2
Functionality	Programming Debugging Boundary Scan	Programming Debugging
Topology	Daisy chained	Star
Extra features	N/A	Print out debug info

8.1 Legacy 20-pin IDC JTAG connector

The legacy JTAG interface is used for flash programming and debugging. The JTAG signal RTCK is not available on the MCU. Additionally, the SWD signals can be shared.

Note: The JTAG interface terminates in a 20-way, 2.54-mm pitch IDC-connector (for example, Hirose HIF3FC-20PA-2.54DSA).

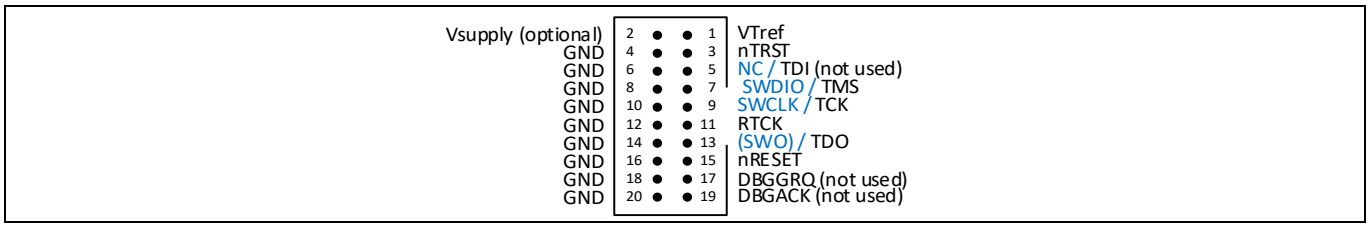


Figure 25 Legacy 20-pin IDC JTAG connector

8.2 10-pin Cortex® debug connector

To use the SWD debug interface, a 10-pin MIPI connector is defined with the minimum number of signals that are required for debugging. The JTAG interface signals are replaced by the bidirectional data signal (SWDIO) and the clock signal (SWCLK). The freed up TDO signal can be reused as a system trace data output serial wire output (SWO).

Debug interface

Note:

1. *For SWD debugging, a 10-way connector with 1.27-mm pitch is applied (for example, Samtech FTSH-105-01-L-DV-K).*
2. *Position 7 (KEY) has no pin and serves only as a key to properly orient the connector..*

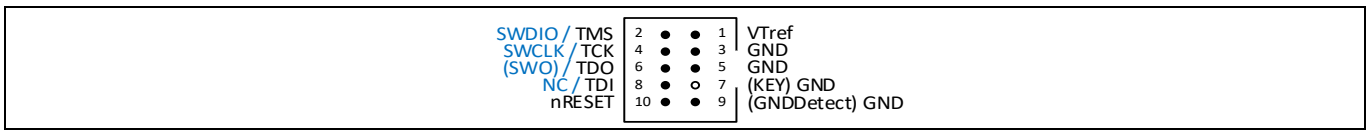


Figure 26 10-pin Cortex® debug connector

8.3 20-pin Cortex® Debug+ETM connector

Besides JTAG debugging and SWD debugging, this connector is used to connect a signal trace probe for the Embedded Trace Macrocell (ETM) instruction trace operations.

Note:

1. *As a connector, a 20-way, 1.27-mm pitch IDC connector is applied (for example, Samtech FTSH-110-01-L-DV-K).*
2. *Position 7 (KEY) has no pin and serves only as a key to properly orient the connector.*

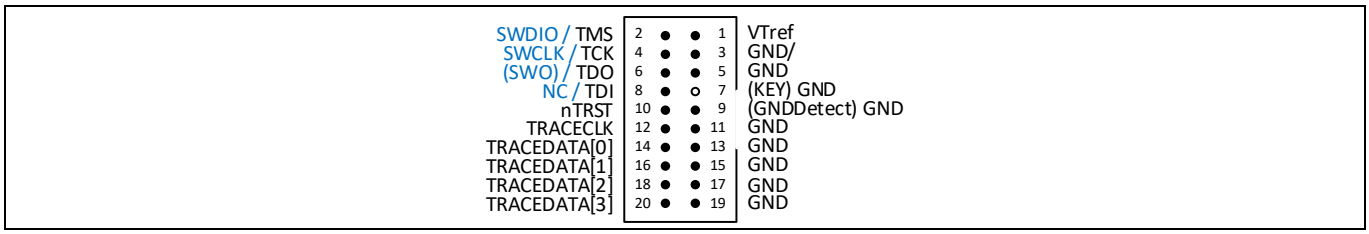


Figure 27 20-pin Cortex® Debug+ETM connector

8.4 Termination resistors

In general, the debug connection needs termination resistors for a proper communication. External termination resistors should not be required for this MCU, because by default, after power-on reset, the JTAG interface is enabled in the boot ROM. If externals are applied on the board, each external signal termination must in the same direction as is done in the device implementation. Although the JTAG interface is enabled by default after reset, the SWD mode can be enabled afterwards by establishing the SWD connection.

Table 12 Termination resistor for debug interface

JTAG mode	SWD mode	Signal	Required termination resistor (If N/A in the MCU)	MCU implementation
TCK	SWCLK	Clock into debug core	10 k–100 kΩ pull-down resistor to GND	Pull-down resistor
TDI	-	JTAG Test Data Input	10 k–100 kΩ pull-up resistor to V_{DDIO}	Pull-up resistor
TDO	SWO (optional)	JTAG Test Data Output, SWD Trace Data Output	10 k–100 kΩ pull-up resistor to V_{DDIO}	None. Termination, push-pull driver implemented.

Debug interface

JTAG mode	SWD mode	Signal	Required termination resistor (If N/A in the MCU)	MCU implementation
TMS	SWDIO	JTAG Test Mode Select, SWD Data In/Out	10 k–100 kΩ pull-up resistor to V_{DDIO}	Pull-up resistor
nTRST	-	JTAG TAP reset (active LOW)	10 k–100 kΩ pull-up resistor to V_{DDIO}	Pull-up resistor
GND	GND	Connection to system ground	-	-

Figure 28 and **Figure 29** show how to connect the debug connector to the MCU. In general, it is recommended to place a series resistor (R16) closer to the connector to avoid reflections and ringing of the debug clock signal. Otherwise, with strong oscillations during the level settlement, the debug interface can interpret the wrong data. Keep in mind that due to the internal termination resistor, a possible voltage divider in the debug clock signal might be created.

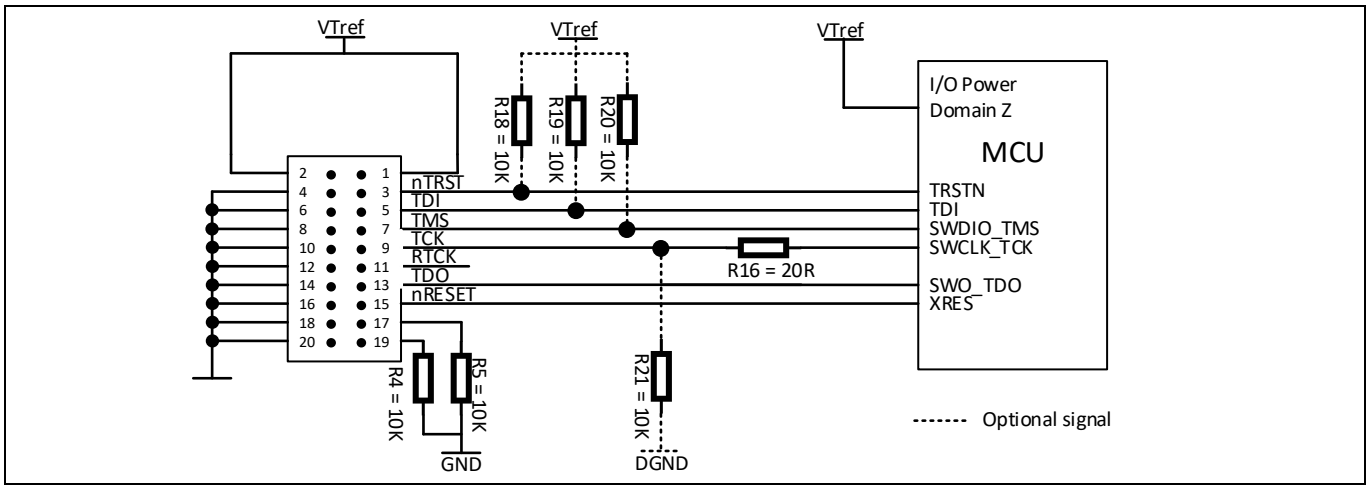


Figure 28 JTAG debug connection to the MCU with 20-pin IDC connector

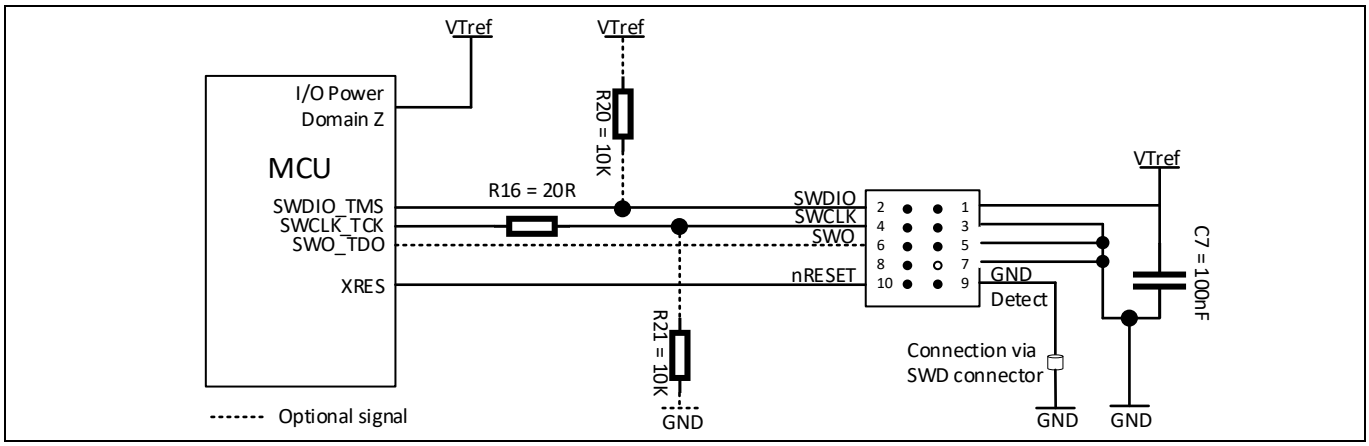


Figure 29 SWD debug connection to the MCU with 10-pin MIPI SWD debug connector

Debug interface

Note:

1. *When SWD is used as the debug interface instead of JTAG, there is a time slot after reset and in between boot ROM and user pin configuration in which the unused JTAG pins are configured according to JTAG communication. When these unused JTAGs pins are used in an application, make sure that the peripherals on the ECU are not affected in an unintended way.*
2. *It is recommended to check the debug connection that is supported by the vendors for flash programming and debugging. Also, check for the target board supply and supported power supply level of the vendor's hardware. Use an adaptor if power supplies do not match.*
3. *Boundary scan is supported only on JTAG interface, not on SWD.*

9 Clock output function

Cross-check the MCU internal clock signals for evaluation purposes with the following options:

- EXT_CLK port pin
- Alternate output function pin

9.1 EXT_CLK port pin

Internal clocks can be routed through a divider to the alternate function port pin EXT_CLK as the clock output function. Keep in mind that the macro Event Generator (EVTGEN) and EXT_CLK are driven by the same internal clock signal CLK_HF1. So, when the divided ECO signal is observed at the EXT_CLK pin, the EVTGEN is also driven with the ECO clock accordingly; this might have an impact to the application. The EXT_CLK pin is a bi-directional pin and can also be used as an external clock source. See **Clock sources** for more information about this pin.

As the MCU clock output functionality drives the fast digital signal, this signal must be routed far away from the analog input and the analog voltage reference signals.

9.2 Alternate function pin

System clocks can be implicitly observed by using a PWM signal coming from a TCPWM output channel, for example. Keep in mind that each TCPWM channel input clock is derived from a dedicated clock divider of the peripheral clock. See the “Clocking System” chapter in the **Architecture TRM** for more details on the clock tree.

10 Layout and electromagnetic compatibility

10.1 General

To avoid ESD problems and noise emission of the system, consider some rules for the layout design.

The most critical point is the VCCD pin, as this is the connection to the internal supply for the MCU core. The required decoupling capacitors (DeCaps) must be placed as close as possible to this pin. Typically, a bigger buffer or bypass capacitor of µF range is added to the dedicated power domain to bypass the period of time until the capacitors are recharged again. Otherwise, DeCaps and subsequently the system may fall below the power supply operating range.

As the MCU has different digital supply rails, the routing of power supply traces must be done carefully. The supply traces should be routed in a star shape or as digital plane in the middle layer. A digital ground plane in the middle layer or on the mounting side just under the MCU is recommended. Decoupling capacitors should be placed as near as possible to the related pins. Placing these capacitors too far away make them ineffective. If possible, all decoupling capacitors should be placed on the same mounting side as the MCU. Alternatively, the DeCaps could be placed on the bottom layer below the paired power supply pins (for example, VDD/VSS pair).

The analog supply should be decoupled from the digital supply; the common ground star point should be as far as possible from the MCU. In hardware design, make sure that no latch-up effect occurs between the digital and analog supply or between analog and digital ground. Therefore, the impedance between the different VSS pins and between analog ground and analog reference input must be as low as possible.

10.2 Power supply pins

All power supply pins, listed in **Table 2**, are EMC-critical pins, DeCaps are required to ensure the correct operation of the MCU. See **General** regarding recommendations for the placement of the DeCaps.

10.3 Ground and power supply

For a multi-layer PCB, the power supply rails and ground should be routed as a plane in the inner layers of PCB. In a layer stack with several power supply planes, these planes should not overlap to avoid noise coupling.

Here are some recommendations for good EMC behavior:

- Use a multi-layer PCB
- Use power supply planes (ground and power) in the inner layer of the PCB layer stack.
- Place one or two decoupling capacitors close to each corresponding supply pin pair to reduce possible radiation.
- Use capacitor groups to match the frequency behavior of power supply decoupling. Decoupling capacitors can have values between 1 nF and 10 µF.
- Make sure that only one common star point connects analog and digital ground planes to each other. To have lower noise on the analog part, the star point should be placed as far as possible from the MCU and as close as possible to the voltage regulator capacitor with respect to the Electronic Control Unit (ECU) connector.
- Make sure that the digital and analog planes do not overlap and interfere. Furthermore, there should be no signal plane between these planes.
- Shield the analog input signals by the analog ground as much as possible.
- Avoid ground loops.
- Make sure that the supply traces with a layer changeover have at least two vias.

Figure 30 shows an example of a bad PCB layer stack, which may have crosstalk between different power supply planes. On the other hand, **Figure 31** shows an example of a well-designed PCB layer stack in which the analog and digital supply planes are separated in the common layer. Thus, the EMC behavior of the board is improved.

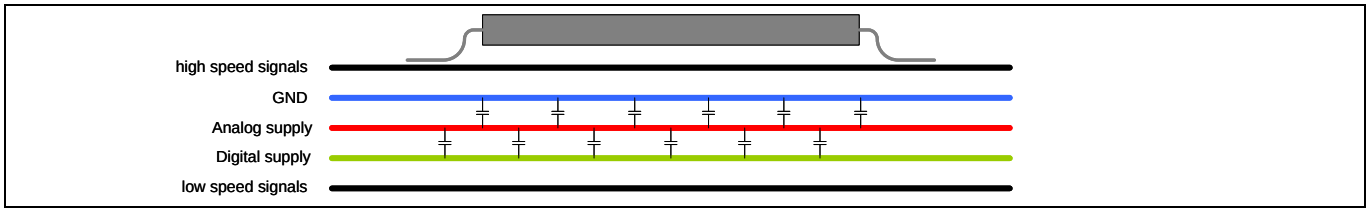


Figure 30 Example of a bad PCB layer stack

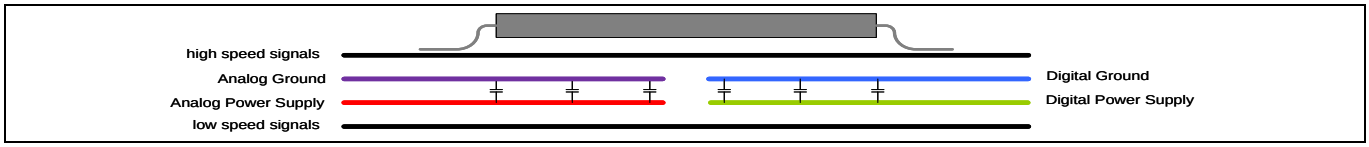


Figure 31 Example of a good PCB layer stack

10.4 Power supply decoupling

10.4.1 Placement

In general, the DeCaps should be placed as close as possible to the MCU. When a small ceramic capacitor is used together with a large electrolytic capacitor for decoupling, place the ceramic capacitor closer to the MCU power supply rail than the electrolytic capacitor.

DeCaps for power supply must be placed within the current flow. If not, they are ineffective because their function becomes less efficient as shown in **Figure 32**. As the description is valid for generic use as shown in **Figure 32** to **Figure 34**, the generic naming convention for power supply pins is VCC and for ground pins is VSS.

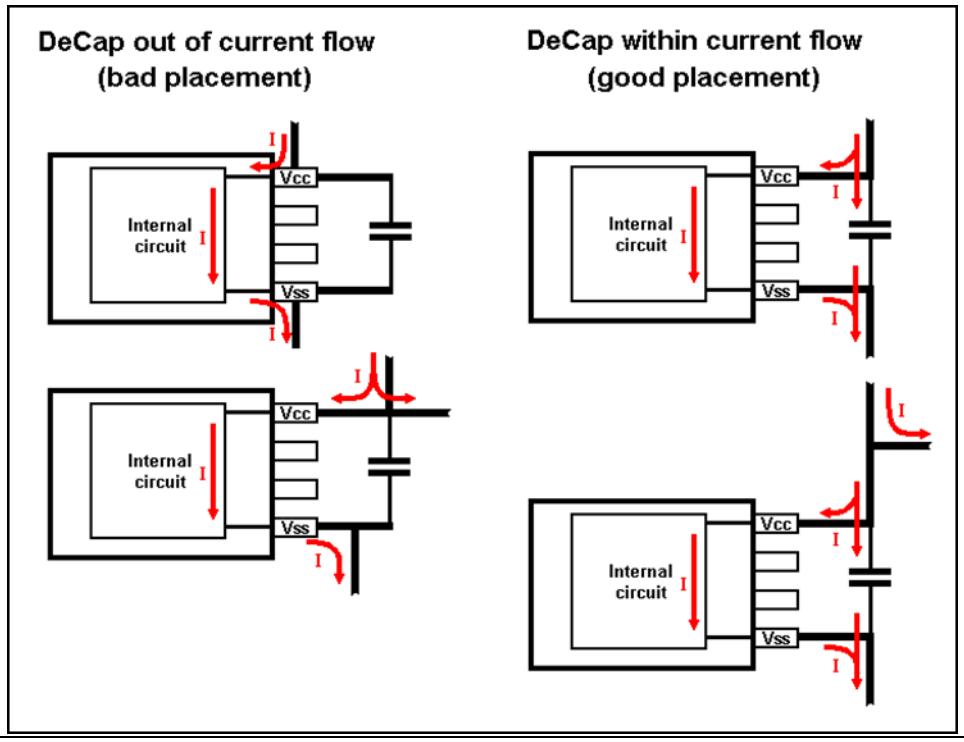


Figure 32 Power supply decoupling capacitor placement

Typically, the noise current should flow through the soldering pad of the decoupling capacitor CB. **Figure 33** shows the recommended routing and placement on the boards.

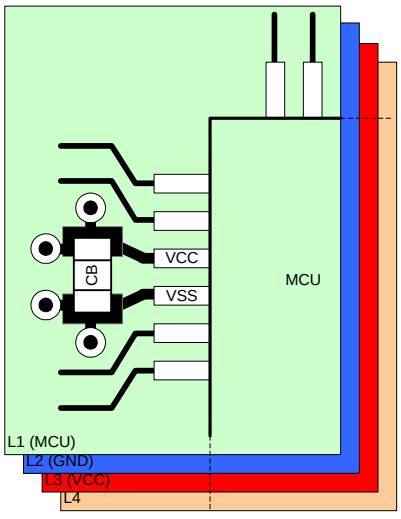


Figure 33 Recommended power supply decoupling on boards

Figure 34 shows an alternative, but not recommended routing and placement. Note that the capacitor is placed on the opposite PCB side like the MCU. This solution is the best for a high-density board assembly.

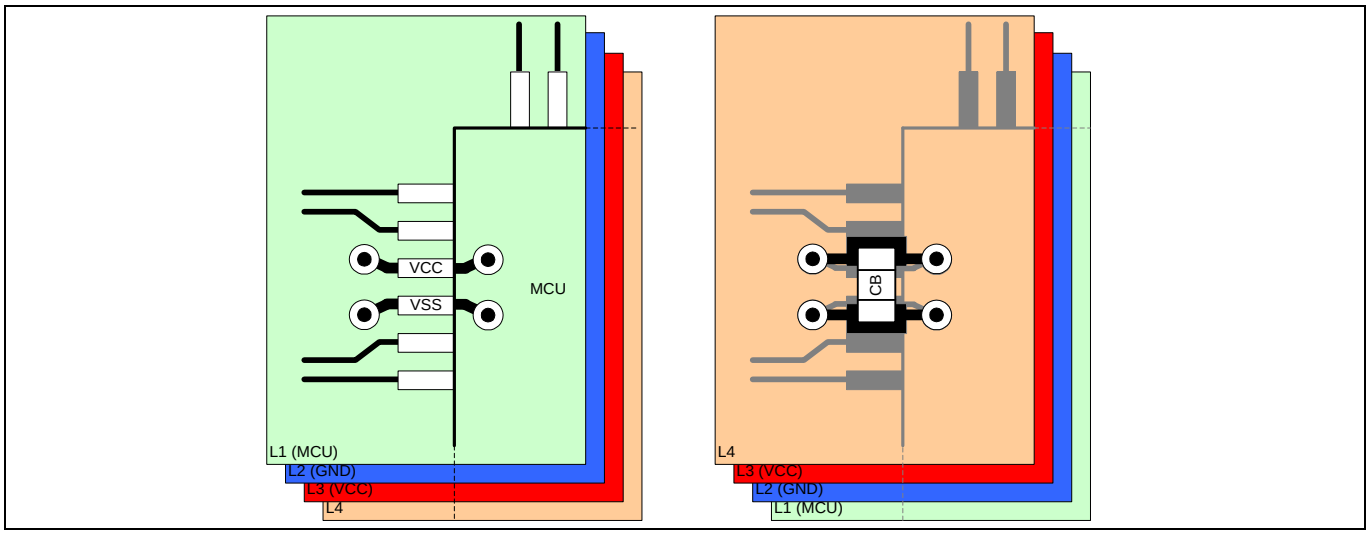


Figure 34 Alternate power supply decoupling on boards

10.4.2 I/O domains

The dimensioning of the DeCaps and bypass capacitors for the I/O domain is application-specific. The following are some points to be considered while dimensioning:

- How is the switching behavior (periodic or random) of the output stages and what is the transition requirement?
- How many outputs have the same transition at the same time during the running operation or after any wakeup or reset?
- How big is the capacitive load at one output pin?
- What is the selected driver strength configuration?
- Is there any DC current caused by resistors, which might be also buffered by a large bypass capacitor?

It is strongly recommended to make either a Power Distribution Network (PDN) analysis with an according model (IBIS or lumped model) or test on the PCB. A simplified consideration about the decoupling is provided in **SRAM Board Design Guidelines**.

10.5 Quartz crystal placement and signal routing

The MCU provides two Pierce oscillators implemented with an embedded feedback resistor (Rf) for the ECO and external watch crystal oscillator (WCO). You can enable both oscillators by software. That means the MCU starts the boot process from an internal clock source.

*Note: **Figure 35** to **Figure 38** showing the implementation of oscillators in the family and trimming features discussed in this application note might differ from the dedicated device **architecture TRM**. Due to different trimming features, external BOM cost can be reduced in the ECU design.*

10.5.1 Setup

Figure 35 shows the principle of an external oscillator circuit. The feedback resistor (Rf) is required to make the inverter act as an amplifier. Optionally, a damping resistor (Rd) is required for drive level (DL) reduction. If the DL is too strong, the crystal can be damaged over life time. The load capacitance C_L is the terminal capacitance

and is connected to the crystal. Thus, C_L includes the external capacitors C1 and C2 and the stray capacitance C_S. C_S comes from the PCB layout, the manufacturing tolerances, and the oscillator MCU pins. As the stray capacitance is usually ~4 pF for each signal line, the value of both load capacitors (C1 and C2) should be determined with a crystal matching test. The crystal matching test must always be done by the crystal manufacturer when there is any change on the target board affecting the oscillator circuit.

Load capacitance C_L

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_S$$

Equation 4

Note:

1. *The oscillator pins are shared with standard GPIO pins, which automatically leads to additional load capacitance in the oscillator circuit. This must be considered with regards to external load capacitors.*
2. *For details on crystal trimming, see AN230194.*

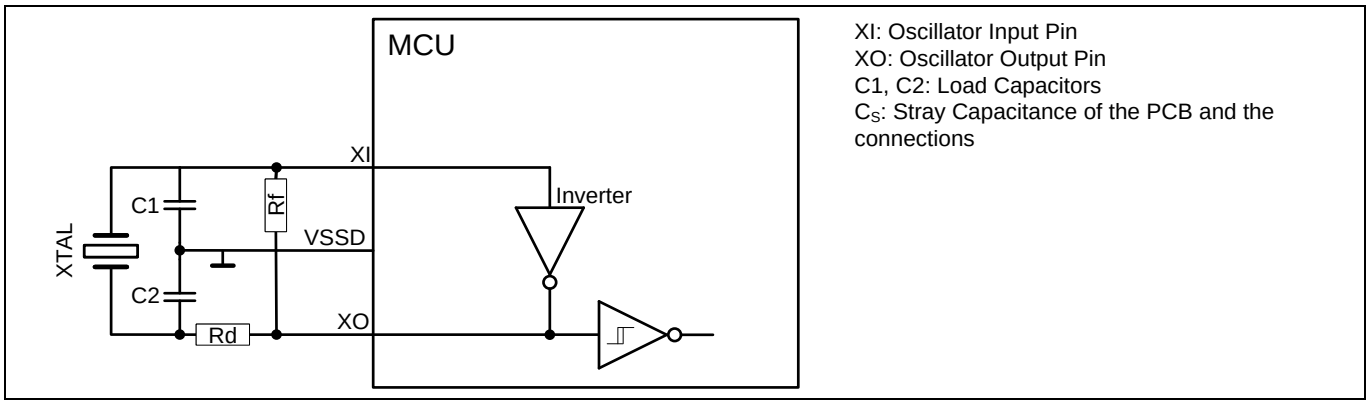


Figure 35 Principle setup of an external oscillator circuit

The ECO design is optimized for BOM costs reduction (see **Figure 36**). This is realized by a scalable DL and an embedded Rf implementation. By trimming features, a broad crystal frequency range can be supported. For more details, see the “Clock Sources” section in the **Architecture TRM**.

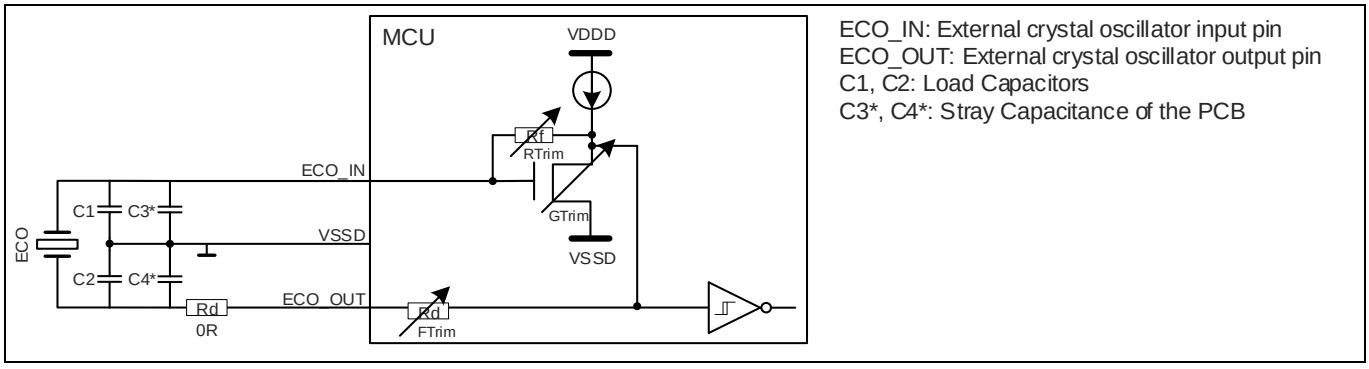


Figure 36 ECO circuit scheme[6]

[6] Figure might differ from dedicated Architecture TRM. Trimming features are not covered 100%.

The WCO implementation scheme is shown in **Figure 37**. Like in the ECO, Rf is embedded to reduce the external BOM cost. An external Rd might be required to avoid a damage of the external watch crystal.

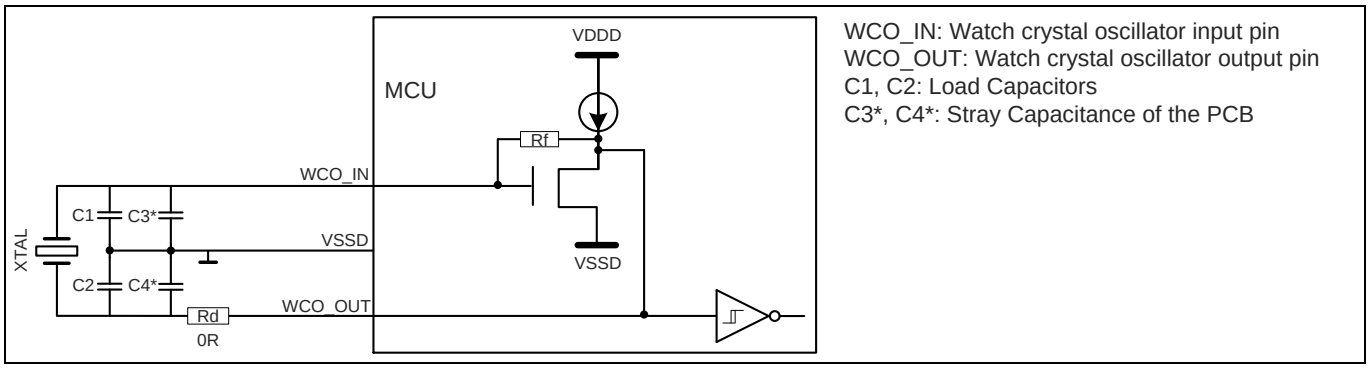


Figure 37 WCO circuit scheme[6]

10.5.2 PCB design

To reduce the impact of the EMI, the placement of external oscillator components and signal routing must be done carefully. The following items should be considered during the PCB layout. Due to design constraints, it might be required to make a tradeoff between the items.

- Stable frequency
  - Place the external oscillator components on the MCU layer.
  - Place the external oscillator components as close as possible to the MCU.
  - Make sure that the connection of the load capacitors C1 and C2 to the oscillator ground is in a common star point.
  - Make sure that there is no signal line between both capacitor ground connections.
  - Do not use vias for ground signal routing.
- Noise injection
  - Use a ground layer directly below the MCU.
  - Use a ground shield in the MCU layer and use the neighbor layer as a ground layer.
  - Shield the area of the oscillator bonding wires.
  - Do not use the ground shield as oscillator ground signal.
  - Avoid ground loops. The oscillator ground signal must be connected at first to VSSD before connecting to the system ground.
  - Make sure that the routing of the oscillator ground to VSSD is as short as possible.
  - Do not route signals with strong pulses close to the oscillator. This is also valid for the neighbor layer.
- Noise emission
  - Do not route sensitive signals close to the oscillator signals (example: analog sensor signals).

10.6 Component placement

- The placement of analog components should be done in a way that the ground connection is on a common partition area. The same should be also done for digital components. The analog voltage reference regulator should be placed over the analog plane and the digital voltage regulator accordingly over the digital plane.
- Components with a common power supply should be located as centrally as possible to each other.

- The MCU and other mixed signal components should accordingly be placed on the PCB as a bridge between the analog and digital partitions.

10.7 Signal routing

- Digital power and signal traces should be routed over the digital ground planes and analog power and signal traces should be routed over the analog ground plane.
- To isolate analog signals traces, areas around the traces should be filled with copper, which are connected to the analog ground plane. The same recommendation is also valid for areas with digital signal traces.
- Do not route traces near to or parallel to other noisy and sensitive traces.
- Keep the trace lengths as short as possible.

Furthermore, when designing an application, the following areas should be closely analyzed to improve the EMC performance:

- Noisy signals, for example, signals with fast edge times
- Sensitive and high-impedance signals
- Signals that capture events, such as interrupts and strobe signals

11 Thermal considerations

Once an indication of the MCU total power requirement is known, it is very important to determine whether the system design can properly dissipate this power into the ambient air efficiently enough and any significant heat sinking and PCB design choices are required.

The MCUs cover a wide range of products from devices capable of very low power to those with very fast complex logic requiring higher power needs. Under certain conditions, MCUs may dissipate more than 1 watt of power including the core, peripheral, and I/O currents. With a lot of power in a device, necessary steps must be considered to avoid overheating. Before a design is finalized, a complete thermal review should be done. Items such as the amount of airflow through the system, nearby heat sources, and PCB construction should be reviewed. The examples given below are first steps to determine whether the preliminary design objectives can be met by taking the equation.

Calculation of junction temperature

$$T_J = T_A + \Theta_{JA} \times P_D \qquad \text{Equation 5}$$

T_J: Junction temperature

T_A: Ambient temperature

Θ_{JA}: Thermal resistance from junction to ambient

P_D: Power dissipation

For a first-order approximation, check the datasheet for the thermal resistance from junction to ambient (θ_{JA}) for the target device package. θ_{JA} is expressed in units of °C/watt. For example, the θ_{JA} for an TEQFP 120-pin is 38 °C/watt. For the same device in an TEQFP 120-pin package with an exposed pad on the bottom side correctly mounted, the θ_{JA} is reduced to 18 °C/watt, allowing a much higher total device power usage or a higher ambient operating temperature.

The maximum temperature difference between the device junction and the ambient air surrounding the device is θ_{JA} times the maximum power, or as in the first case above, 38°C/watt x 1.0 watt = 38°C. Because the specified maximum operating junction temperature of the device is 125°C, the maximum allowable ambient air temperature is 125 – 38 = 87°C. If you use the exposed pad version of package, which has a lower thermal resistance θ_{JA} of 18°C/watt if implemented with proper PCB to pad design, the maximum allowable ambient air temperature is 125°C – 18°C = 107°C. This allows a 20°C increase in ambient operating temperature or the possibility to drive more power from the device I/O or core.

Each datasheet for a device series contains a table showing package thermal resistance and maximum permissible power. This allows you to quickly see the amount of power that can practically be consumed by a device in a given package. In the datasheet, the recommended minimal PCB construction might be given. So, for example, a four-layer PCB has a better power dissipation characteristic than a two-layer PCB, because inner plane layers help to dissipate the heat.

Note: *Datasheet specifications for θ_{JA} are typical. The ambient air temperature should be much less than the allowable maximum for the product design.*

Note: *With the above calculation, if the θ_{JA} or the power dissipated is high, the maximum allowable ambient air temperature could theoretically approach the 125°C junction temperature limit. However, the product's commercial-range ambient air temperature limit of 85°C or the industrial-range ambient air temperature limit of 105°C still applies. In the example above, the first example would be unacceptable for operating a consumer grade (85°C) device. In the second example, a*

consumer-grade or industrial-grade device would be well suited depending on the choice of operating conditions of the final product.

MCUs offered in BGA or QFN packages have a reduced available surface area for thermal conduction due to the small package size; these packages must be thoroughly reviewed for power applications.

Detailed information is provided in the application notes AN72845, AN202751, and AN79938 listed in **Related documents**.

12 ADC

This section considers ADC and its analog input (AN) circuit for highly accurate sampling of the analog sensor level and other potential issues.

12.1 Filter design consideration for analog inputs

12.1.1 Principle of acquisition

The full period of sampling the analog value and then the conversion into a digital value is called acquisition time (t_{ACQ}). The voltage level of the analog input is sampled by an internal sample capacitor (C_{VIN}) within a configurable sample time (t_S); the conversion time (t_{CNV}) is implicitly configurable by the ADC clock input.

Figure 38 shows a principle circuit between the sensor, the analog source V_0, and the analog input.

$$t_{ACQ} = t_S + t_{CNV}$$ Equation 6

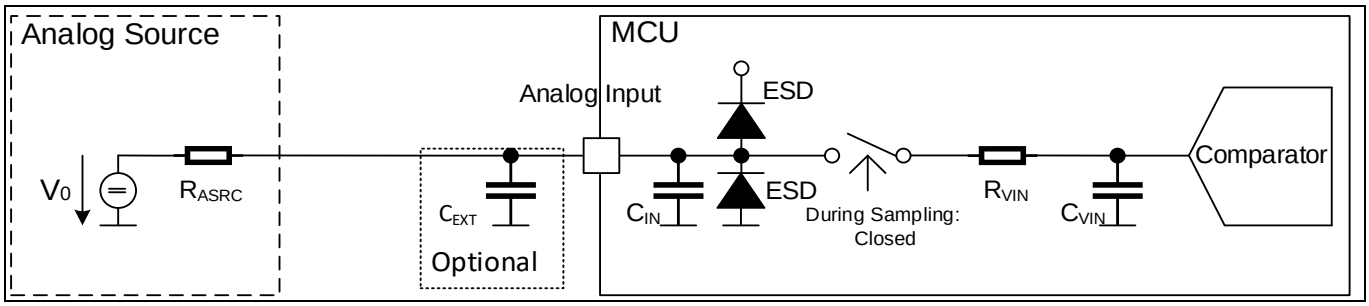


Figure 38 Analog with optional external buffer capacitor

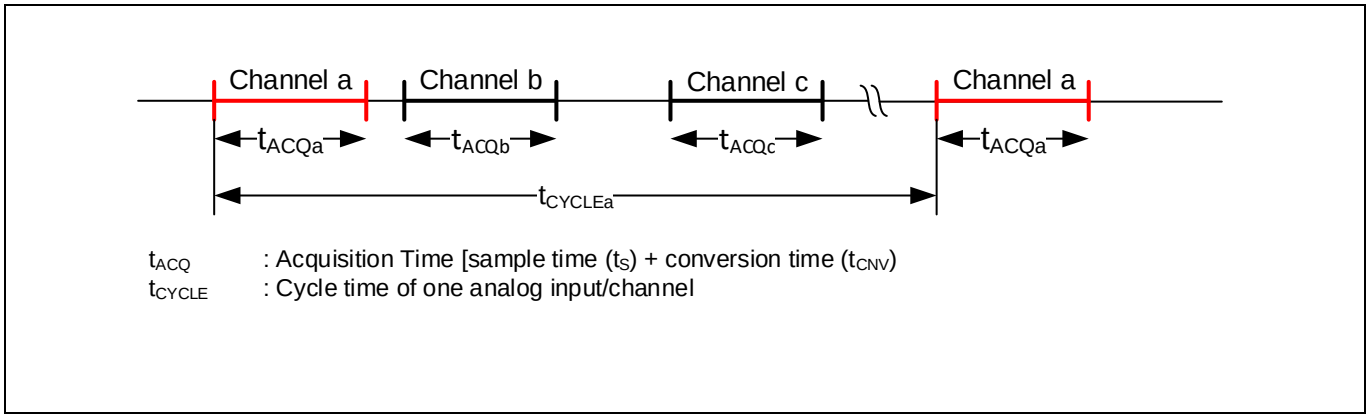


Figure 39 Cycle time of analog channels

12.1.2 Accuracy at sample time

The sample time (t_S) must be long enough for charging C_{VIN} on the same level as the analog source, which means that that the internal resistance of the analog source (R_{ASRC}) should be usually small enough. When the R_{ASRC} is too high, either the sample time must be longer which has an impact on the total sample rate of all channels, or the cycle time (t_{CYCLE}), which is the period between two acquisitions of a channel, must be longer (see **Figure 39**). After the cycle time, there should be either no or a neglectable voltage difference between the analog

source V_0 and the analog input AN before the next acquisition. When a channel is sampled twice or more directly one after the other, the following equation must be fulfilled: $t_{CYCLE} \leq t_{ACQ}$.

Keep in mind the following while calculating the cycle time t_{CYCLE}:

- The analog input must be reloaded to a new source level V_0 with the remaining voltage difference V_R depending on the required resolution 2^r. V_R should be smaller than the sampled error.
- Reloading from the external capacitor C_{EXT} to the internal sample capacitor C_{VIN} during the sample time extends the cycle time.

$$t_{CYCLE} = t_S + k \times \tau = t_S + \ln\left(\frac{2^r}{V_{R,LSB}}\right) \times \left(R_{ASRC} \times (C_{EXT} + C_{IN})\right)$$ Equation 7

Example:

Resolution: 12-bit

$V_{R,LSB}$: 0.25 LSB = 0.25 x ($1/2^{12}$)

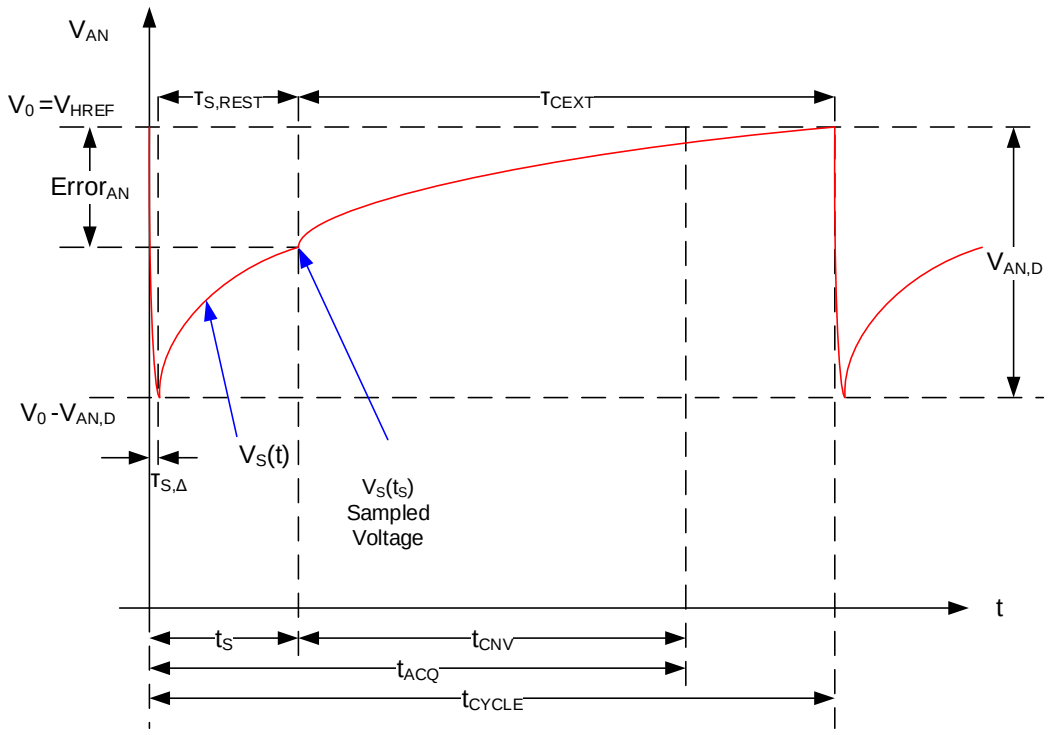
$$t_{CYCLE} = t_S + k \times \tau = t_S + \ln\left(\frac{2^{12}}{0.25}\right) \times \left(R_{ASRC} \times (C_{EXT} + C_{IN})\right) = t_S + 9.7 \times \tau$$ Equation 8

12.1.3 Sample time charging process

During the sample phase, the sample capacitor CVIN is charged by the external capacitor CEXT until both reach a common voltage (charge balancing). After that, both capacitors are charged to the analog source level V_0 via the source resistance.

So, different time constants must be considered:

- $T_{S,\Delta}$: Time constant at the beginning of the sample time for charge balancing between C_{EXT} and C_{VIN}.
- $T_{S,REST}$: Time constant during the sample time after charge balancing to charge closely to V_0 with an acceptable error.
- T_{CEXT}: Time constant, starting from the conversion time and ending with the next sample phase of the analog input.



t_s	: Sample time (t_S)
t_{ACQ}	: Acquisition time
t_{CYCLE}	: Cycle time of one analog input/channel
$\tau_{S,D}$	: Time constant for the charge balancing between C_{EXT} and C_{VIN} causing a voltage drop during sample time
$\tau_{S,REST}$	: Time constant for charging C_{EXT} and C_{VIN} by analog source V_0 for the rest of the sample time
τ_{CEXT}	: Time constant for C_{EXT} only after sample time
V_0	: Voltage of the analog source
$V_S(t)$	: Voltage level at analog input during sample time
t_{CNV}	: Conversion time
$V_{AN,D}$	: Voltage drop caused at analog input due to the charge balancing during the sample time
$Error_{AN}$	: Voltage error between sample voltage and analog source voltage level

Figure 40 Charging curve of analog input during acquisition time

12.1.4 Charge balancing between C_{EXT} and C_{VIN}

Depending on the ADC macro implementation, the sample capacitor can be precharged to a target level ($C_{VIN, PRE}$) before starting the sample phase. If this feature is not deployed, C_{VIN} will have the voltage level of the previous acquisition, which means that in the worst case, the maximum voltage difference ($\Delta V_{CVIN, PRE}$) between C_{VIN} and the external capacitor C_{EXT} corresponds to the analog reference voltage V_{REFH}. When the sample switch is closed, charge balancing between the external capacitor C_{EXT} and the sample capacitor C_{VIN} causes a voltage drop at the analog input $V_{AN, D}$.

$$V_{AN,D} = \frac{Q_{VIN}}{(C_{IN} + C_{EXT}) + C_{VIN}} = \frac{C_{VIN} \times (V_0 - V_{VIN,PRE})}{(C_{IN} + C_{EXT}) + C_{VIN}} = \frac{C_{VIN} \times \Delta V_{VIN,PRE}}{(C_{IN} + C_{EXT}) + C_{VIN}}$$ Equation 9

In simplified consideration of **Equation 9**, the analog input and the analog source have the same voltage level $V_{AN} = V_0$, resulting in **Equation 10**.

$$V_{AN,D} = \frac{Q_{VIN}}{(C_{IN} + C_{EXT}) + C_{VIN}} = \frac{C_{VIN} \times (V_0 - V_{VIN,PRE})}{(C_{IN} + C_{EXT}) + C_{VIN}}$$ Equation 10

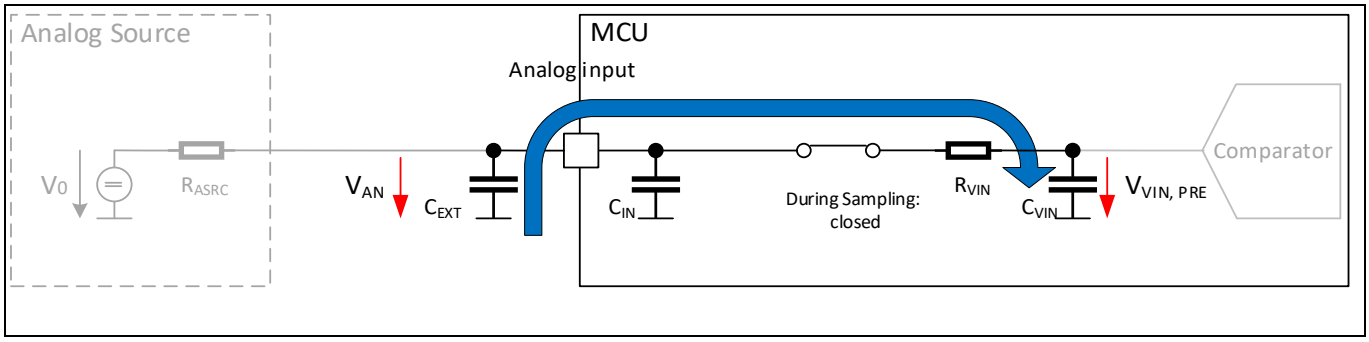


Figure 41 Charge balancing during ADC sample time

While this charge balancing happens, it is assumed that $R_{ASRC} >> R_{VIN,}$ and therefore R_{ASRC} has no impact during that phase. This results in the following time constant $\tau_{S,\Delta}$ for charging the capacitor:

$$\tau_{S,D} = R_{VIN} \times C_{SUM} = R_{VIN} \times \left(\frac{1}{1/(C_{EXT} + C_{IN}) + 1/C_{VIN}} \right)$$ Equation 11

So, in the worst scenario for the maximum voltage difference between analog input and the sample capacitor after $9.7^{*}\tau_{S,D}$, the voltage error of the analog input is less than 0.25 LSB_{12}.

12.1.5 Charging analog input by analog source V_0

Depending on the dimensioning of the external capacitor C_{EXT}, charge balancing between C_{EXT} and C_{VIN} causes a huge voltage difference in the analog input in relation to the analog source V_0, and the analog input must be charged by V_0 itself directly. In this case, the analog source resistance R_{ASRC} has a relevant influence for the charging curve.

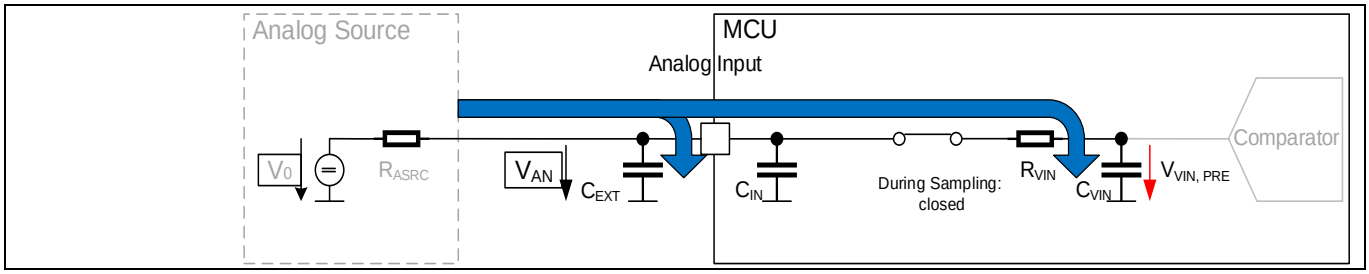


Figure 42 Charging of analog input during sample time by the analog source V_0

So, for the rest of the sample time, the time constant $\tau_{S,REST}$ is calculated as follows:

$$\tau_{S,REST} = (R_{VIN} + R_{ARSC}) \times C_{VIN} + R_{ARSC} \times (C_{EXT} + C_{IN}) \quad \text{Equation 12}$$

12.1.6 Filter case: $C_{EXT} > 2^r * C_{VIN}$

When the analog source impedance is too high, the sampling period for analog voltages may be insufficient, especially when all analog inputs need to be sampled with a common high sample rate (for example, 1 MS/s). If the cyclic sampling of the dedicated analog input, the cycle time (t_{CYCLE}), can be much longer, a large external buffer capacitor C_{EXT} can be deployed. The dimensioning considers the maximal target error at the sampled analog input $Error_{AN}$.

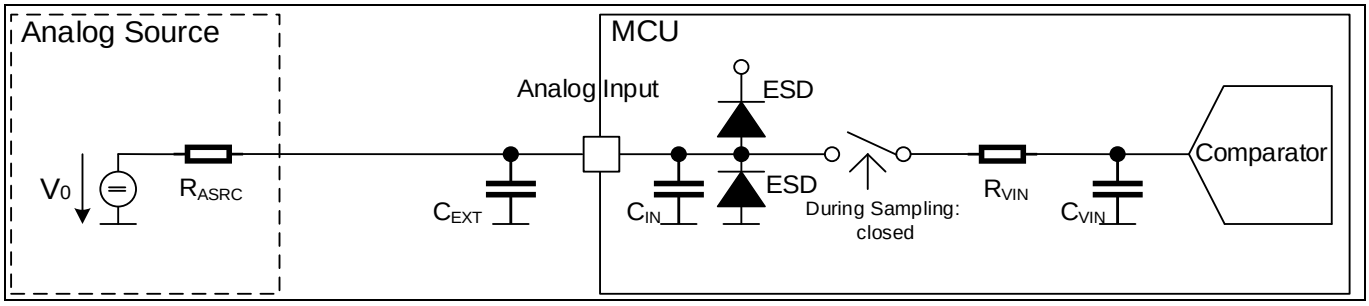
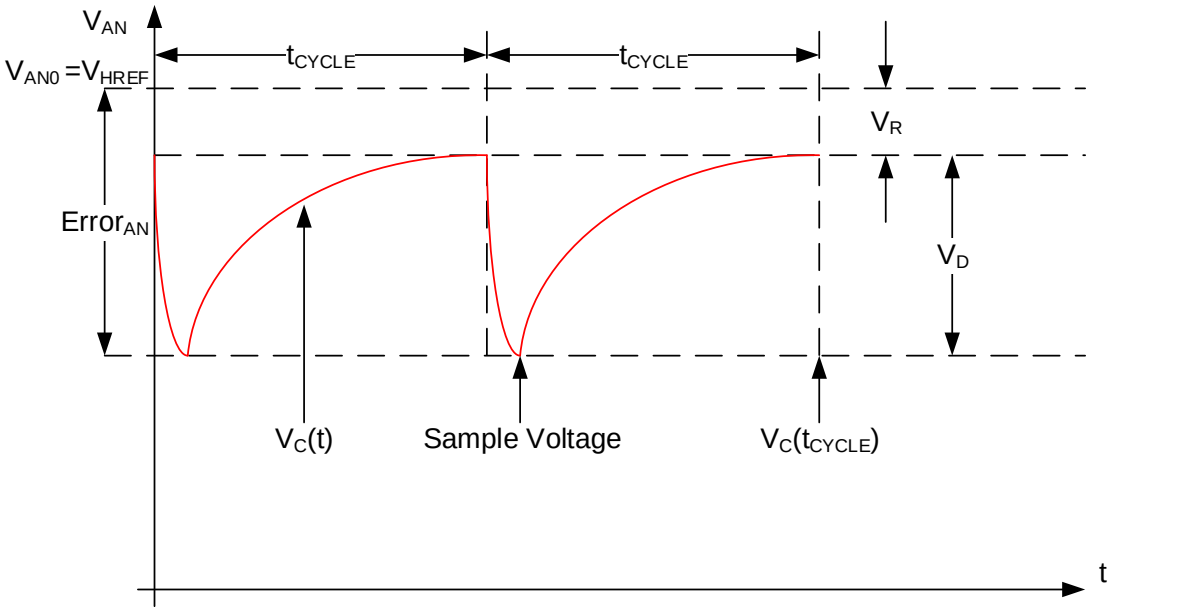


Figure 43 Analog input with decoupling capacitor against internal switching noise



t_{CYCLE} : Cycle time of one analog input / channel
V_0 : Voltage of the analog source
V_R : Remaining voltage at the end of t_{CYCLE}
$V_C(t)$: Charge curve for C_{EXT}
V_D : Voltage drop at the beginning of the sample phase due to charging vom C_{EXT} to sample capacitor C_{VIN}
$Error_{AN}$: Voltage error between sample voltage and analog source voltage level

Figure 44 Simplified cyclic charge curve of C_{EXT} for use case CEXT > 2r * CVIN

At first, the maximum permitted error $Error_{AN}$ must be defined as shown in **Equation 13**.

$$Error_{AN} = 1/2^{E} \times LSB_r \quad \text{Equation 13}$$

with:

r = 12: 12-bit resolution E = 0; ErrorAN = 1 LSBr

r = 12: 12-bit resolution E = 1; ErrorAN = LSBr / 2

r = 12: 12-bit resolution E = 2; ErrorAN = LSBr / 4

$$C_{EXT} = 2^{r+E} \times C_{VIN} \quad \text{Equation 14}$$

To achieve a sampling error of less than 0.25 LSB (E = 2) at 12-bit resolution (r = 12), the minimum external filter capacitor C_{EXT} is as shown in **Equation 15**.

$$C_{EXT,0.25LSB} \geq 2^{r+E} \times C_{VIN} = 2^{12+2} \times C_{VIN} \quad \text{Equation 15}$$

Due to the selection of $C_{EXT} > 2^r * C_{VIN}$, the sample time t_S can be selected independently of the analog source R_{ASRC}. Nevertheless, R_{ASRC} has a direct impact to the cycle time t_{CYCLE}.

12.1.7 Discrete RC filter

If an extended sample time is insufficient to filter the noise on the analog signal input, you can use an external low-pass filter (RC filter) to the analog input pin (see **Figure 45**). Cross-check the possible sample period with the cut-off frequency of the RC filter. Furthermore, the voltage drop at R_{EXT} due to the complete leakage current of the analog input must not be higher than the required accuracy of the measured analog signal.

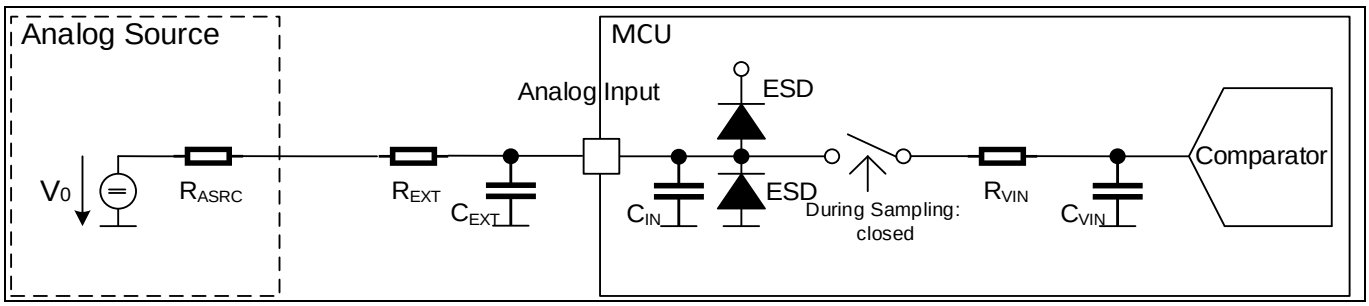


Figure 45 Analog input with low-pass filter

13 Assembly and package-related PCB design

The application notes AN202751 and AN79938 provided guidelines on surface mount assembly for different BGA packages, related PCB design, surface mount process flow, and final joint inspection methods.

14 Summary

The application note described how to set up a minimum MCU system. The application note also provided hints on how to handle different uses cases at MCU pins and how to make a proper PCB layout design.

15 Abbreviations

Abbreviation	Description
ADC	A/D Converter
ALT	Alternate
AN	Analog Input
BOD	Brown-out-Detection
BOM	Bill of Material
DeCap	Decoupling capacitor
DDR	Double Data Rate. Data sampled twice within a clock cycle. fDATA = fCLK
DS	Data Sheet
DUT	Device under Test
ECU	Electronic Control Unit
ETM	Embedded Trace Macrocell™
Ext	external
GND	Electrical ground
GPIO	General Purpose I/O
HVD	High-Voltage-Detection
IC	Integrated Circuit
IF	Interface
Int	Internal
IO	Input Output
JTAG	Joint Test Action Group is the common name for the IEEE 1149.1 Standard Test Access Port, Boundary-Scan Architecture, and interface for debug tools for on-chip debug inside the target MCU
LDO	Low Drop-Out Line Regulator
LPF	Low Pass Filter
LVD	Low-Voltage-Detection
LU	Latch-up
MAC	Media Access Control. Component independent from communication medium.
MCU	Microcontroller
MCU	Microcontroller Unit
PDN	Power Distribution Network
SDR	Single Data Rate. Data sampled only once within a clock cycle. fDATA = ½ x fCLK
S/s	Samples per second
NC	Not connected
OCD	Over-Current-Detection
OVD	Over-Voltage-Detection
PCB	Printed Circuit Board
POR	Power-On-Reset
Rd	Damping resistor
Rf	Feedback resistor
STP	Shielded Twisted-Pair
SWD	Serial Wire Debug

Abbreviations

Abbreviation	Description
TRM	Technical Reference Manual
VCC	Generic naming convention for power supply pin
Voltage droop	Transient voltage drop
VSS	Generic naming convention for ground pin
WDT	Watchdog Timer

16 Related documents

- AN230194 – Setting ECO Parameters
- AN224153 – Design and Layout Guide for Semper Flash Memory
- **AN79938** – Design Guidelines for Cypress Ball Grid Array (BGA) Packaged Devices
- **AN202751** – Surface Mount Assembly Recommendations for Cypress FBGA Packages
- **AN213250** – Power Filter Options for FPD-Link Interfaces
- AN234415 – XMC7000 External Power Supply Design Guide
- AN234334 – Getting Started with the XMC7000 MCU on ModusToolbox software
- **AN72845** – Design Guidelines for QFN Packaged Devices
- **AN89611** – PsoC 3 and PSoC 5LP Getting Started with Chip Scale Packages
- **AN80994** – Design Considerations for Electrical Fast Transient (EFT) Immunity
- **AN57821** – PsoC 3, PSoC 4, and PSoC 5LP Mixed Signal Circuit Board Layout Considerations
- **ARM_Link_01** – CoreSight Components Technical Reference Manual (Cortex® debug connector detailed specification in Appendix C)
- **ARM_Link_02** – Cortex®-M Debug Connectors
- **SRAM Board Design Guidelines**
- Technical Reference Manual (TRM)
  - XMC7000 Architecture Technical Reference Manual (Doc No. 002-33816)
  - XMC7100 Register Technical Reference Manual (Doc No. 002-33817)
  - XMC7200 Register Technical Reference Manual (Doc No. 002-33812)
- Device datasheet
  - Datasheet 32-Bit Arm® Cortex®-M7 Microcontroller XMC7100 Family (Doc No. 002-33896)
  - Datasheet 32-Bit Arm® Cortex®-M7 Microcontroller XMC7200 Family (Doc No. 002-33522)

Contact **Technical Support** to obtain XMC7000 family series datasheets and Technical Reference Manuals.

17 Appendix A - Power supply concept

The appendix provides the MCU-specific proposals for a power supply concept including decoupling capacitors for the MCU power supply.

*Note: The deployment of decoupling caps and the bypass capacitors depend on the application. This is especially valid for the I/O supplies. For more information, see **I/O domains**.*

Definitions

- f_{CLK}: Clock signal frequency
- f_{DATA}: Data signal frequency
- SDR: Single Data Rate. Data sampled only once within a clock cycle. $f_{DATA} = ½ \times f_{CLK}$
- DDR: Double Data Rate. Data sampled twice within a clock cycle. $f_{DATA} = f_{CLK}$
- 'Pin': Synonym for the original pin name
- Domain: Power Domain. One power domain can have one or more power pins (for example, VDDD has several pins)
- Voltage drop: Transient voltage drop

17.1 XMC7000 Series with TEQFP package

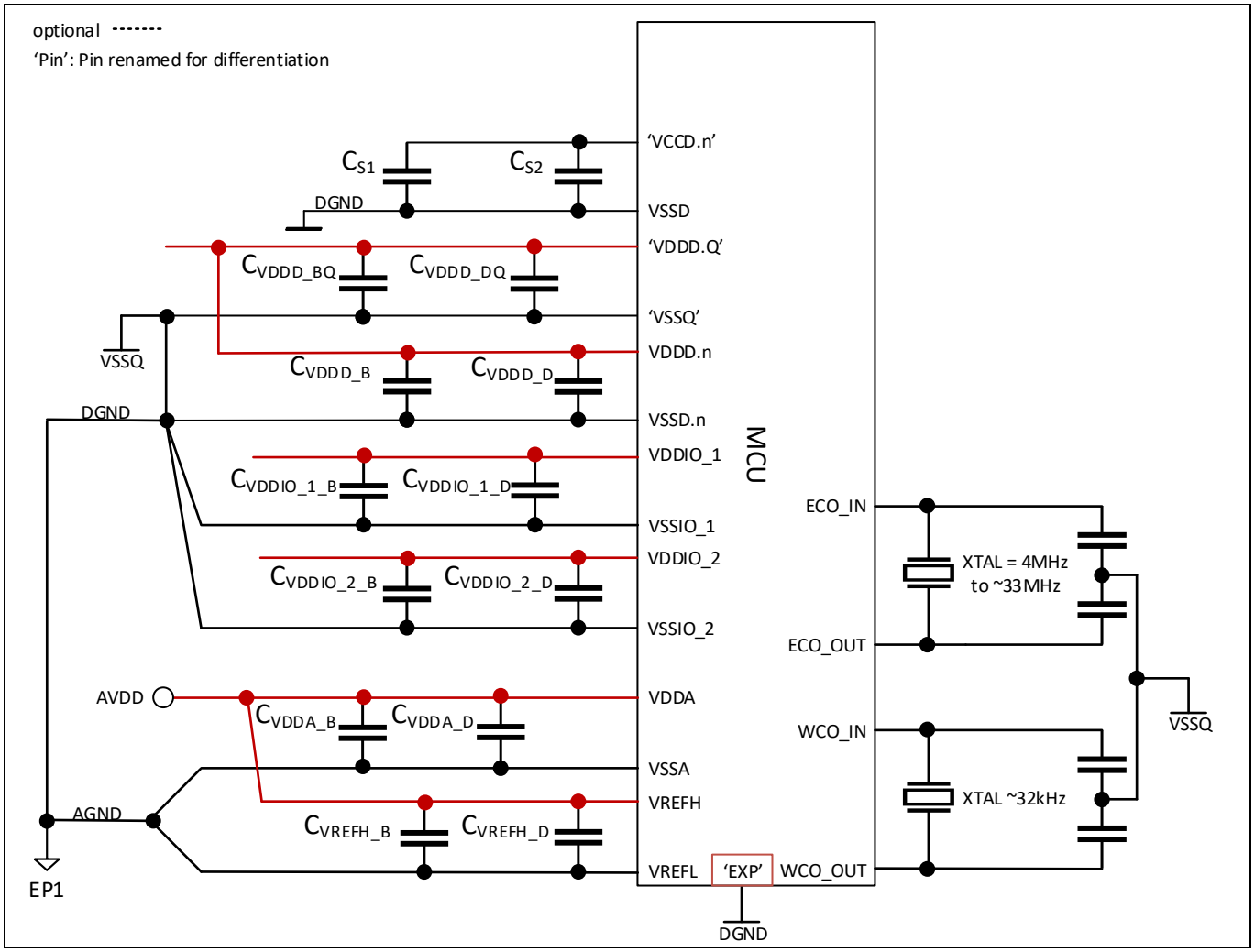


Figure 46 Power supply concept example for XMC7000 Series with TEQFP package

Appendix A - Power supply concept

Table 13 External component integration example for XMC7000 Series with TEQFP package

Symbol	Parameter	Package	
		Value	Remark
C_{S1}	Bypass/smoothing capacitor for core power supply domain VCCD	X7R type	Value in the datasheet. Close to pin pair according to the device datasheet specification with respect to 'VCCD.CS1'. Two capacitors per power domain. ESR ≤ 100 mΩ, ESL ≤ 4 nH in total per capacitor including board track to all VCCD pins with priority on pin 'VCCD.CS1' with I_{DD_VDDD}[7] ≤ 150 mA by the active regulator. Values do not cover higher load transition cases like wakeup from DeepSleep with permanent supply from an external PMIC.
C_{S2}	Decoupling capacitor for core power supply domain VCCD	100 nF X7R ALT: 47 nF X7R	1 capacitor per power domain pin group. For VCCD pin group definition, see **Table 14**.
C_{VDDD_BQ}	Bypass capacitor for VDDD domain IPs	10 µF X7R	Also, used for low-frequency decoupling and MCU inrush current. For PCB-specific capacitor dimensioning, consider the inrush current from the active regulator in spec ID SID603 mentioned in the datasheet and **Appendix D - Active regulator inrush current**. 2 capacitors per power domain. ESR ≤ 100 mΩ, ESL ≤ 4 nH in total per capacitor including the board track.
C_{VDDD_DQ}	Decoupling capacitor for VDDD domain IPs	100 nF X7R	Voltage drop greater than 300 mV must be avoided to keep the stability of the internal LDO and reset assertion trip points. Pin 'VDDD.Q' (Quiet Supply) is not shared with I/O domain, but with the oscillator among others.
C_{VDDD_B}	Bypass capacitor for VDDD domain IPs and I/O	-	Required only if C_{VDDD_BQ} is not sufficient for bypassing the power rail supply.
C_{VDDD_D}[8,9]	Decoupling capacitor VDDD domain logic and I/O	100 nF X7R	1 capacitor per power domain pin. Decoupling conditions are valid per pin; all toggling groups should toggle asynchronously with each other.
$C_{VDDIO\_1\_B}$	Bypass capacitor for IO domain VDDIO_1	TBD	Optional. Depending on the power supply inductance.

[7] I_{DD_VDDD}: input current definition of VDDD in internal supply mode in XMC7000 datasheet

[8] VDDD: 5V, 4% voltage drop, f_{DATA}: 2 MHz, 4x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[9] VDDD: 5V, 4% voltage drop, f_{DATA}: 0.1 MHz, 4x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

Appendix A - Power supply concept

Symbol	Parameter	Package	
		Value	Remark
$C_{VDDIO\_1\_D}$[10,11]	Decoupling capacitor for IO domain VDDIO_1	100 nF X7R	1 capacitor per power domain pin. Decoupling condition is valid for the whole domain.
$C_{VDDIO\_2\_B}$	Bypass capacitor for IO domain VDDIO_2	-	
$C_{VDDIO\_2\_D}$[12]	Decoupling capacitor for IO domainVDDIO_2	100 nF X7R	1 capacitor per power domain pin. Decoupling condition is valid for the whole domain. *Note: Voltage drop at VDDIO_2 must fulfill the requirement VDDA – 0.3 V ≤ VDDIO_2 ≤ VDDA*
C_{VDDA_B}[13]	Bypass capacitor for ADC VDDA	2.2 µF X7R	-
C_{VDDA_D}	Decoupling capacitor for ADC VDDA	100 nF X7R	1 capacitor per power domain pin
C_{VREFH_B}	Bypass capacitor for ADC VREFH	2.2 µF X7R	Optional. Required only if a separate analog reference supply is used. Silent supply is required. If the supply is not sufficient, LPF is required.
C_{VREFH_D}	Decoupling capacitor for ADC VREFH	100 nF X7R	

Table 14 Special power domain pins for XMC7000 Series with TEQFP package

Name	Package pin number (original pin name)			Remark
	100-TEQFP	144-TEQFP	176-TEQFP	
'VDDD.Q'	86 (VDDD)	124 (VDDD)	153 (VDDD)	Quiet supply. Not shared with the I/O domain.
'VSSQ'	87 (VSSD)	125 (VSSD)	154 (VSSD)	Quiet ground for the oscillator.
'VCCD.CS2.A'	27 (VCCD) 28 (VCCD)	38 (VCCD) 39 (VCCD)	46 (VCCD) 47 (VCCD)	One decap C_{S2} on pin group
'VCCD.CS2.B'	63 (VCCD) 64 (VCCD) 65 (VCCD)	91 (VCCD) 92 (VCCD) 93 (VCCD)	111 (VCCD) 112 (VCCD) 113 (VCCD)	One decap C_{S2} on pin group
'VCCD.CS2.C'	89 (VCCD)	127 (VCCD)	156 (VCCD)	One decap C_{S2} on pin group
'EXP'	yes	yes	yes	Exposed Pad

[10] VDDIO_1: 5V, 4% voltage drop, f_{DATA}: 2 MHz, 5x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[11] VDDIO_1: 5V, 4% voltage drop, f_{DATA}: 0.1 MHz, 5x parallel transition: 100 ns, C_L/pin: 47 pF, asynchronous to footnote **10**, no consideration of device internal impedance

[12] VDDIO_2: 5 V, 4% voltage drop, f_{CLK}: 2 MHz, SDR, 10 x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[13] Connection of C_{VDDA_B} to both ADC DeCaps for low-noise environment. Three ADC units run simultaneously, not asynchronously and no use of the precondition feature. Power rails and ground parasitic for the analog supply should not exceed the following values according to **Figure 49**: R_{AVDD} ≤ 100 mΩ, L_{AVDD} ≤ 15 nH, R_{AGND} ≤ 100 mΩ, L_{AGND} ≤ 15 nH, L1 ≤ 1 nH, L2 ≤ 1nH

17.2 XMC7000 Series with BGA package

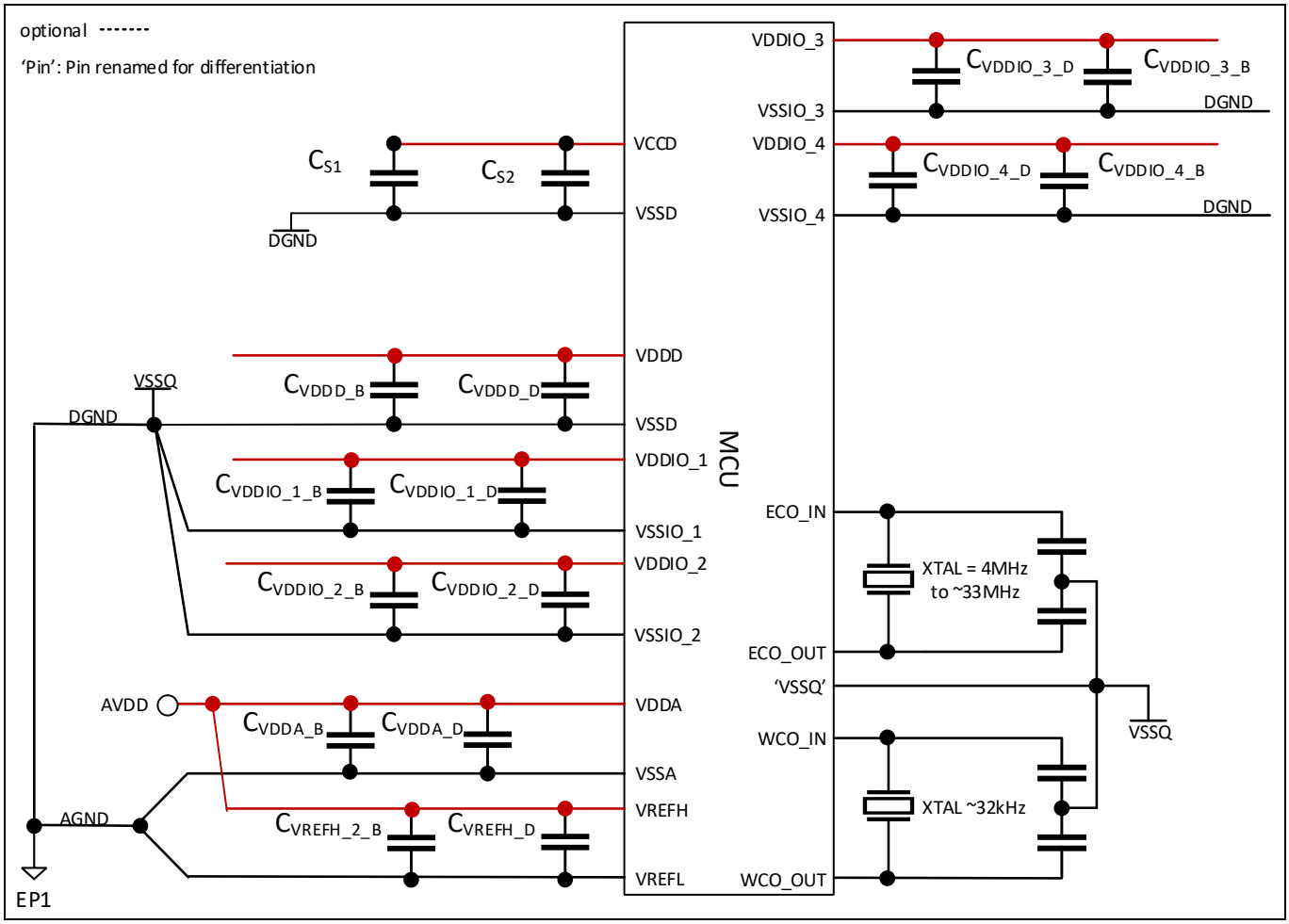


Figure 47 MCU power supply concept example for XMC7000 Series with BGA package

Table 15 External component integration example for XMC7000 Series BGA package

Symbol	Parameter	Package	
		Value	Remark
C_{S1}	Bypass/smoothing capacitor for core power supply domain VCCD	X7R Type	Value in the datasheet. Nominal value for the power domain. Close to pin pair according to the device datasheet specification. Check the capacitor value and placement requirements between MCU and PMIC depending on core VCCD power rail concept.
C_{S2}	Decoupling capacitor for core power supply domain VCCD	100 nF X7R ALT: 47 nF X7R	1 capacitor per power domain pin
C_{VDDD_B}	Bypass capacitor for VDDD domain IPs and I/O	10 µF X7R	Required for internal LDO. For PCB-specific capacitor dimensioning, consider the inrush current from the active regulator in spec ID SID603 mentioned in

Appendix A - Power supply concept

Symbol	Parameter	Package	
		Value	Remark
			the datasheet and **Appendix D - Active regulator inrush current**.
C_{VDDD_D}	Decoupling capacitor VDDD domain logic and I/O	100 nF X7R	1 capacitor per power domain pin. Voltage drop greater than 300 mV must be avoided due to internal LDO and reset assertion trip points. The number of parallel transitions should be reduced as much as possible.
$C_{VDDIO\_1\_B}$[14]	Bypass capacitor for IO domain VDDIO_1	1 µF X7R	1 capacitor per power domain
$C_{VDDIO\_1\_D}$[12]	Decoupling capacitor for IO domain VDDIO_1	100 nF X7R	1 capacitor per power domain pin. Minimum two pieces are required.
$C_{VDDIO\_2\_B}$	Bypass capacitor for IO domain VDDIO_2	-	
$C_{VDDIO\_2\_D}$[15]	Decoupling capacitor for IO domain VDDIO_2	100 nF X7R	1 capacitor per power domain pin *Note: Voltage drop at VDDIO_2 must fulfill the requirement VDDA – 0.3 V ≤ VDDIO_2 ≤ VDDA*
$C_{VDDIO\_3\_B}$	Bypass capacitor for IO domain VDDIO_3	1 µF X7R	1 capacitor per power domain. Equivalent power rail inductance: 20 nH
$C_{VDDIO\_3\_D}$[16]	Decoupling capacitor for IO domain VDDIO_3	100 nF X7R 10 nF X7R	1 capacitor for power domain 1 capacitor for power domain
$C_{VDDIO\_4\_B}$	Bypass capacitor for IO domain VDDIO_4	1 µF X7R	1 capacitor per power domain. Equivalent power rail inductance: 20 nH
$C_{VDDIO\_4\_D}$[17]	Decoupling capacitor for IO domain VDDIO_4	100 nF X7R 10 nF X7R	1 capacitor for power domain 1 capacitor for power domain
C_{VDDA_B}[18]	Bypass capacitor for ADC VDDA	2.2 µF X7R	-
C_{VDDA_D}	Decoupling capacitor for ADC VDDA	100 nF X7R	1 capacitor per power domain pin
$C_{VREFH\_2\_B}$	Bypass capacitor for ADC VREFH	2.2 µF X7R	Optional. Required only if a separate analog reference supply is used.
C_{VREFH_D}	Decoupling capacitor for ADC VREFH	100 nF X7R	

[14] VDDIO_1: 3.3 V, 5% voltage drop at capacitors(s), f_{CLK}: 25 MHz, DDR, 9 x parallel transition: 3 ns, C_L/pin: 20 pF, no consideration of device internal impedance

[15] VDDIO_2: 5 V, 4% voltage drop at capacitor(s), f_{DATA}: 2 MHz, 10 x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

Conditions:

[16] VDDIO_3: 3.3 V, 7% voltage drop at capacitors, f_{CLK}: 100 MHz, DDR, 9 x parallel transition: 1.5 ns, C_L/pin: 15 pF, no consideration of device internal impedance

[17] VDDIO_4: 3.3 V, 7% voltage drop at capacitors, f_{CLK}: 125 MHz, SDR, 9 x parallel transition: 0.75 ns, C_L/pin: 10 pF, no consideration of device internal impedance

[18] Connection of C_{VDDA_B} to both ADC DeCaps for low-noise environment. Three ADC units run simultaneously, not asynchronously and no use of the precondition feature. Power rails and ground parasitic for the analog supply should not exceed the following values according to **Figure 49**: R_{AVDD} ≤ 100 mΩ, L_{AVDD} ≤ 15 nH, R_{AGND} ≤ 100 mΩ, L_{AGND} ≤ 15 nH, L1 ≤ 1 nH, L2 ≤ 1nH

Table 16 Special power domain pins for XMC7000 Series with BGA package

Name	Package pin number (original pin name)	Remark
	272-BGA	
'VSSQ'	L11 (VSSD_1)	Quiet ground for the oscillator

18 Appendix B - Analog supply

Figure 48 and **Figure 49** show the difference between an ideal analog supply without any parasitic elements and a real analog supply with the parasitic elements in the power rail and in the filter capacitors.

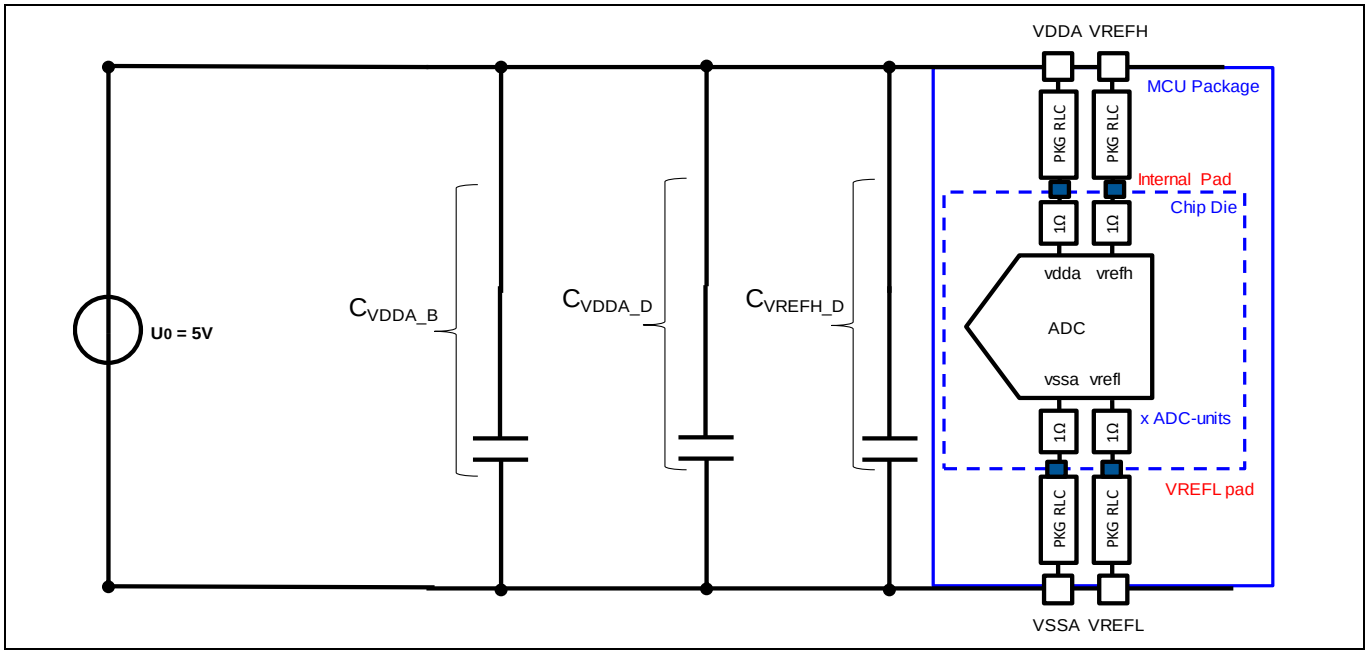


Figure 48 Ideal analog power supply

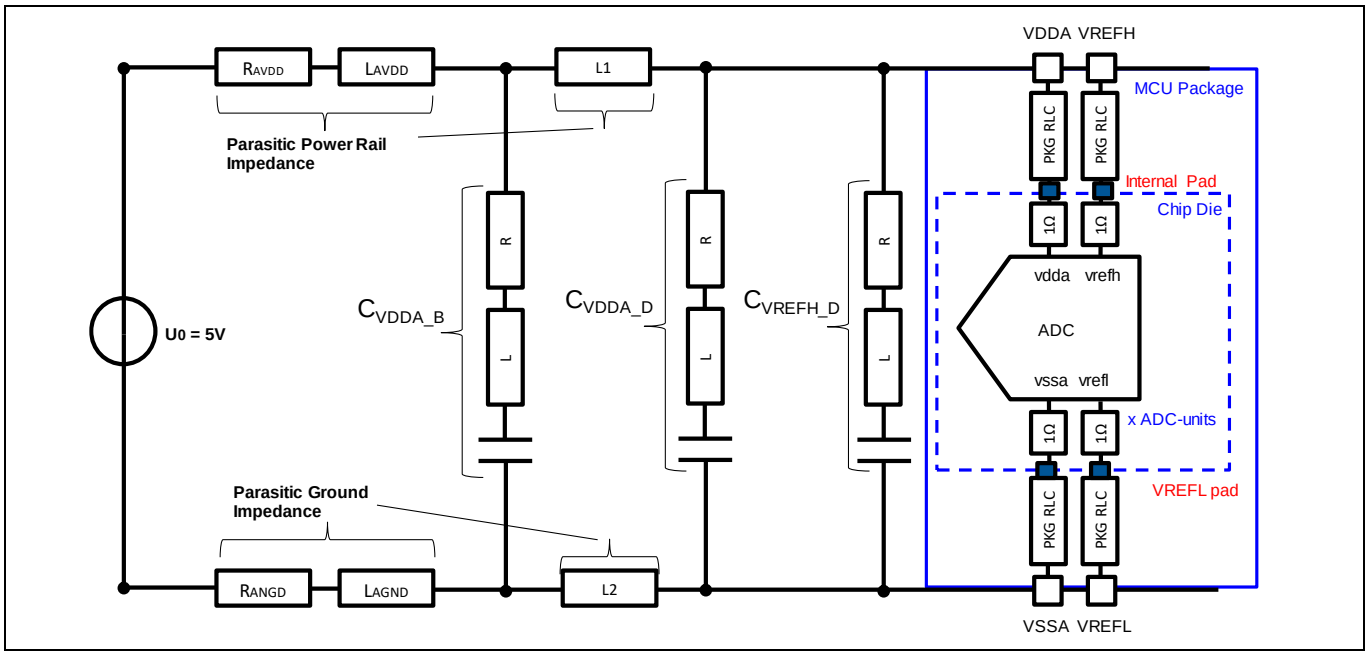


Figure 49 Real analog power supply

19 Appendix C - Oscillator layout

Note: Layout design neither gives any warranty for correct component ratio nor does not follow any PCB design rules. Changes between different packages might be required.

19.1 TEQFP packages

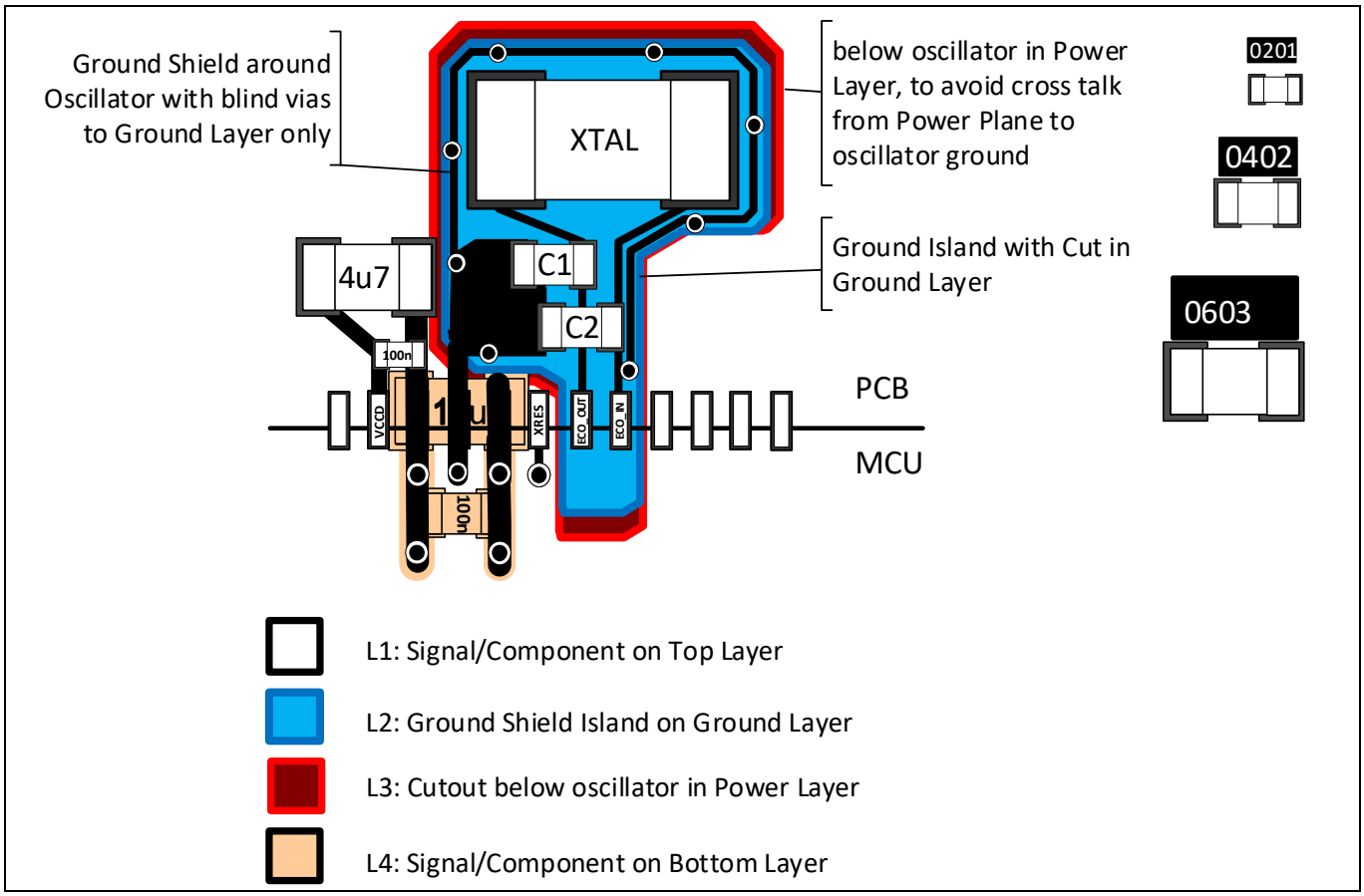


Figure 50 Oscillator layout proposal for XMC7000 Series TEQFP packages

19.2 BGA packages

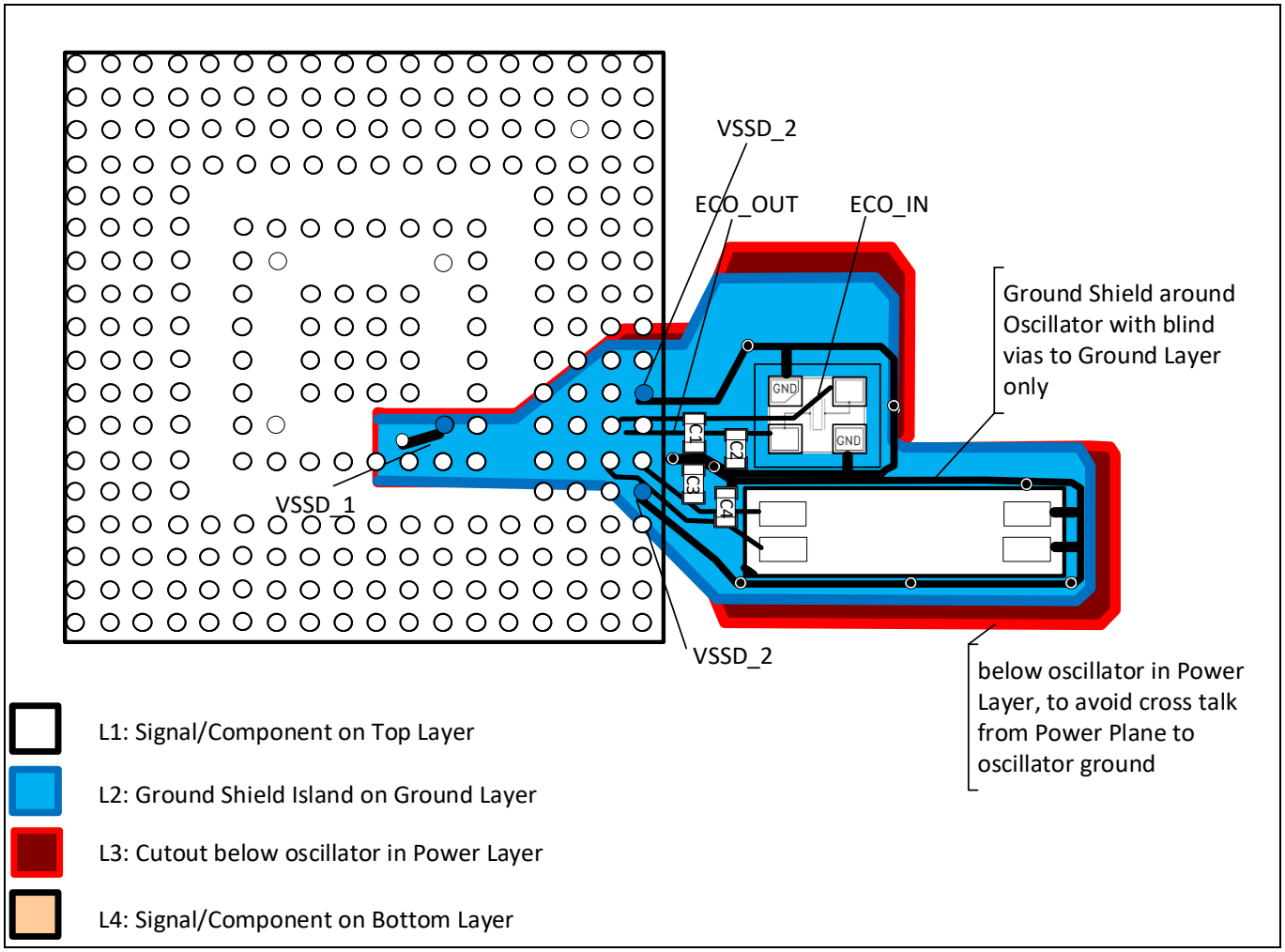


Figure 51 Oscillator layout proposal for BGA packages (based on XMC7000 Series 272-BGA package)

20 Appendix D - Active regulator inrush current

As one part of dimensioning of the bypass capacitors at the VDDD domain, the external voltage regulator, the PCB parasitics (ESR and ESL) of that power rail, and the maximum current consumption of the active regulator (internal LDO) must be considered. The fastest inrush current transient into the active regulator is shown for MCUs with a maximum of 300 mA internal LDO operation current (XMC7000).

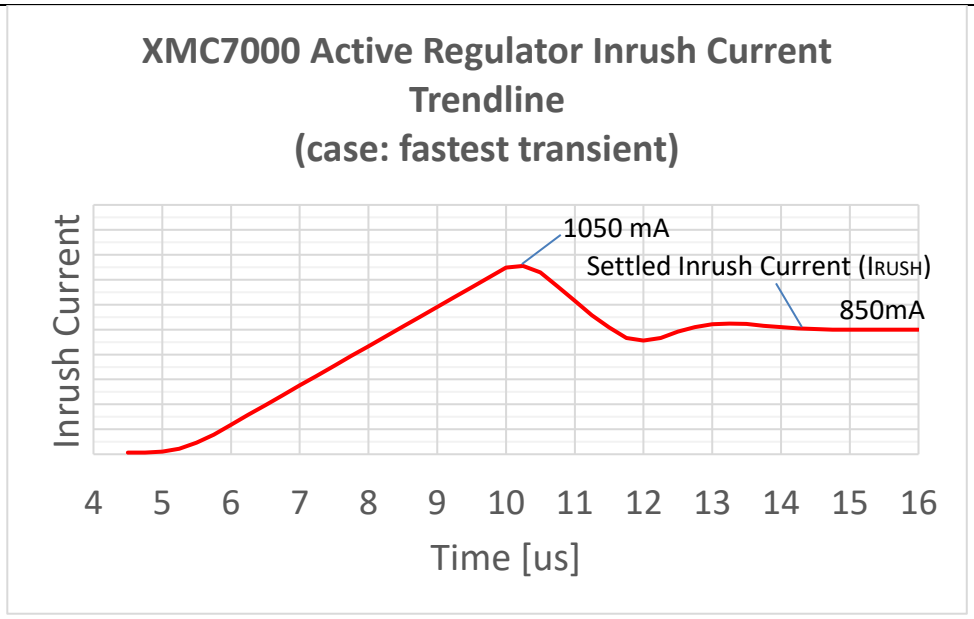


Figure 52 XMC7000 active regulator inrush current in worst-case scenario

21 Appendix E - Unused power domain handling

This section explains how to handle unused power domains and their I/O port pins. It does not consider the transition requirements for different power modes, that is, the power ON/OFF sequencing. With regard to I/O port pin handling, make sure that the ECU peripherals are in proper states during power mode transitions.

21.1 XMC7000 Series

Table 17 Unused domain handling of XMC7000 Series

Power domain	Voltage operation range	Permanent unused domain (active mode)			DeepSleep Mode			Hibernate		
		Can be switched OFF? [Yes, No]	I/O pin handling[19]	Remark	Can be switched OFF? [Yes, No]	I/O pin handling[19]	Remark	Can be switched OFF? [Yes, No]	I/O pin handling[19]	Remark
VDDD (always-on)	2.7 - 5.5 V	No	-	-	No	-	-	No	-	-
VCCD	1.09 - 1.21 V	No	-	-	No	-	-	-	-	-
VDDA_ADC	2.7 - 5.5 V	No	-	-	Yes	-	Disable BOD Reset before DeepSleep	Yes	-	-
VDDA_VREFH	2.7 - 5.5 V	Yes	-	-	Yes	-	-	Yes	-	-
VDDIO_1	2.7 - 5.5 V	Yes	Tie to GND, Open pin	-	Yes	Disable	-	Yes	Disable	-
VDDIO_2	2.7 - 5.5 V	No	-	-	Yes	Disable	-	Yes	Disable	-
VDDIO_3	2.7 - 3.6 V	Yes	Tie to GND, Open pin	-	Yes	Disable	-	Yes	Disable	-

[19] Explanation on I/O Pin Handling (For details on unused I/O port pins, see **Port input/unused pins**)

- Tie to GND: Direct connection to GND. Floating levels must be avoided due to latch-up (LU) risk
- Open pin: Pin stays open, no wiring. Exception in power save modes.
- Disable: Disable input-buffer and disable output.

Power domain	Voltage operation range	Permanent unused domain (active mode)			DeepSleep Mode			Hibernate		
		Can be switched OFF? [Yes, No]	I/O pin handling[19]	Remark	Can be switched OFF? [Yes, No]	I/O pin handling[19]	Remark	Can be switched OFF? [Yes, No]	I/O pin handling[19]	Remark
VDDIO_4	2.7 - 3.6 V	Yes	Tie to GND, Open pin	N/A in all packages	Yes	Disable	-	Yes	Disable	-

22 Appendix F - Power supply filter characteristics

As part of a second-order LPF, a ferrite bead is deployed instead of an inductor. This appendix shows a ferrite bead specification example.

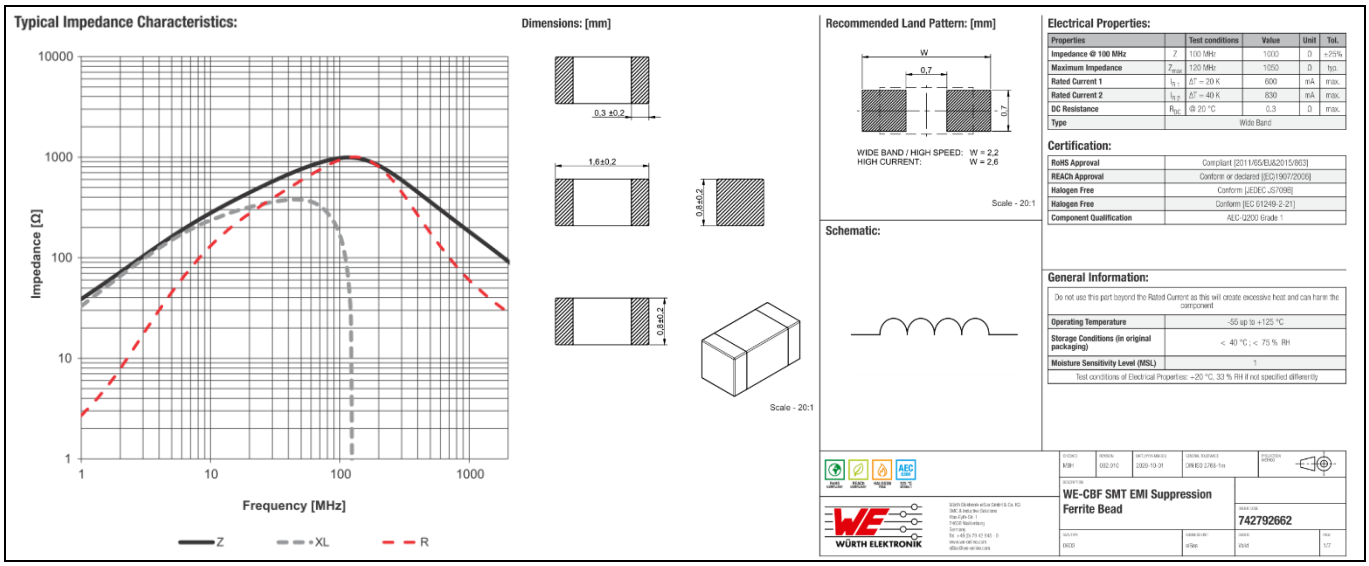


Figure 53 Ferrite bead specification example

Revision history

Document version	Date of release	Description of changes
**	2021-12-02	New application note.

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