HYPERRAM™ timing compatibility with JEDEC xSPI (JESD251)

About this document

Scope and purpose

AN234072 discusses the input and output timing compatibility between Infineon's latest high-density, high performance, 64-Mb/128-Mb HYPERRAM™ and JEDEC xSPI (JESD251). This application note also analyzes the input and output timing parameter mismatch between HYPERRAM™ and JESD251 and provides a workaround to mitigate any incompatibility due to timing mismatch in a system.

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1 Introduction

HYPERBUS™ & OCTAL xSPI HYPERRAM™ is a high-performance, 8-bit wide, serial, Self-Refresh DRAM or also called Pseudo-Static Random-Access Memory (PSRAM) introduced by Infineon. HYPERRAM™ follows JEDEC standard Expanded Serial Peripheral Interface (xSPI) (JESD251) protocol and timings. JESD251 specifies two interface profiles where profile-1 is OCTAL xSPI and profile-2 is HYPERBUS™. Both profiles support the 8D-8D-8D signaling standard in which the command, address, and data bytes are transmitted over the 8-bit DQ (IO) bus, in DDR mode. Even though HYPERRAM™ follows the JESD251 standard, there are some parameters/timings differences between the two that may make HYPERRAM™ incompatible with hosts (MCUs/ASICs) which are designed following JESD251 standard.

This application note compares all input and output timing of the 64/128-Mb HYPERRAM™ with JESD251 and analyzes any timing mismatch between them. In addition, this application note also suggests a workaround that can help in resolving any timing mismatch and make the access timing compatible in a system. Since HYPERRAM™ came into existence earlier than JESD251, some spec mismatch in HYPERRAM™ from JESD251 are inevitable. Therefore, analyzing and fixing any timing incompatibility with appropriate timing adjustment is necessary for a reliable system design. This application note doesn't capture all timing parameters and details; therefore, you must refer to the **64-Mb/128-Mb HYPERRAM™** datasheets for additional information.

Even though this application note has exclusively used the timing parameters of the 64-Mb/128-Mb density HYPERRAM™ for comparison, this timing compatibility analysis also applies to higher density HYPERBUS™ and OCTAL xSPI HYPERRAM™ (256Mb and above).

2 HYPERRAM™ vs JESD251 timing

This section provides a comparison between the input and output timings of the 64-Mb/128-Mb HYPERRAM™ and JESD251. Any timing gap either due to a difference in the measurement level and/or the parameter value is highlighted with supporting note and possible system workaround. Read-Write Data Strobe (RWDS) and Data-line (DQ) of HYPERRAM™ are the same as Data Strobe (DS) and Data-line (IO) of JESD251.

2.1 Input timing

Table 1 summarizes HYPERRAM™ and JESD251 input timing comparison at 200MHz clock (CK). **Figure 1** and **Figure 2** show the input measurement reference for JESD251 and HYPERRAM™. Key voltage reference levels for the input timing measurement are specified as $V_T = V_{CC}/2$, V_{IH}/V_{IL} = 70%/30% of V_{CC}. JESD251 specifies V_{DD} as the IO voltage which is the same as V_{CC}/V_{CCQ} for HYPERRAM™.

Table 1 Input timing comparison for 1.8V device

JESD251 Spec				64Mb/128Mb HYPERRAM™ Datasheet				Unit
Parameter	**Symbol**	**Min**	**Max**	**Parameter**	**Symbol**	**Min**	**Max**	
Clock Input Threshold (AC)	V_T(AC)	0.50*V_{DD}	0.50*V_{DD}	Not specified [1]				V
Input Differential Crossing (AC)	V_{IX}(AC)	0.4*V_{DD}	0.6*V_{DD}	Input Differential Crossing (AC)	V_{IX}(AC)	0.4*V_{CCQ}	0.6* V_{CCQ}	V
Cycle Time Data Transfer Mode	t_{PERIOD}	5		CK Period	t_{CK}	5		ns
Slew Rate (CK and Signals) - (1.8V)	SR	1.125		Minimum Input Rise and Fall Slew Rates (1.8V)		1.13		V/ns
Slew Rate (CK and Signals) - (3V)	SR	2.06		Minimum Input Rise and Fall Slew Rates (3.0V)		2.06		V/ns
Duty Cycle Distortion	t_{CKDCD}	0	0.25	Not specified [2]				ns
Minimum Pulse Width	t_{CKMPW}	2.25		CK Half Period - Duty Cycle	t_{CKHP}	0.45*t_{CK}	0.55 *t_{CK}	ns
Input Setup Time, with respect to V_{IH}/V_{IL}	t_{ISUddr}	0.5		Input Setup, with respect to V_T	t_{IS}	0.5		ns

HYPERRAM™ vs JESD251 timing

JESD251 Spec				64Mb/128Mb HYPERRAM™ Datasheet				Unit
Parameter	**Symbol**	**Min**	**Max**	**Parameter**	**Symbol**	**Min**	**Max**	
Input Hold Time, with respect to V_{IH}/V_{IL}	t_{IHddr}	0.5		Input Hold, with respect to V_T	t_{IH}	0.5		ns

[1]The input clock (CK) AC input threshold is not specified in the HYPERRAM™ datasheet. However, all input measurement reference for HYPERRAM™ is V_T of CK, which is identical to the JESD251 measurement reference.

[2]The clock (CK) duty cycle distortion is not specified in the HYPERRAM™ datasheet. However, HYPERRAM™ allows input clock duty cycle variation between 45% to 55% of t_{CK} or $0.5t_{CK}$ +/- $5\%t_{CK}$ which covers the t_{CKDCD} specification of JESD251.

2.1.1 JESD251 input measurement

As per JESD251 spec, the input measurement reference is V_T of CK to V_{IH}/V_{IL} of IOs, as highlighted in **Figure 1**.

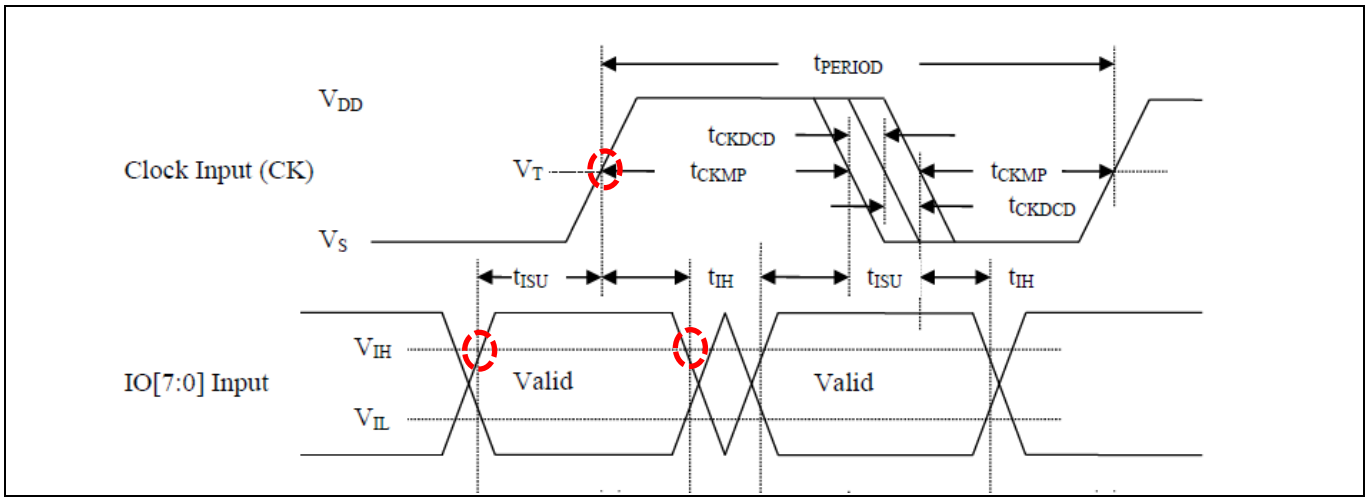

Figure 1 JESD251 input timing diagram

2.1.2 HYPERRAM™ input measurement

As per the HYPERRAM™ datasheet, the input measurement reference is V_T of CK to V_T of DQs, as highlighted in **Figure 2**.

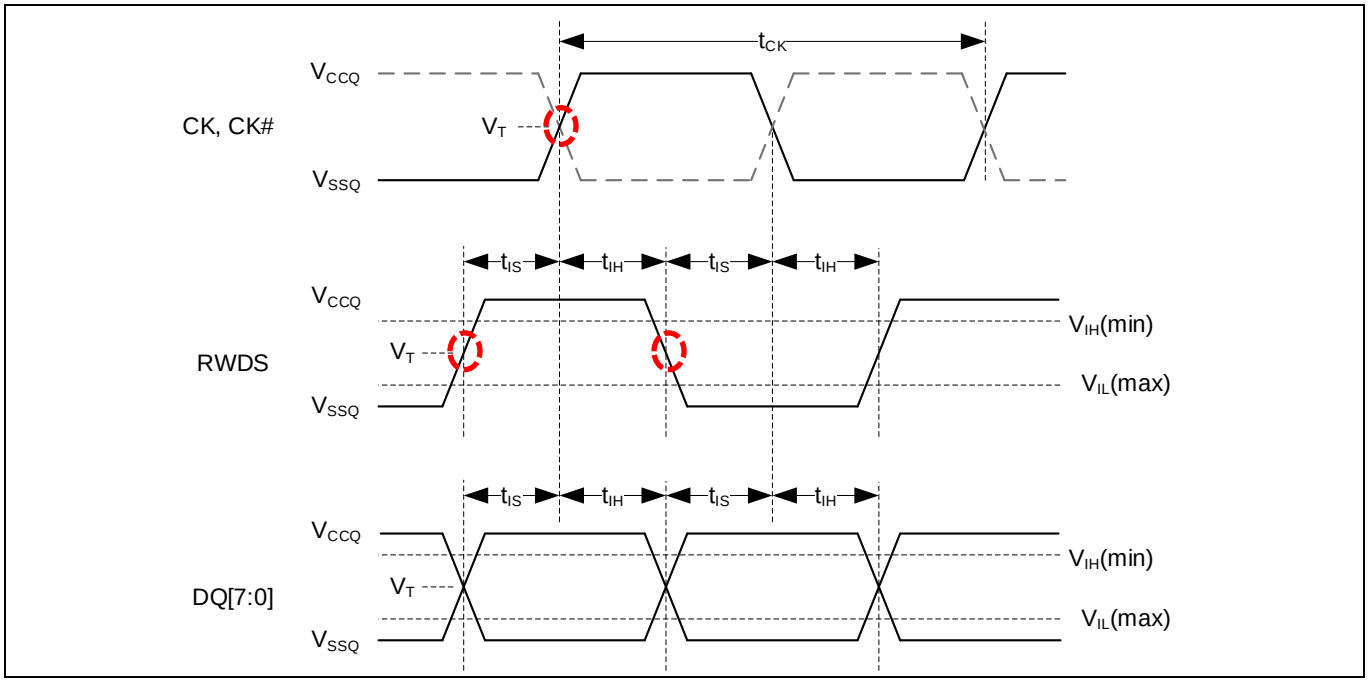

Figure 2 HYPERRAM™ input timing diagram

2.1.3 Input timing compatibility analysis

The input measurement reference level for HYPERRAM™ is CK (V_T) to DQ (V_T) while it is CK (V_T) to IO (V_{IH}/V_{IL}) for JESD251, as highlighted in **Figure 1** and **Figure 2**. This section analyzes the input timing compatibility with respect to both measurement references by translating one reference timing to other and compares both the timings at the same reference.

2.1.3.1 Analyzing with JESD251 input reference (V_T to V_{IH}/V_{IL})

If the host drives inputs as per JESD251 reference (HYPERRAM™ write operations), it will end up driving with an extra timing margin for HYPERRAM™. As highlighted in **Figure 3**, when extrapolating the HYPERRAM™ input timings from its standard V_T to V_{IH} /V_{IL}, the input timing requirement for the HYPERRAM™ @ V_{IH}/V_{IL} reduces by Δt.

For example: V_{CCQ} = 1.8V with SR=1.125V/ns for both rising and falling signal calculates Δt1/Δt2 = 0.32ns (0.2*1.8/1.125). Hence, HYPERRAM™ input setup (t_{IS}) and the input hold (t_{IH}) timing requirements at V_{IH}/V_{IL} reference will become t_{IS}/t_{IHS} @ V_T – 0.32 ns or 0.18 ns which is then compared with the host input timing @V_{IH}/V_{IL} per JESD251 spec, as shown in **Table 1**.

2.1.3.2 Analyzing with HYPERRAM™ input reference (V_T to V_T)

If the host drives inputs per HYPERRAM™ reference during the write operation, the host will end up driving with an extra timing margin for HYPERRAM™. As highlighted in **Figure 3**, when extrapolating the host input timings from its standard V_{IH} /V_{IL} to V_T, the equivalent input timing driven by the host @ V_T will increase by Δt.

For example: V_{CCQ} = 1.8V with SR=1.125V/ns for both rising and falling signal calculates Δt1/Δt2 = 0.32ns (0.2*1.8/1.125). Hence, the equivalent setup (t_{IS}) and hold (t_{IH}) timing driven by the host at V_T will become t_{IS}/t_{IHS} @ V_{OH}/ V_{OL} + 0.32 ns or 0.832 ns, which is then compared with HYPERRAM™ input timings at V_T, as shown in **Table 1**.

HYPERRAM™ vs JESD251 timing

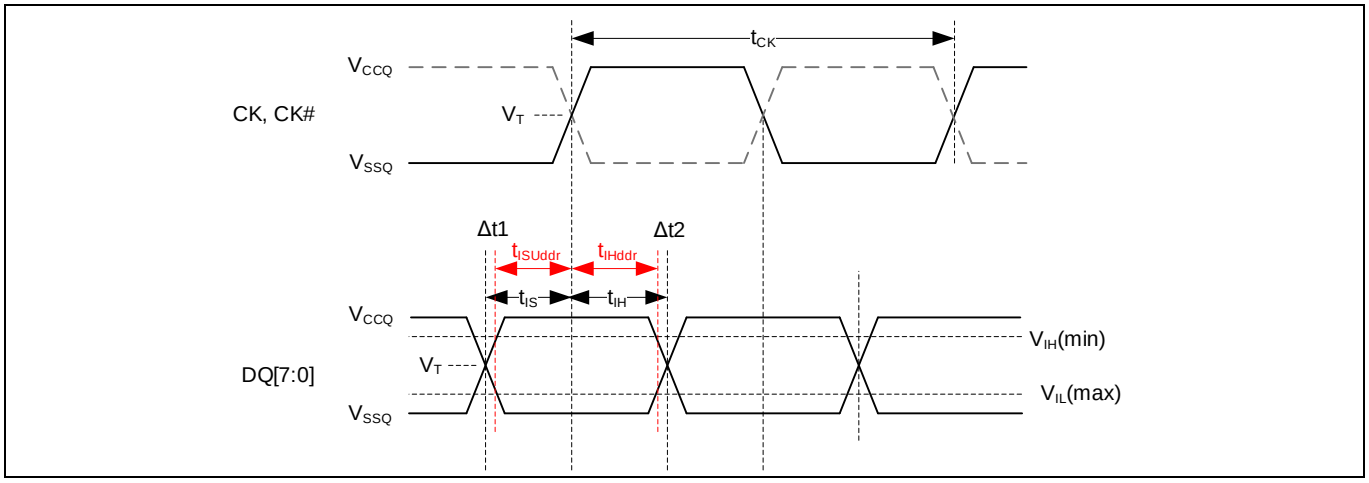

Figure 3 Input timing comparison JESD251 vs HYPERRAM™

2.2 Output timing

Table 2 summarizes HYPERRAM™ and JESD251 output timing comparison at 200MHz CK. **Figure 6** and **Figure 8** show the output measurement reference for JESD251 and HYPERRAM™. Output high voltage (V_{OH}) and output low voltage (V_{OL}) levels for the high-speed, 1.8V LVCMOS (JESD8-31) outputs are V_{OH} = 75% of V_{DD} or 0.75*V_{DD}; V_{OL} = 25% of V_{DD} or 0.25*V_{DD}.

Table 2 Output timing comparison for 1.8V device

JESD251 spec				64-Mb/128-Mb HYPERRAM™ datasheet				
Save Data Output	**Symbol**	**Min**	**Max**	**Data Output**	**Symbol**	**Min**	**Max**	**Unit**
Cycle Time Data Transfer Mode	t_{PERIOD}	5		CK Period	t_{CK}	5		ns
Duty Cycle Distortion	t_{DSDCD}	0	0.2	Not specified [0]				ns
Minimum Pulse Width	t_{DSMPW}	2.05		Not specified [4]				ns
Output skew	t_{RQ}		0.4	RWDS transition to DQ Valid [5]	t_{DSS}	-0.4	0.4	ns
Output hold skew	t_{RQH}		0.4	RWDS transition to DQ Invalid [5]	t_{DSH}	-0.4	0.4	ns

[3] t_{DSDCD} or Duty Cycle Distortion parameter is not measured on HYPERRAM™. This parameter in conjuction with t_{CKMPW} can determine the minimum pulse width (t_{DSMPW}) of the data strobe (DS/RWDS) output. Therefore, if the t_{CKMPW} (t_{CKHP}) and t_{DSMPW} are specified, t_{DSDCD} definition becomes redundant (optional).

[4] t_{DSMPW} is not provided in the HYPERRAM™ datasheet. However, characterization of t_{DSMPW} on limited HYPERRAM™ samples demonstrate that HYPERRAM™ can support t_{DSMPW} = 2.05 ns (typ) and 2.0 ns (min). See **Table 3** and **Figure 4** for more details.

[5] HYPERRAM™ RWDS and DQs are the same as DS and IO signals of JESD251.

HYPERRAM™ datasheet values for t_{DSS} and t_{DSH}, as shown in **Table 2**, are specified as per their production testing limits, while their actual measurement on the silicon is much improved. **Table 3** summarizes the improved t_{DSS}/t_{DSH} and new t_{DSMPW} of HYPERRAM™. Though these measurements are performed on limited samples they are measured across voltage, temperature, and process corners to guarantee the spec limits. Therefore, users of

this application note can take the improved timings, as per new spec limits in **Table 3**, instead of datasheet timings if they are too tight or create challenge while evaluating the 1.8V, 64Mb/128Mb HYPERRAM™.

Table 3 64 Mb/128 Mb, 1.8 V HYPERRAM™ output timing (improved)

Parameter	Symbol	Min. [6, 8]	Typ [7,8]	Max [6, 8]	Unit
Read-Write Data Strobe (RWDS) Transition to Data Valid	t_{DSS}	-0.3	-	0.3	ns
RWDS Transition to Data Invalid	t_{DSH}	-0.3	-	0.3	ns
RWDS Minimum Pulse Width	t_{DSMPW}	2.0	2.05	-	ns

[6]Test Conditions: f_{CK} = 200 MHz, V_{CC}/V_{CCQ} = 1.8 V, T_A = -40°C to +105°C, all corners.

[7]Test conditions: f_{CK} = 200 MHz, V_{CC}/V_{CCQ} = 1.8 V, T_A = -40°C to +105°C, typical corner.

[8]Values are guaranteed by characterization and not 100% tested in production.

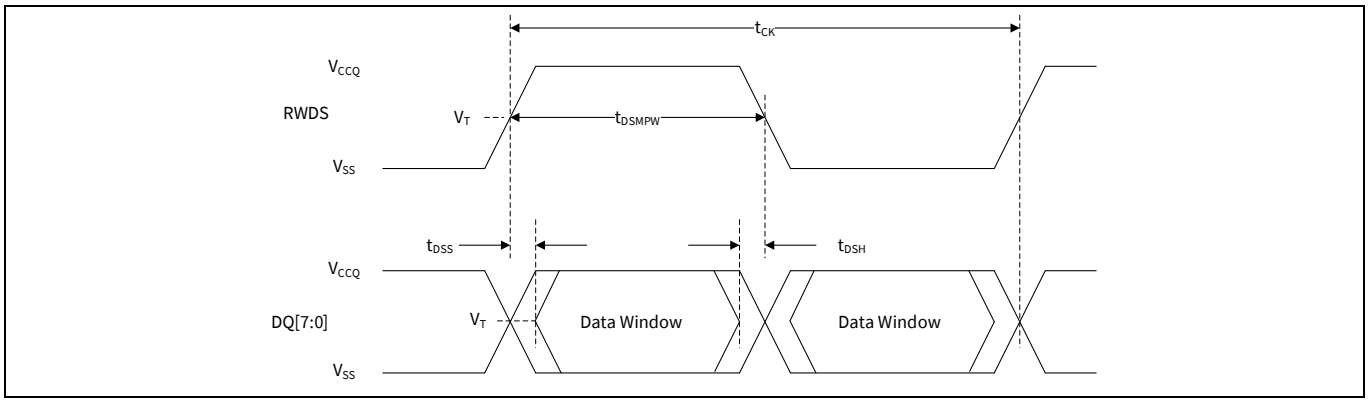

Figure 4 HYPERRAM™ output data window & t_{DSMPW}

2.2.1 JESD251 output measurement

JESD251 output parameters are measured with capacitive load $C_{REFERENCE}$ (C_L) = 6pF as, shown in **Figure 5**.

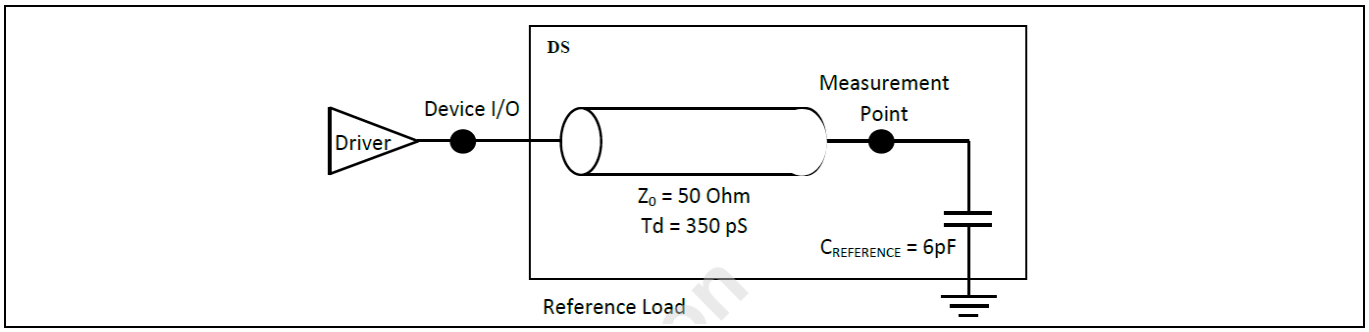

Figure 5 JESD251 output load reference

JESD251 output measurement reference is V_T of DS to V_{OH}/V_{OL} of IOs, as highlighted in **Figure 6**.

HYPERRAM™ vs JESD251 timing

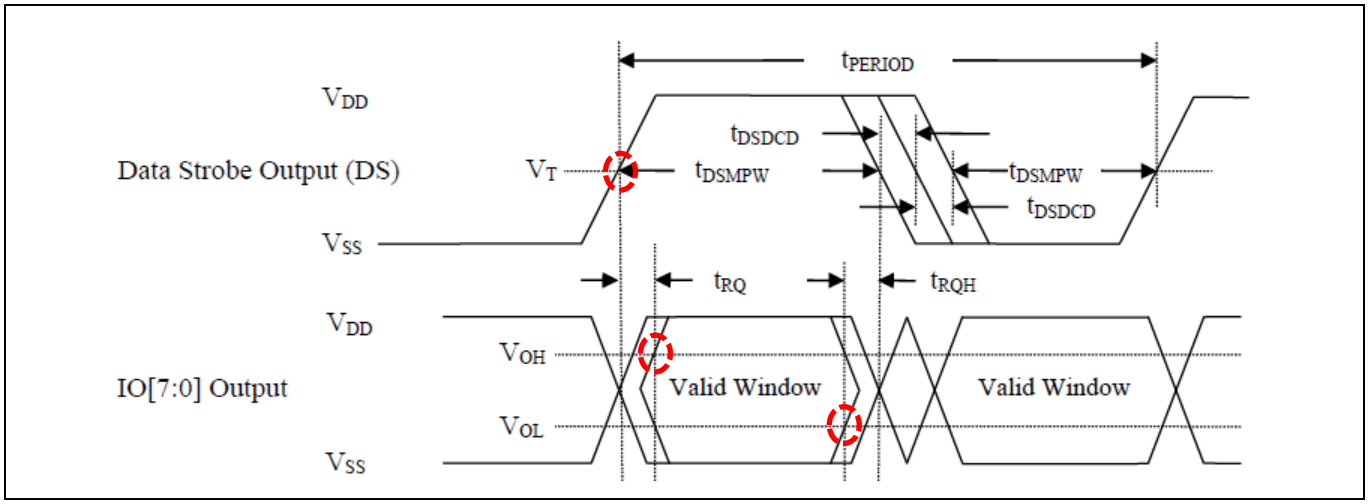

Figure 6 JESD251 data output timing

2.2.2 HYPERRAM™ Output Measurement

HYPERRAM™ output parameters are measured with capacitive load C_L ($C_{REFERENCE}$) = 15pF, as shown in **Figure 7**.

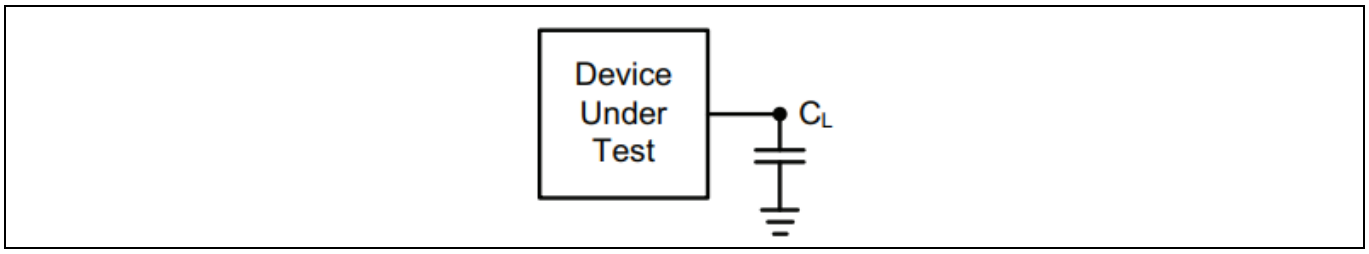

Figure 7 HYPERRAM™ output load reference

HYPERRAM™ output measurement reference is V_T of RWDS to V_T of DQs, as shown in **Figure 8**.

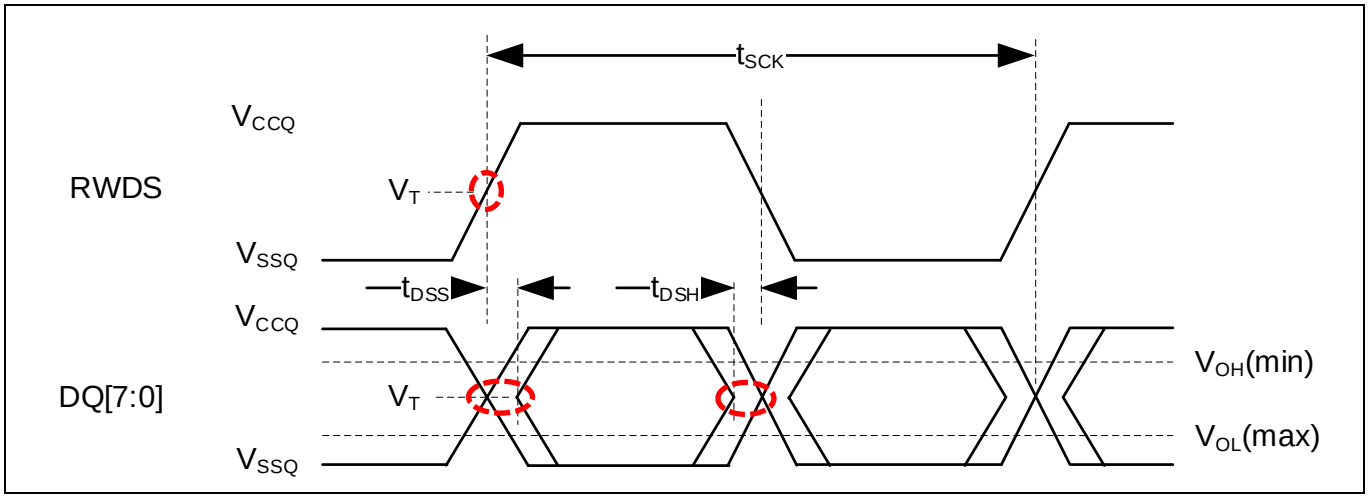

Figure 8 HYPERRAM™ data output timing

2.2.3 Output timing compatibility analysis

The output measurement reference for HYPERRAM™ is RWDS (V_T) to DQ (V_T) while it is DS (V_T) to IO (V_{OH}/V_{OL}) for JESD251, as highlighted in **Figure 6** and **Figure 8**. This section analyzes the output timing compatibility for both references by translating one reference timing to other and compares both the timings at the same reference.

2.2.3.1 Analyzing with JESD251 output reference (V_T to V_{OH}/V_{OL})

When shifting the HYPERRAM™ output reference from V_T to (V_{OH} /V_{OL}), its new t_{DSS}/t_{DSH} value at (V_{OH} /V_{OL}) reference will observe a Δt1/Δt2 increase from its standard V_T reference. The adjusted t_{DSS}/t_{DSH} for HYPERRAM™ is calculated as: t_{DSS}/t_{DSH} @ V_T (0.3ns/0.3ns) + (Δt1/ Δt2) which is then compared against host's t_{RQ}/t_{RQH} @ (V_{OH} /V_{OL}), as shown in **Table 3**.

Figure 9 highlights the Δt1/Δt2 change when shifting the HYPERRAM™ output reference from V_T to (V_{OH} /V_{OL}).

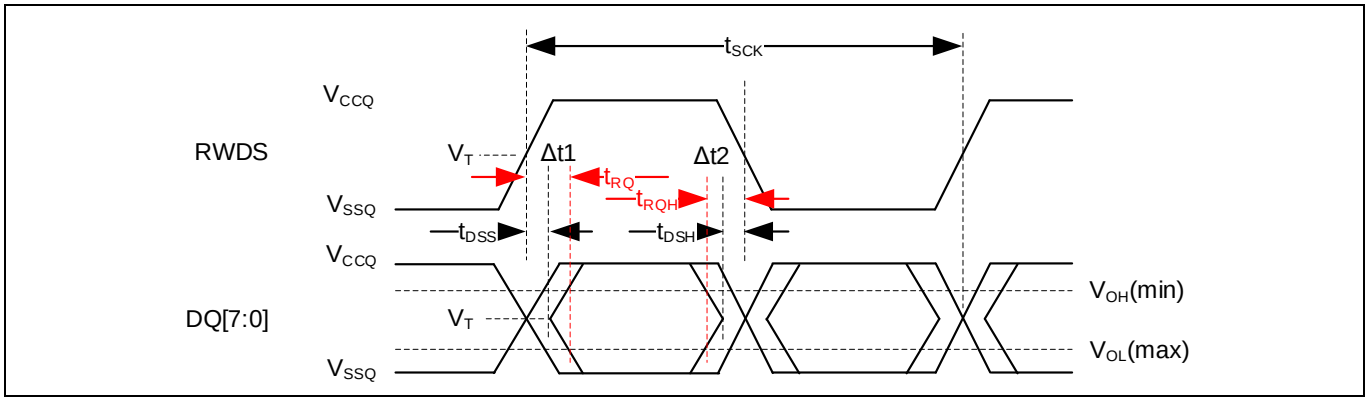

Figure 9 Output timing comparison JESD251 vs HYPERRAM™

The value of Δt shift is determined by the HYPERRAM™ output drive strength and the system bus load capacitance. **Figure 10** shows the RC charging and discharging behavior of an output buffer when it transitions from '0' to '1' (RC charging) or from '1' to '0' (RC discharging). For a given RC network, it takes ~0.7T(1.4T-0.7T)) to raise the output from V_T to V_{OH}. While it takes ~0.4*T(0.69T-0.29T) to fall the output from V_{OH} to V_T. T=RC is the time contact of the HYPERRAM™ output circuit.

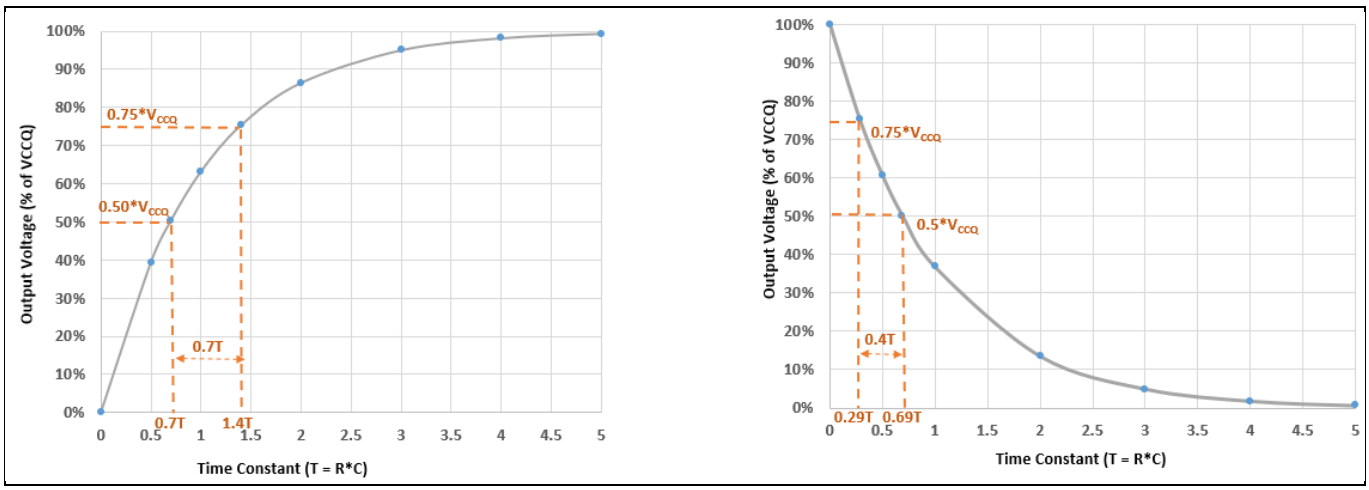

Figure 10 Output load (CL) charging and discharging characteristics

Infineon HYPERRAM™ supports configurable output drive strength whose value can vary from 19 Ω (strongest) up to 115 Ω (weakest) with 34 Ω being the default output impedance. The configurable drive strength in

HYPERRAM™ vs JESD251 timing

HYPERRAM™ applies to both DQ and RWDS outputs. **Table 4** shows the Δt for various HYPERRAM™ output drive strengths with JESD251 reference load, C_L = 6pF. HYPERRAM™ adjusted t_{DSS}/t_{DSH} is calculated as: t_{DSS}/t_{DSH} @ V_T (0.3ns/0.3ns) + Δt1/ Δt2; while the host's t_{RQ}/t_{RQH} will be as per **Table 2**.

Table 4 HYPERRAM™ adjusted t_{DSS}/t_{DSH} with RWDS (V_T) to DQ (V_{OH}/V_{OL}): CL = 6pF

R (Ω)	C_L (pF)	0.7*T(RC) (Δt1) (ps)	0.4*T(RC) (Δt2) (ps)	HYPERRAM™ adjusted t_{DSS}/t_{DSH} with reference (RWDS (V_T) to DQ (V_{OH}/V_{OL}))			
				t_{DSS} (ns)		t_{DSH} (ns)	
				Min	Max	Min	Max
19	6	79.8	45.6	-0.380	+0.380	-0.346	+0.346
34	6	142.8	81.6	-0.443	+0.443	-0.382	+0.382

Table 5 shows the Δt for various HYPERRAM™ output drive strength with C_L = 15pF.

Table 5 HYPERRAM™ adjusted t_{DSS}/t_{DSH} with RWDS (V_T) to DQ (V_{OH}/V_{OL}): CL = 15pF

R (Ω)	C_L (pF)	0.7*T(RC) (Δt1) (ps)	0.4*T(RC) (Δt2) (ps)	HYPERRAM™ adjusted t_{DSS}/t_{DSH} with reference (RWDS (V_T) to DQ (V_{OH}/V_{OL}))			
				t_{DSS} (ns)		t_{DSH} (ns)	
				Min	Max	Min	Max
19	15	199.5	114	-0.50	+0.50	-0.414	+0.414
34	15	357	204	-0.657	+0.657	-0.504	-0.504

-Green text color indicates adjusted new HYPERRAM™ limits are within the host's spec min
-Orange text color indicates adjusted new HYPERRAM™ limits are off by <15% of the host's spec min
-Red text color indicates adjusted new HYPERRAM™ limits are >15% off the host's spec min

2.2.3.2 Analyzing with HYPERRAM™ output reference (V_T to V_T)

When shifting the host's output reference from (V_{OH} /V_{OL}) to V_T, its new t_{RQ}/t_{RQH} spec value at (V_T) reference will observe Δt1/ Δt2 decrease from its standard (V_{OH}/ V_{OL}) reference. The adjusted t_{RQ}/t_{RQH} for the host will be calculated as: t_{RQ}/t_{RQH} @ V_{OH}/ V_{OH} (0.4ns/0.4ns) – (Δt1/ Δt2) which is then compared against HYPERRAM™ t_{DSS}/t_{DSH} @ V_T, as shown in **Table 3**.

Figure 9 highlights the Δt1/ Δt2 change when shifting the host output timing measurement reference from (V_{OH} /V_{OL}) to V_T.

Table 6 shows the Δt for various HYPERRAM™ output drive strengths with JESD251 reference load, C_L = 6pF.

Table 6 Host's adjusted t_{DSS}/t_{DSH} with DS (V_T) to IO (V_T): CL = 6pF

R (Ω)	C_L (pF)	0.7*T(RC) (Δt1) (ps)	0.4*T(RC) (Δt2) (ps)	Host's adjusted t_{RQ}/t_{RQH} with reference (DS (V_T) to IO (V_T)			
				t_{RQ} (ns)		t_{RQH} (ns)	
				Min	Max	Min	Max
19	6	79.8	45.6	-0.320	+0.320	-0.354	+0.354
34	6	142.8	81.6	-0.257	+0.257	-0.318	+0.318

Table 7 shows the Δt for various HYPERRAM™ output drive strength with C_L = 15pF.

HYPERRAM™ vs JESD251 timing

Table 7 Host's adjusted t_{DSS}/t_{DSH} with DS (V_T) to IO (V_T): CL = 15pF

R (Ω)	C_L (pF)	0.7*T(RC) (Δt1) (ps)	0.4*T(RC) (Δt2) (ps)	Host's adjusted t_{RQ}/t_{RQH} with reference (DS (V_T) to IO (V_T)			
				t_{RQ} (ns)		t_{RQH} (ns)	
				Min	Min	Min	Min
19	15	199.5	114	-0.20	+0.20	-0.286	+0.286
34	15	357	204	-0.043	+0.043	-0.196	+0.196

-Green text color indicates adjusted new limits for the host are within the HYPERRAM™ spec min
-Orange text color indicates adjusted new limits for the host are off by <15% of the HYPERRAM™ spec min
-Red text color indicates adjusted new limits for the host are >15% off the HYPERRAM™ spec min

3 Document References

Datasheets

[1] **64-Mb HYPERRAM™ self-refresh DRAM with HYPERBUS™ interface**

[2] **128-Mb HYPERRAM™ self-refresh DRAM with HYPERBUS™ interface**

[3] **64-Mb HYPERRAM™ self-refresh DRAM with octal SPI interface**

[4] **128-Mb HYPERRAM™ self-refresh DRAM with octal SPI interface**

[5] **256-Mb HYPERRAM™ self-refresh DRAM with HYPERBUS™ interface**

[6] **512-Mb HYPERRAM™ self-refresh DRAM with HYPERBUS™ interface**

[7] **256-Mb HYPERRAM™ self-refresh DRAM with octal SPI interface**

[8] **512-Mb HYPERRAM™ self-refresh DRAM with octal SPI interface**

Application notes

[9] **AN226576** – Getting Started with HYPERRAM™

[10] **AN211622** - HYPERFLASH™ and HYPERRAM™ Layout Guide

[11] **AN218684** - HYPERBUS™ Memory: Guide to Efficient Data Access

Ecosystem

[12] **Chipset Partners**

Specifications

[13] JESD251 - Optional x4 quard I/O with data strobe

[14] **HYPERBUS™ specification**

[15] **Expended Serial Peripheral Interface (xSPI) for non-volatile memory devices, version 1.0 JESD251B**

[16] **1.8 V HIGH-SPEED LVCMOS (HS_LVCMOS) interface JESD8-31**

Revision history

Document version	Date of release	Description of changes
**	2022-01-12	Initial release

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