Enabling chipset support of Infineon flash memory devices

About this document

Scope and purpose

This application note provides best practices, recommendations, advices, and details on Infineon supporting tools to enable a chipset manufacturer to develop support and complete qualification for an Infineon memory device on its chipset.

Numerous milestones for such an infrastructure support and qualification processes will be discussed, and recommendations will be provided accordingly.

Intended audience

This application note is intended for chipset manufacturers planning to support Infineon memory device as well as for customers wanting to use an Infineon memory device with a given chipset.

Taxonomy:

Through this application note, the term “chipset” will cover System-on-Chip (SoC), MCU, MPU, and FPGA.

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1 Memory controller support and selection

Multiple serial Flash memory interfaces and protocols exist such as Quad I/O SPI (in SDR and/or in DDR mode), Dual Quad I/O SPI (SDR and/or DDR), HYPERBUS™ (8-pin serial), Octal xSPI, x16 SPI.

A memory controller can support one or more of these protocols by sharing interface pins. For example, it is relatively common for a chipset to support Quad I/O SPI (SDR and DDR), Dual Quad I/O SPI (SDR and DDR), HYPERBUS™ and Octal xSPI protocols using a common memory interface up to 8-bit width. Chipset manufacturers can develop their own memory controller or rely on third-party memory controller providers.

To help chipset manufacturers to develop their own memory controller, Infineon provides the HYPERBUS™ protocol specification, available at this link: **https://www.cypress.com/file/213356/download**
The HYPERBUS™ protocol encompass both HYPERFLASH™ and HYPERRAM™ memory devices.

Additionally, Infineon provides free-of-charge HYPERBUS™ memory controller RTL IP for chipset partners who want to integrate that IP as a hard IP in their chipset, or for customers willing to integrate that IP as soft IP in an FPGA to enable memory expansion.

The HYPERBUS™ memory controller can be requested by filling a form on our website at this link: **https://www.cypress.com/documentation/software-and-drivers/hyperbus-master-interface-controller-ip-intellectual-property**

Note: *HYPERBUS™ memory controller only supports HYPERBUS™ protocol and not Octal xSPI, Quad I/O SPI, or Dual Quad I/O SPI protocols.*

Note: *HYPERBUS™ memory controller is compliant with generation 1 of HYPERBUS™ protocol, but is not compliant with JEDEC JESD251 xSPI (profile 2) standard.*[1]

[1] eXpanded Serial Peripheral Interface (xSPI) for non-volatile memory devices, version 1.0:
https://www.jedec.org/system/files/docs/JESD251A.pdf
Access to the document requires an active JEDEC membership.

Memory controller support and selection

See **Table 1** for a list of memory controller options for HYPERBUS™ and/or JEDEC xSPI support.

Table 1 Memory controller options

IP partner	Memory protocols supported	Link	Incorporable as hard IP
Arasan	JEDEC xSPI JESD251 profile 1 (Octal xSPI) and profile 2 (HYPERBUS™), Quad/Dual/Single I/O SPI	**https://www.arasan.com/product/xspi-master-ip-nor-ip/**	Hard IP
Cadence®	HYPERBUS™ 1.0, Octal xSPI, Quad/Dual/Single I/O SPI	**https://ip.cadence.com/uploads/1197/cdn-dsd-mem-fla-controller-and-phy-ip-for-qspi-hyperflash-pdf**	Hard IP
	JEDEC xSPI JESD251 profile 1 (Octal xSPI), HYPERBUS™, Quad/Dual/Single I/O SPI	**https://ip.cadence.com/uploads/1244/cdn-dsd-mem-fla-host-controller-ip-for-xspi-pdf**	Hard IP
Mobiveil	HYPERBUS™ 1.0	**http://mobiveil.com/hyperbus/**	Hard IP
Synaptic Laboratories Ltd.	HYPERBUS™ 1.0 (HYPERRAM ™ 1.0, HYPERFLASH™, HyperMCP)	**https://synaptic-labs.com/sll-hyperbus-memory-controller-hbmc-ip/**	Soft IP
	JEDEC xSPI JESD251 profile 1 (Octal xSPI) and profile 2 (HYPERBUS™)	**https://synaptic-labs.com/ip-mbmc3-main-product/**	Soft IP – potentially hard IP
Synopsys	JEDEC xSPI JESD251 profile 1 (Octal xSPI) and profile 2 (HYPERBUS™), Dual Quad/Quad /Dual/Single I/O SPI	**https://www.synopsys.com/dw/ipdir.php?ds=amba_ssi**	Hard IP

*Note: Visit **https://www.cypress.com/hyperbus-chipset-support** to ensure that you access the latest revision of third-party Flash memory IP solutions.*

1.1 Quad I/O SPI (QSPI)

While Octal/HYPERBUS™ xSPI is standardized at JEDEC (JESD251 profile 1/profile 2 respectively), Quad I/O SPI (QSPI) protocol is not. Consequently, some commands have different operands depending of QSPI Flash memory vendors.

In order to offer maximum flexibility to chipset partners and customers and to ease their software design, Infineon Flash memory products implement several operands for a same command to match alternative supplier operands. For example, both “EBh” and “ECh” are valid operands for the *Quad I/O Read* command. Similarly, both “02h” and “12h” are valid operands for the *Page Program* command.

Many third-party IP vendors provide QSPI (SDR and/or DDR) memory controller IP. See the above list for Octal / HYPERBUS™ xSPI controller IP providers—many of these partners also provide a QSPI memory controller IP.

2 Boot support and implementation

After the processor has powered-up, **boot sequence** immediately happens. The boot process between the Flash and the processor can be handled in the following ways:

- **Using the ROM**
- **Using SFDP parameters**

2.1 Using the ROM

In this approach, the processor fetches the Flash Manufacturer ID and/or the Flash Device ID and starts the boot process if either one or both of the returned IDs match the values stored in its boot ROM.

2.1.1 Implementation

The Flash Manufacturer ID and Flash Device ID can be read through the Read Device Identification transaction command, usually '9Fh'. The manufacturer identification is assigned by JEDEC. The device identification is assigned by Infineon, and vary across Flash families and Flash densities within a given family.

2.1.2 Recommendations

For legacy Infineon Flash memory up to (and including) 65nm MIRRORBIT™ and 65nm Floating Gate Flash process technologies, the Manufacturer ID is '01h' (this corresponds to the legacy AMD/Spansion Manufacturer ID).

Starting with SEMPER™ Flash based on the 45nm MIRRORBIT™ process technology, the Flash Manufacturer ID is '34h' (this corresponds to the legacy CYPRESS™ Manufacturer ID).

The list of Flash Manufacturer IDs is maintained by JEDEC in JEDEC JEP106BC[1] document.

2.2 Using SFDP parameters

Serial Flash Discoverable Parameters (SFDP) is a JEDEC standard (JESD216[2]) that provides device feature and configuration information. The SFDP standard defines a common parameter table describing important device characteristics and serial access methods used to read the parameter table data. These parameter tables can be interrogated by the host system software to enable adjustments needed to accommodate divergent features from multiple Flash vendors. JESD216 Rev D (JESD216D) is the latest revision of SFDP standard covering Octal SPI and HYPERBUS™ protocols.

2.2.1 Implementation

When relying on SFDP, the host does not know initially (i.e., immediately after boot) what type of Flash memory device has been attached to it. It could be a Quad I/O SPI Flash in Single Data Rate (SDR) or in Dual Data Rate (DDR) mode, an Octal xSPI Flash, or a serial Flash with HYPERBUS™ Interface. Therefore, the host memory controller will boot in the lowest common denominator across these families of Flash, i.e., in SPI Single I/O and SDR mode. The frequency will be low, as access to SFDP parameters can only be done up to 50-MHz SDR frequency. Access to SFDP always has a dummy cycle of eight.

[1] JEDEC JEP106BC: **https://www.jedec.org/system/files/docs/JEP106BC.pdf**
Access to the document requires an active JEDEC membership.

[2] JEDEC JESD216 standard: **https://www.jedec.org/system/files/docs/JESD216D-01.pdf**
Access to the document requires an active JEDEC membership.

Boot support and implementation

The following is an example of how to use SFDP to configure the host memory controller from 1S-1S-1S mode to 8D-8D-8D mode for Octal SPI Flash:

See the Octal xSPI S28HS-T datasheet from CYPRESS SEMPER™ Access Program[1].

1. The Octal xSPI Flash powers-up in 1S-1S-1S mode, i.e., Command/Address and Data are all in Single I/O and in SDR mode.
2. The host reads JEDEC SFDP byte addresses 00h to 07h with command 5Ah (1-1-1) and 8 Wait States (WS).

Table 2 Verification of compliance with SFDP Rev D

SFDP header		SEMPER™ S28HS-T data
Signature	Address bytes 00h to 03h	“50444653h”
SFDP minor revision	Address byte 04h	“08h” (JEDEC JESD216 Revision D)
SFDP major revision	Address byte 05h	“01h” (JEDEC JESD216 Revision D)
xSPI Profile 1	Address byte 07h	“FEh” (xSPI NOR Profile 1 Octal, (8D, 8D, 8D) operation, 4-byte addressing for SFDP command, 8 WAIT states (booting in 1S-1S-1S mode)

3. The host reads SFDP “Status, Control and Configuration Register Map DWORD-3” at SFDP addresses 174h to 177h for Infineon SEMPER Octal SPI Flash. See **Table 3**.

Table 3 Number of dummy cycles used for generic addressable read status/control register

174h	Status, Control and Configuration Register Map DWORD-3	C0h	Bit 31 = Generic Addressable Read Status/Control register command for volatile registers supported for some (or all) registers = 1b Bit 30 = Generic Addressable Write Status/Control register command for volatile registers supported for some (or all) registers = 1b Bits 29:28 = Number of address bytes used for Generic Addressable Read/Write Status/Control register commands for volatile registers = 3 byte (default) = 10b Bit 27:26 = Number of dummy bytes used for Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode = 10b Bit 25:14 = Not supported = FFFh Bit 13:10 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (8S-8S-8S) mode = 3 = 0011b Bit 9:6 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (8D-8D-8D) mode = 3 = 0011b Bit 5:4 = Reserved = 00b Bit 3:0 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode = 0000b
175h		CCh	
176h		FFh	
177h		EBh	

   - This DWORD provides the number of dummy cycles used for the Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode. The SFDP table shows that these configuration registers are accessed in 3-byte addressing mode, which is the default mode for SEMPER™ Flash in 1S-1S-1S access.
4. The host reads SFDP “Command Sequences to Change to Octal DDR (8D-8D-8D) mode DWORD-1 to -4” at SFDP addresses 1DCh to 1EBh for Infineon SEMPER Octal SPI Flash. See **Table 4**.

[1] CYPRESS™ SEMPER™ Access Program: **https://go.cypress.com/semper-access-program-ap**

Boot support and implementation

Table 4 Commands needed to switch from 1S-1S-1S mode to 8D-8D-8D mode

1DCh	Command Sequences to Change to Octal DDR (8D-8D-8D) mode DWORD -1	00h	Bits 7:0 = Byte 3 of first command sequence
1DDh		00h	Bits 15:8 = Byte 2 of first command sequence
1DEh		06h	Bits 23:16 = Byte 1 of first command sequence
1DFh		01h	Bits 31:24 = Length of first command sequence = 1 byte
1E0h	Command Sequences to Change to Octal DDR (8D-8D-8D) mode DWORD -2	00h	Bits 7:0 = Byte 7 of first command sequence
1E1h		00h	Bits 15:8 = Byte 6 of first command sequence
1E2h		00h	Bits 23:16 = Byte 5 of first command sequence
1E3h		00h	Bits 31:24 = Byte 4 of first command sequence
1E4h	Command Sequences to Change to Octal DDR (8D-8D-8D) mode DWORD -3	00h	Bits 7:0 = Byte 3 of second command sequence - volatile register address
1E5h		80h	Bits 15:8 = Byte 2 of second command sequence - volatile register address
1E6h		71h	Bits 23:16 = Byte 1 of second command sequence
1E7h		05h	Bits 31:24 = Length of second command sequence = 5 bytes
1E8h	Command Sequences to Change to Octal DDR (8D-8D-8D) mode DWORD -4	00h	Bits 7:0 = Byte 7 of second command sequence
1E9h		00h	Bits 15:8 = Byte 6 of second command sequence
1EAh		43h	Bits 23:16 = Byte 5 of second command sequence - volatile register address
1EBh		06h	Bits 31:24 = Byte 4 of second command sequence - volatile register address

- DWORD-1 and DWORD-2 shows *1-byte* length command sequence and “06h” as the command, which corresponds to *Write Enable*.
- DWORD-3 and DWORD-4 shows a *5-bytes sequence* with values “71h”, “80h”, “00h”, “06h”, “43h” which correspond to the *Write Any Register* command at address 800006h with the write value “43h”.

This address corresponds to Volatile Configuration register 5 (CFR5V).

Table 5 Register addresses

Function	Register type	Register name	Volatile component address (hex)	Non-volatile component address (hex)
Device status	Status register 1	STR1N[7:0], STR1V[7:0]	0x00800000	0x00000000
	Status register 2	STR2V[7:0]	0x00800001	N/A
Device configuration	Configuration register 1	CFR1N[7:0], CFR1V[7:0]	0x00800002	0x00000002
	Configuration register 2	CFR2N[7:0], CFR2V[7:0]	0x00800003	0x00000003
	Configuration register 3	CFR3N[7:0], CFR3V[7:0]	0x00800004	0x00000004
	Configuration register 4	CFR4N[7:0], CFR4V[7:0]	0x00800005	0x00000005
	Configuration register 5	CFR5N[7:0], CFR5V[7:0]	0x00800006	0x00000006

The value “43h” corresponds to the Octal interface and protocol selection – I/O width set to 8 bits (8-8-8): CFR5V[0] and selection of Octal SPI in DDR Mode: CFR5V[1].

Table 6 Configuration register 5 description

Bit number	Name	Function	Read/Write N = Non-volatile V = Volatile	Factory default	Description
CFR5N[7] CFR5V[7]	RESRVD	Reserved for future use	N -> R/W V -> R/W	0	These bits are Reserved for future use. This bit must always be written/loaded to its default state.
CFR5N[6] CFR5V[6]	RESRVD	Reserved for future use	N -> R/W V -> R/W	1	
CFR5N[5:2] CFR5V[5:2]	RESRVD	Reserved for future use	N -> R/W V -> R/W	0000	
CFR5N[1] CFR5V[1]	SDRDDR	Octal SPI SDR or DDR selection	N -> R/W V -> R/W	0	Description: The SDRDDR bit selects between SDR or DDR for all data transfers to the device. Based on SDRDDR selection, all transactions either are SDR or DDR. **Note** SDRDDR bit only controls the interface for octal mode (8-8-8). Selection options: 0 = SDR enabled 1 = DDR enabled Dependency: N/A
CFR5N[0] CFR5V[0]	OPI-IT	Octal interface and protocol selection – I/O width set to 8 bits (8-8-8)	N -> R/W V -> R/W	0	Description: The OPI-IT bit selects the I/O width of the device to be 8-bits wide. When configured to 8-bits (OPI-IT) all transactions required Opcode, address and data always sent on all eight I/Os. Selection options: 0 = Data width set to 1bit wide (1x) – Legacy single SPI protocol 1 = Data width set to 8-bit wide (8x) – Octal protocol Dependency: N/A

The following provides an alternative configuration flow to configure the host memory controller from 1S-1S-1S mode to 8D-8D-8D mode for Octal SPI Flash:

5. Check whether the flash is compliant with SFDP JESD216 Rev D standard. See the section **2.2.1** to learn how.
6. Scan through the basic Flash parameters table (starting at SFDP address 100h for Infineon SEMPER Octal SPI S28HS-T):
   - DWORD-1 (address 100h to 103h): Indicates whether the default access is in 3-bytes or 4-bytes addressing mode
   - DWORD-2 (address 104h to 107h): Indicates the Flash density in bits

- DWORD-18 (address 144h to 147h): Indicates whether the high byte and low byte of the 16-bit words are in the same order when read in 1-1-1 mode and 8-8-8 mode
- DWORD-20 (address 14Ch to 14Fh): Indicates the maximum operation speed of devices in 8S-8S-8S mode when using the data strobe

7. Scan through JEDEC xSPI profile 1.0 DWORD-1 (starting at SFDP address 158h):
   - DWORD-1 (SFDP address 158h to 15Bh): Indicates dummy cycles for 8D-8D-8D, initial latency for various read Commands
   - DWORD-3 (SFDP address 160h to 163h): Provides information on various supported commands
   - DWORD-4 (SFDP address 164h to 167h) and DWORD-5 (SFDP address 168h to 16Bh): Provide the number of dummy cycles required for 100MHz DDR, 133 MHz DDR, 166 MHz DDR, and 200 MHz DDR read operations. DWORD-4 is helpful to move from the initial 50MHhz frequency to 200 MHz DDR or 166 MHz DDR high frequency for maximum throughput and performance of the Flash

2.2.2 Recommendations

Relying on Flash Device IDs hard-coded in the boot ROM enables optimized configuration of the memory controller for the selected Flash device. However, such scheme is not at all flexible; adding a new flash not originally supported into the SoC boot ROM would require a costly ROM re-spin. On the other hand, relying on SFDP parameters enables maximum flexibility across various Flash manufacturers who support SFDP. Furthermore, next-generation Flash memory not yet available at the time of the SoC design can be supported later on by the SoC. This enables potential cost reduction on the Flash memory side when adding support for new features or increasing the memory frequency.

Infineon Flash memory products with SFDP support starts with 65nm MIRRORBIT™ families and continue onwards. Note the following:

- For 1.8V QSPI S25FS-S family: all densities (64 Mb to 1 Gb) support SFDP Rev D
- 3V QSPI S25FL-S family: Only the 512Mb density (S25FL512S) supports SFDP Rev D
- SEMPER Flash: all SEMPER Flash supports SFDP Rev D

3 Modelization and system-level simulation

3.1 Memory controller Verification IP (VIP)

Once the memory controller IP (host IP) has been developed, it's important to verify whether it accurately implements the protocols (QSPI, HYPERBUS™, Octal SPI) it intends to support, as well as the commands and timings required to support Infineon memory devices. Such verification is typically done by using a Verification IP (VIP) and corresponding test suite.

Infineon does not directly deliver memory controller VIP, but has partnered with third-party partners notably Cadence® and Siemens. **Table 7** lists of some of Cadence® models available at the time of writing of this document. Contact Cadence® for the latest information of availability of Verification IP (VIP).

Table 7 Cadence® models available

Cadence® Verification IP (VIP)	Hyperlink
HYPERFLASH™ (1.8V and 3V)	**https://ip.cadence.com/ipportfolio/verification-ip/memory-models/non-volatile-memory/memory-model-for-hyperflash**
SEMPER™ Flash x8 SPI (1.8V and 3V)	**https://ip.cadence.com/ipportfolio/verification-ip/memory-models/non-volatile-memory/xspi**
QSPI (1.8V and 3V)	**https://ip.cadence.com/ipportfolio/verification-ip/memory-models/non-volatile-memory/q-spi-quad-spi**
HYPERRAM™ 1.0 & HYPERRAM™ 2.0 (1.8V and 3V)	**https://ip.cadence.com/ipportfolio/verification-ip/memory-models/flash/memory-model-vip-for-hyperram**

Contact Siemens for the latest information on EDA Questa® Verification IP (QVIP) availability: **https://static.sw.cdn.siemens.com/siemens-disw-assets/public/78814/en-US/Siemens-SW-QVIP-Flash-FS-83680-C1.pdf**

3.2 Simulation of memory and chipset

Before taping out a chipset, simulation at system-level must be done to verify and validate the architecture implemented and the S/W developed. A common first-stage approach is to simulate the chipset and the memory at the system level in a Verilog environment. Another possibility, or a second step, is to emulate the chipset into an FPGA target and use Verilog models of the memory devices (Flash, HYPERRAM™) to test the FPGA target.

Infineon provides Verilog models of its Flash and HYPERRAM™ memory devices, which can be accessed directly on the website as indicated in **Table 8**.

Table 8 Verilog models of Flash and HYPERRAM™ memory devices

Memory type/OPN	Hyperlink	Note
QSPI Flash (1.8V and 3V)	**https://www.cypress.com/products/serial-nor-flash-memory#tabs-0-bottom_side-7**	
HYPERFLASH™ and HYPERMCP (1.8V & 3V)	**https://www.cypress.com/search/all?sort_by=changed&f%5B0%5D=meta_type%3Asoftware_tools&f%5B1%5D=field_related_products%3A85756&f%5B2%5D=software_tools_meta_type%3A580**	

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Memory type/OPN	Hyperlink	Note
HYPERRAM™ 2.0 (1.8V and 3 V) x8 SPI Interface	**https://www.cypress.com/documentation/models/verilog/verilog-model-octal-spi-interface?source=search&cat=software_tools**	
HYPERRAM™ 2.0 (1.8V and 3 V) HYPERBUS™ Interface	**https://www.cypress.com/documentation/models/verilog/verilog-model-hyperbus-interface?source=search&cat=software_tools**	
SEMPER™ Flash (QSPI, Octal xSPI, HYPERBUS™)	**https://go.cypress.com/semper-access-program-ap**	Register to SEMPER™ Access Program to access Verilog models

Additionally, third-party providers such as Cadence® have a portfolio of Flash memory models (Denali models) which also include models for Infineon Memory Solutions: **https://ememory.cadence.com/en/user/login.jsp?nocache=MTYzMDM0NTgyODExNQ%3D%3D**. Contact Cadence® for the latest information on availability of Infineon flash memory models.

When emulating a chipset in an FPGA target, you can use one of the following:

- Verilog model of that memory (see **Table 8**)
- Physical sample of the Flash memory connected to the FPGA
- Dedicated memory models optimized for the emulator

Note: Infineon does not provide optimized memory models for the emulator but has partnered with third-party providers. For example, Cadence has optimized memory models for their Palladium emulation systems. Contact Cadence for information about Infineon memory models available for their Palladium emulation system.

3.3 IBIS models

In addition to the behavioral and timing validation done using the Verilog model of the devices (chipset and memory), another usual validation is done by using I/O Buffer Information Specification (IBIS) files.

IBIS models contain data made up of the current and voltage values in output and input pins, and the voltage and time relationship at the output pins under rising or falling switching conditions. IBIS models are intended to be used for signal integrity analysis on systems boards.

Table 9 IBIS models of Infineon memory devices

Memory type / OPN	Hyperlink	Note
QSPI Flash (1.8V and 3V)	**https://www.cypress.com/products/serial-nor-flash-memory#tabs-0-bottom_side-7**	
HYPERFLASH™ (1.8V and 3V)	**https://www.cypress.com/search/all?sort_by=changed&f%5B0%5D=meta_type%3Asoftware_tools&f%5B1%5D=field_related_products%3A85756&f%5B2%5D=software_tools_meta_type%3A580&page=1**	
HYPERMCP (3V)	**https://www.cypress.com/products/128mb-512mb-30v-hyperflash-kl-and-64mb-hyperram-mcp-hyperbus-interface#tabs-0-bottom_side-5**	

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HYPERRAM™ 2.0 (1.8V and 3V) HYPERBUS™ Interface	*Under development*	
SEMPER™ Flash (QSPI, x8 SPI, HYPERBUS™)	**https://go.cypress.com/semper-access-program-ap**	Register to SEMPER™ Access Program to access IBIS models

4 Recommendations for high-frequency memory support

4.1 HYPERBUS™ and Octal SPI memory devices

By introducing x8-bit HYPERBUS™, Infineon Memory Solutions raised the traditional level of performance and throughput reached by NOR Flash, enabling up to 333MB/s bandwidth. With the new generation of SEMPER™ and HYPERRAM™ 2.0 memory devices, throughput can go up to 400 MB/s (200 MHz DDR). The maximum throughput differs depending of the Flash voltage (1.8 V, 3 V). Also, clock support and implementation differ across memory generation.

Table 10 Memory controller options

		HYPERFLASH™ HYPERRAM™ 1.0	SEMPER™ Flash (HYPERBUS™ and x8 Octal xSPI) HYPERRAM™ 2.0
Throughput (frequency)	1.8V	333 MB/s (166 MHz DDR)	400 MB/s (200 MHz DDR)
	3V	200 MB/s (100 MHz DDR)	333 MB/s (166 MHz DDR)
Clock	1.8V	CK and CK#: two Clock signals in opposite phase[1]	x8 Octal xSPI: CK, single-ended clock HYPERBUS™: user configurable - CK, single-ended clock or CK & CK#, two clock signals in opposite phase
	3V	CK: Single-ended clock	CK: Single-ended clock
DDR Center Aligned Read Strobe (DCARS)[2]	1.8V	Two signals: Phase Shifted Clock (PSC); Phase Shifted Clock in opposite phase (PSC#)	Not supported
	3V	One Phase Shifted Clock (PSC)	Not supported
Read write data strobe (RWDS)[3]	1.8V & 3V	Supported (HYPERFLASH™ uses RWDS only as a read data strobe)	Supported (SEMPER™ uses RWDS only as a read data strobe)

Infineon Memory Solutions works directly with ecosystem partners to ensure that HYPERBUS™ memory devices (HYPERFLASH™, HYPERRAM™), SEMPER™ Flash (with HYPERBUS™ interface and with Octal xSPI interface) are fully compatible and qualified with existing and new chipsets. This effort ensures that Infineon memory devices can be easily paired with chipsets from industry-leading manufacturers while shortening customers' embedded system design cycles.

See this web page for the latest information on HYPERBUS™ chipset support. Note that this list is regularly updated with new relevant chipsets: **https://www.cypress.com/hyperbus-chipset-support**

4.2 Quad I/O SPI

As the Double Data Rate (DDR) protocol has been added to Quad I/O SPI Flash, and the clock frequency has been increased up to 80 MHz DDR and up to 166 MHz in Single Data Rate (SDR), it is not possible to use the traditional t_v(max) method as the strobe point within the data window to accurately capture the data. At

[1] See the Cypress Community on CK & CK# implementation: **https://community.cypress.com/t5/Knowledge-Base-Articles/Differential-Clock-Requirements-for-HyperBus-Products-KBA219878/ta-p/249263**

[2] When the DDR center-aligned read strobe (DCARS) feature is enabled, a second differential phase-shifted clock input PSC/PSC# is used as the reference for RWDS edges instead of CK/CK#. **For better supply and easier migration to new generation of x8 memory devices (SEMPER™ and HYPERRAM™ 2.0), support of DCARS is NOT recommended for new design (NRND).**

[3] For details on RWDS, see the HYPERBUS™ specification: **https://www.cypress.com/file/213356/download**.

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frequencies above 120 MHz SDR or 60 MHz DDR, the data eye and capture window become too narrow to enable possible and optimal capture point.

The following sections provide possible solutions.

- Add a Data Strobe

This approach adds a data strobe similar to the implementation done on HYPERBUS™ and Octal SPI protocols. This addition of a Data Strobe to QSPI has been ratified by JEDEC as *optional* and specified in the addendum No.1[1] to JESD251A[2] eXpanded Serial Peripheral Interface (xSPI) for non-volatile memory devices.

  - However, a few Flash memory suppliers already provide Quad I/O SPI flash with such Data Strobe. Furthermore, the additional Data Strobe signal prevents the Quad I/O SPI Flash from fitting into the popular small-size SOIC-8 package, because 9 signals are now needed to support such flash.
- Use Data Learning Pattern (DLP)
- This is an elegant solution because it does not require an additional pin on the host side, it enables a wider data-capture window, and supports higher-frequency Quad I/O SPI Flash.

The overall data-capture strategy for the host memory controller is to use the DLP input as a test sequence to characterize system response and determine t_V and t_{DV}. Once the data eye has been identified during the DLP portion of the read sequence, the controller selects the optimal data-capture point to maximize the timing margin for the read data.

A common way to create the master data-capture logic is via a series of skewed data-capture points that span the data-valid window. **Figure 1** shows the implementation for a single DQ, which might consist of five channels with a fixed sampling delay between each of the channels. The five delayed strobes (A through E) could be generated with a delay-locked loop (DLL) or using an oversampling clock that is in turn generated using an internally available higher-frequency clock. The host controller samples the target DQ while the DLP is being output. The phase-delayed strobes (A-E) are triggered by the clock edges when the DLP is output.

The following are some of the key points:

- Data oversampled: Samples from ‘taps’ B, C, and D always successfully capture the DLP. In this case, Tap C provides the greatest margin. Use Tap C to capture the data for the remainder of this read transaction
- Recalibration can be performed prior to every read transaction; it provides a more robust/reliable operation across operating conditions

[1] Addendum N°1 to JESD251, Optional x4 Quad I/O with Data Strobe: **https://www.jedec.org/system/files/docs/JESD251-A1.pdf**
Access to the document requires an active JEDEC membership.

[2] eXpanded Serial Peripheral Interface (xSPI) for non-volatile Memory Devices, Version 1.0:
https://www.jedec.org/system/files/docs/JESD251A.pdf
Access to the document requires an active JEDEC membership.

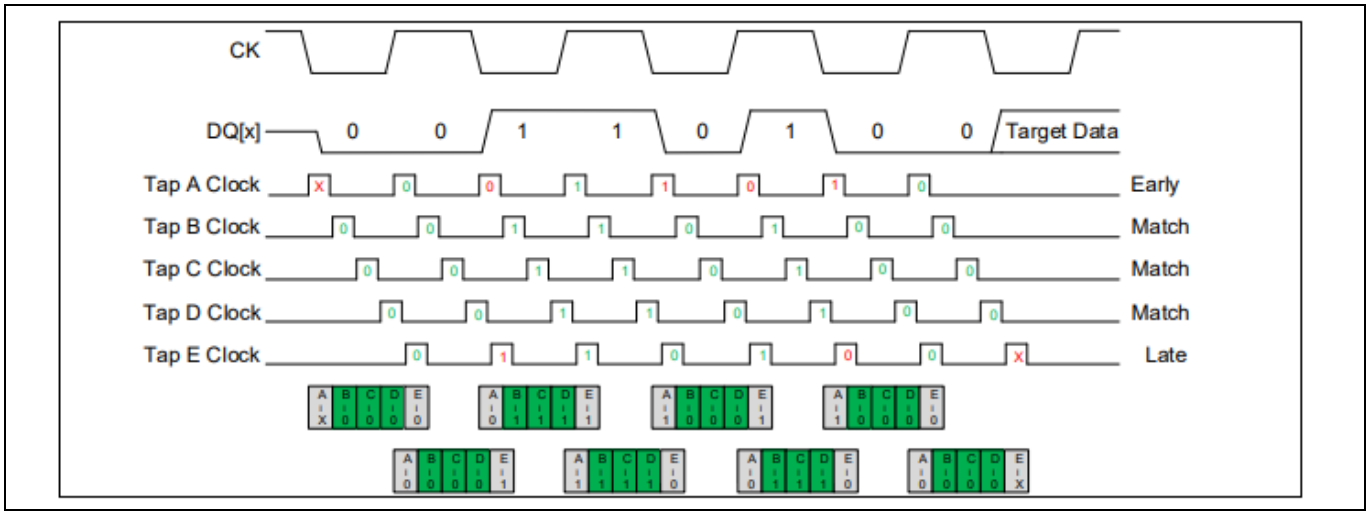

Figure 1 Host capture strategy DDR

For more details, see the application note: **DLP- Optimized Read Performance for Quad SPI Flash FL-S, FS-S and FL-L Families**.

4.3 Signal integrity for high-throughput memory devices

IBIS models are intended to be used for signal integrity analysis (signal timing/crosstalk simulations) on systems boards. See **Modelization and system-level simulation** and IBIS models for links to IBIS models for Infineon memory devices (section 3.3).

Based on the signal integrity/power delivery simulations done by using IBIS models of both the Infineon memory devices and memory controller, Infineon has developed PCB layout guides which provide initial reference towards PCB design with Infineon high-performance memory devices. These documents include both signal integrity and power delivery guidelines. In general, to achieve the highest performance, the PCB design should provide impedance-controlled routing for signals, support a low-impedance power delivery system, and control the EMI.

- **Design and layout guide for HYPERFLASH™ and HYPERRAM™ 1.0 Memory products**
- AN224153 - Design and Layout Guide for SEMPER™ Flash and HYPERRAM™ 2.0 Memory products
- Register to SEMPER™ Access Program to access this document: **https://go.cypress.com/semper-access-program-ap.**

In addition, you should always empirically verify actual signal characteristics on prototype and validation build units. If your design cannot meet these recommendations, detailed simulations should be performed to determine whether the exceptions will impact the performance of HYPERBUS™ memory devices.

5 Infineon software support and tools

5.1 SEMPER™ Solutions Hub

When developing a system that includes an Infineon NOR Flash products, the Infineon solutions hubs provide all the building blocks you need for design success. The SEMPER™ Solutions Hub includes software and hardware, and works with popular design environments.

5.1.1 Software

SEMPER™ Solutions Hub software is bundled and downloaded collectively as a SEMPER™ Software Development Kit (SDK) containing:

- production-grade NOR Flash drivers
- application code examples,
- hardware abstraction layers,
- design environment integration hooks.

There are three SEMPER™ SDK variants:

- SEMPER™ SDK Base includes basic NOR Flash APIs.
- SEMPER™ SDK Safe adds Functional Safety APIs
- SEMPER™ SDK Secure: goes further and includes security APIs

All three SEMPER™ SDKs can be downloaded from **Infineon Toolbox Online**.

5.1.2 Hardware

SEMPER™ Solutions Hub hardware provides turnkey development platforms to speed time to market. Some Infineon PSoC™ and AURIX™ kits are supported; they come pre-integrated with a SEMPER™ NOR Flash.

SEMPER™ SDK also works with standard third-party platforms, such as Raspberry Pi and NVIDIA Jetson Nano. SEMPER™ NOR flash memory can be integrated quickly with a MikroElektronika Click Board or an Infineon Pmod-compatible memory module. Also, Pmod resources for popular SEMPER™ memory configurations are available.

This SEMPER™ Solution Development Kit (SEMPER SDK) is built for various SEMPER™ NOR Flash families (SEMPER™, SEMPER™ Secure, SEMPER™ Nano) that are used in fail-safe automotive, industrial, and communications systems.

5.1.3 SDK key features

- Production-grade and MISRA-C compliant host drivers (for Parallel NOR Flash, QSPI Flash, HYPERFLASH™ and SEMPER™ Flash)
- Hardware abstraction layers to simplify integration
- Code examples, Flash memory models, and evaluation kits to reduce the learning curve
- C-model and wolfSSL security library for a quick start
- Starter kits and memory modules for easy evaluation
- Crypto algorithm validation module for compatibility

5.1.4 SDK architecture diagram

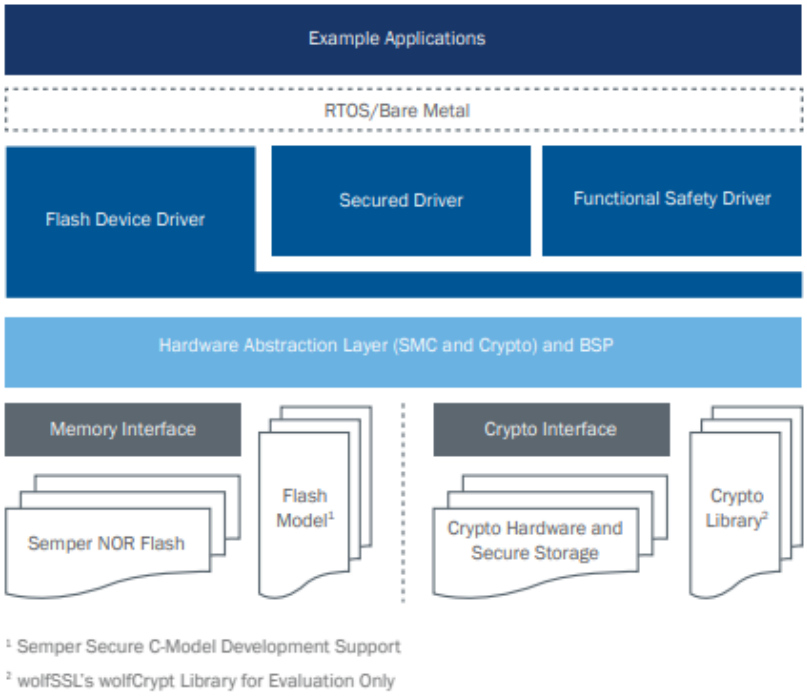

Figure 2 SDK architecture diagram

- For more details on the SDK, see **https://www.cypress.com/file/506601/download.**
- The SEMPER™ SDK is available from Infineon Toolbox at **https://softwaretools.infineon.com/tools#S**

5.2 Infineon NOR Flash patches for U-Boot and Linux MTD

SoC boot structure traditionally rely on either U-Boot or Linux MTD boot loader.

  - **U-Boot** (Universal Boot Loader) is an open-source, primary bootloader used in embedded devices to package the instructions to boot the device's Operating System kernel
  - Similarly, **Linux MTD** (Memory Technology Device) subsystem was created to provide an abstraction layer between the hardware-specific device drivers and higher-level applications.
- Infineon Memory Solutions software provides patches for both U-Boot and Linux MTD for specific Flash families (for example: SPI, HYPERFLASH™, SEMPER™ with x8 Octal xSPI…) and/or specific chipset targets (e.g., Xilinx Zynq 7000).

Table 11 U-Boot and MTD Linux patches

Flash type	Hyperlink	Note
Parallel NOR Flash	**https://www.cypress.com/products/parallel-nor-flash-memory#tabs-0-bottom_side-5**	Both U-Boot and Linux patches
SPI NOR Flash	**https://www.cypress.com/products/serial-nor-flash-memory#tabs-0-bottom_side-5**	Both U-Boot and Linux patches
HYPERBUS™ Flash	**https://www.cypress.com/products/hyperbus-memory#tabs-0-bottom_side-5**	Linux MTD

SEMPER™ Flash Quad SPI, x8 Octal xSPI	**https://community.cypress.com/t5/Semper-Flash-Access-Program/tkb-p/semper-flashtkb-board/label-name/semper%20flash%20software%20tools**	U-Boot - Register to SEMPER™ Access Program to access these files

Infineon Memory Solutions submit, on regular bases, new patches for its Flash into the respective U-Boot and MTD Linux communities. Many of these patches have been adopted by these communities and up-streamed in their respective source code. Visit U-Boot and MTD Linux communities to get the full list of updated Infineon Memory Solutions patches already up-streamed.

5.3 Flash programming tool

Flash programming tools are used to pre-program the Flash device prior to mounting it on the board. This is done as an alternative to the other flash programming method, called *in-situ* through which the Flash is programmed via the chipset on the board.

- See **https://www.cypress.com/products/device-programmer-system-partners#tabs-0-bottom_side-5** for the complete list of Infineon-supported Flash devices for programmer system partners.

6 Infineon resources for Memory qualification

6.1 Flash qualification database

Infineon Memory Solutions Flash datasheets provides AC and DC characteristics (current and timings) for a Flash device that are valid across the entire range of *P* (process), *V* (voltage range), and *T* (temperature range) conditions under which that given flash device is specified. However, your design might actually rely on tighter conditions such as follows:

- You need to support a voltage range of 2.7V to 3.0V only for your system, instead of the entire 2.7V to 3.6V range that the Flash can support.
- You operate the Flash device only at room temperature (25°C)
- You do not need more than 1,000 Program/Erase cycle during the lifetime of the project as your code is stable.
  - Infineon can provide you with **Fl**ash **Q**ualification **D**atabases which give you details on the Flash timing parameters under various Voltage, Temperature and Program/Erase cycle conditions. With such information, you can get a fine-tuned estimation of the Flash performance (timing, power consumption) in your system under these operating conditions.

These Flash Qualification Databases are available only for customers and chipset partners who have a valid NDA with Infineon Memory Solutions. Contact your local Infineon sales representative or FAE to request a Flash Qualification Database or to enter an NDA with Infineon to get it.

6.2 Certification program – Joint qualification

- To do in-depth verification of the compliance of the selected Flash and chipset in your system, under the specific conditions you plan to operate at production level, you can enter a **Joint Qualification** with Infineon Memory Solutions. Such Joint-Qualification fully covers and verify the signal integrity, timing compliance, Flash schematics and PCB layout, S/W design, and Flash behavior in system under real-life conditions. In addition, Infineon can review your Flash usage model and point out areas of concern or incorrect usage. Passing this **Joint-Qualification** will ensure that your system works as expected in production. Contact your local Infineon sales person or FAE to get more details on Infineon Memory Solutions Joint Qualification program.

7 Infineon tools to select best memory device with chipset

7.1 Infineon Memory solutions Chipset pairing charts

Infineon Memory Solutions works with many chipset partners to qualify our memory devices with their SoCs and MCU. Chipset partners get early access to Infineon Memory Solutions products and their preliminary specifications, as well as to dedicated support to qualify Infineon memory devices on their boards.

These efforts result in **Pairing Charts** that provide a mapping of Infineon memory devices with a given Chipset Partner product portfolio, and includes the following features:

- For each listed chipset, indicates the supported memory interfaces
- Highlights both Qualified memory and Recommended memory devices (i.e., memory devices that are known to be working with that specific chipset but has not been (yet) fully qualified by the chipset partner).

Infineon memory qualification with a chipset has been done by the chipset partner either on the Reference Design, the Evaluation Board, the Bring-Up Board, the Demonstration Board, the Validation Board or the Turnkey Reference Design.

See **https://www.cypress.com/chipset-partners** for access to the pairing of Infineon memory devices with more than 20 chipset partners.

7.2 Contacting Infineon Memory Solutions

Contact your local Infineon sales person or FAE or through **https://go.cypress.com/Get-in-Touch** if your targeted chipset partner is not listed, or if you cannot find a given chipset part number in the pairing charts, or if you have additional questions.

8 Summary

This application note discusses multiple items to consider for enabling support of Infineon memory devices on a given chipset. It provides relevant recommendations and best practices to pass each stage of the support cycle.

For more detailed information on any specific development milestones, see the links to additional information provided in that application note or contact your local Infineon sales or FAE person.

Revision history

Document version	Date of release	Description of changes
**	2021-09-29	New application note
*A	2022-03-31	Removed the section 5.2 Flash file system (FFS)

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Edition 2022-03-31
Published by
Infineon Technologies AG
81726 Munich, Germany

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Document reference
002-33989 Rev. *A

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