Migrating from ISSI IS25LQ032B to Infineon S25FL064L

About this document

Scope and purpose

This application note provides guidelines to migrate from ISSI's IS25LQ032B to Infineon's S25FL064L 65nM Floating Gate Serial NOR Flash family of products, and highlights the similarities and differences in both specifications to facilitate this migration path.

Intended audience

This application note is intended to assist System Designers, Field Applications Engineers, Applications Engineers, and end users migrate from ISSI IS25LQ032B to Infineon's S25FL064L.

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1 Introduction

Infineon S25FL064L device is a 3.0-V Flash nonvolatile (NV) memory product fabricated with the 65-nm Floating Gate process technology. This application note describes the similarities and key differences to consider when migrating from the ISSI IS25LQ032B (32 Mb) to the Infineon S25FL064L (64 Mb) device. The Power-On-RESET, Hardware RESET, and (VCC) Power-up and Power-down timing diagrams are included. There are registers that do not exist on the IS25LQ032B, but exist on the S25FL064L, which may need to be set, depending on the requirement.

2 Feature Comparison

Table 1 Comparison of IS25LQ32B with S25FL064L

Parameter/Feature	IS25LQ032B	S25FL064L	Notes
Density	32 Mb	64 Mb	***S25FL064L:*** Double the density, no SPI densities below 64 Mb
VCC	2.3 V to 3.6 V	2.7 V to 3.6 V	
Page Program buffer size	256 B	256 B	
QUAD I/O SDR Freq.	104 MHz	108 MHz	
SPI CLK Mode 0, 3	Yes	Yes	
Uniform 4KB sector	Yes	Yes	
Program / Erase Cycles	>100,000	>100,000	
Data Retention	20 years	20 years	
Erase Resolution	4 KB, 32 KB, 64 KB	4 KB, 32 KB, 64 KB	
Program - Erase / Suspend - Resume	Yes	Yes	
Security Regions	4 x 256 B	4 x 256 B	
AEC-Q100 Temp. Grade	Yes	Yes	IS25LQ032B: Grade-1(+125C) only. ***S25FL064L:*** Grade-3(+85C), 2(+105C), 1(+125C)
8-pin SOIC 208mil pkg 8-contact WSON 5mm x 6mm pkg.	Yes	Yes	IS25LQ032B: HOLD# on pin-7 ***S25FL064L:*** RESET# on pin-7[1]
Address Byte Length	3 B	3 B or 4 B	
Device ID	Manuf. ID: 9Dh/Device ID: 4016h	Manuf. ID: 01h/Device ID: 6017h	Read Product Identification (RDID) command 9Fh
SFDP	Yes	Yes	
Program Current Consumption	17 mA (typ) 25 mA (max)	17 mA (typ) 25 mA(max)	
Erase Current Consumption	17 mA (typ) 25 mA (max)	17 mA (typ) 25 mA (max)	
Standby Current	8 mA (typ) 60 mA (max)	20 mA (typ) 55 mA (max)	
Deep Power Down	5 uA (typ) 10 uA (max)	2 uA (typ) 20 uA (max)	

[1] Hardware (Warm) Reset

Feature Comparison

A configuration option is provided to allow IO3/RESET# to be used as a hardware reset input when the device is not in any Quad or QPI mode or when it is in any Quad mode or QPI mode and CS# is HIGH. In Quad or QPI mode, on some packages, a separate reset input is provided (RESET #). When IO3/RESET# or RESET# is driven LOW for t_{RP} time, the device starts the hardware reset process. The process continues for t_{RPH} time. At the end of both t_{RPH} and the reset hold time following the rise of RESET# (t_{RH}), the device transitions to the Interface STANDBY state and can accept commands.

3 S25FL064L - RESET#

The RESET# input provides a hardware method of resetting the device to STANDBY state, ready for receiving a command. When RESET# is driven to logic LOW (VIL) for at least a period of t_{RP}, the device starts the hardware reset process. RESET# causes the same initialization process to be performed when power comes up and requires t_{PU} time. RESET# may be asserted LOW at any time. To ensure data integrity, any operation that was interrupted by a hardware reset should be reinitiated once the device is ready to accept a command sequence. RESET# has an internal pull-up resistor and may be left unconnected in the host system if not used. The internal pull-up will hold Reset HIGH after the host system has actively driven the signal HIGH and then stops driving the signal. The RESET# input is not available on all package options. When not available, the RESET# input of the device is tied to the inactive state. If a Hardware Reset is initiated during an Erase, Program, or writing of a Register operation, the data in that Sector, Page, or Register is not stable, the operation that was interrupted needs to be initiated again. If a Hardware Reset is initiated during a Software Reset operation, the Hardware Reset might be ignored.

3.1 S25FL064L - Power-On (Cold) Reset

The device executes a Power-On Reset (POR) process until a time delay of t_{PU} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold. See **Figure 1**. The device must not be selected (CS# to go HIGH with $V_{CC)}$ during power-up (t_{PU}), that is, no commands may be sent to the device until the end of t_{PU}. RESET# and IO3/RESET# reset function are ignored during POR. If RESET# or IO3/RESET# is LOW during POR and remains LOW through and beyond the end of t_{PU}, CS# must remain HIGH until t_{RH} after RESET# and IO3/RESET# return HIGH. RESET# and IO3/RESET# must return HIGH for greater than t_{RS} before returning LOW to initiate a hardware reset. The IO3/RESET# input functions as the RESET# signal when CS# is HIGH for more than t_{CS} time or when Quad or QPI Mode is not enabled CR1V[1] = 0 or
CR2V[3] = 0.

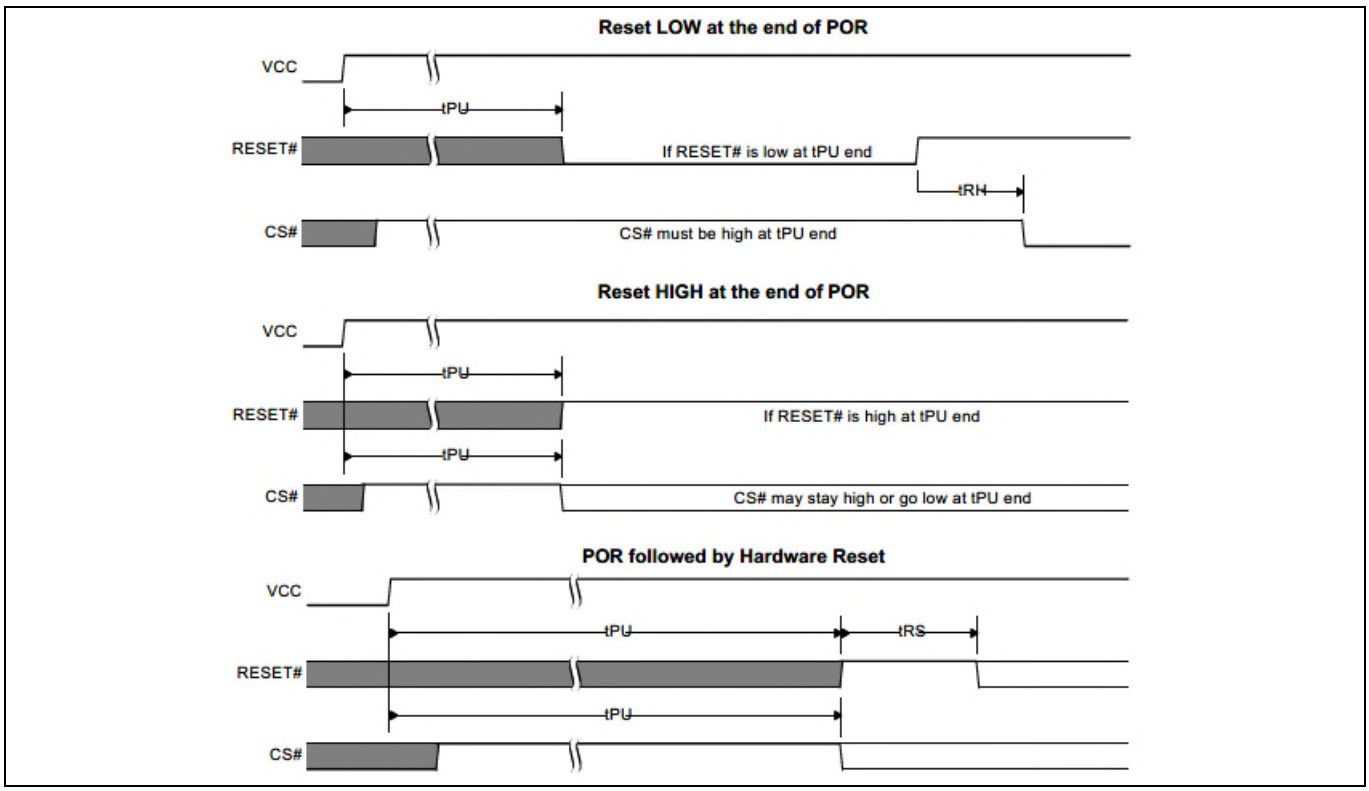

Figure 1 Power-On (cold) RESET Timing - POR

S25FL064L - RESET#

3.2 S25FL064L - Hardware (warm) RESET Timing

Table 2 Hardware Reset Parameters[2,3,4]

Parameter	Description	Limit	Time	Unit
t_{RS}	Reset Setup – Prior Reset end and RESET# HIGH before RESET# LOW	Min	50	ns
t_{RPH}	Reset Pulse Hold – RESET# LOW to CS# LOW		100	us
t_{RP}	RESET# Pulse Width		200	ns
t_{RH}	Reset Hold – RESET# HIGH before CS# LOW		150	

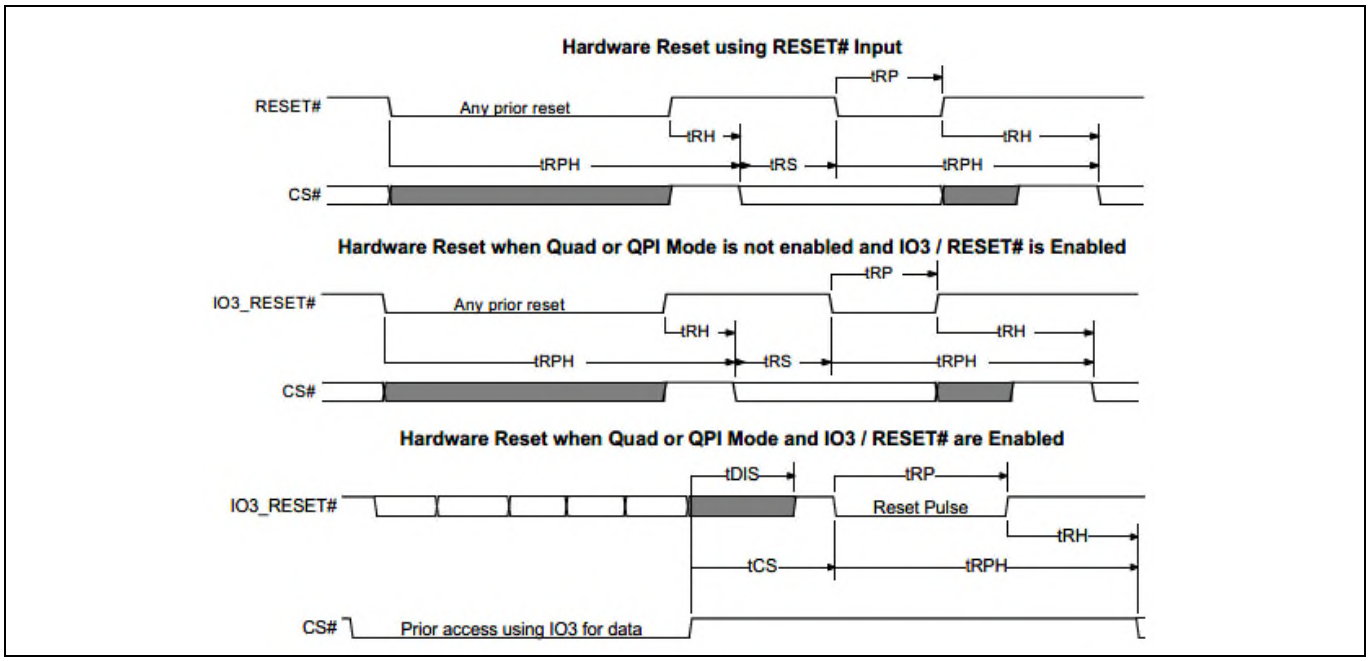

Figure 2 Hardware (warm) RESET Timing

[2] RESET# and IO3/RESET# LOW are ignored during Power-up (t_{PU}). If Reset# is asserted during the end of t_{PU}, the device will remain in the reset state and tRH will determine when CS# may go LOW.

[3] If Quad or QPI mode is enabled, IO3/RESER# LOW is ignored during t_{CS}.

[4] Sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.

4 S25FL064L - Power-up/Power-down

Table 3 Power-up/Power-down Voltage and Timing

Symbol	Parameter	Min	Max	Unit
V_{cc} (min)	V_{cc} (minimum operation voltage)	2.7		V
V_{cc} (cut-off)	V_{cc} (Cut-off where re-initialization is need)	2.4[5,6]		
V_{cc} (low)	V_{cc} (low voltage for initialization to occur)	1.0[5,6]		
t_{PU}	V_{CC} (min) to Read operation		300	us
t_{PD}	V_{CC} (low) time	10.0		

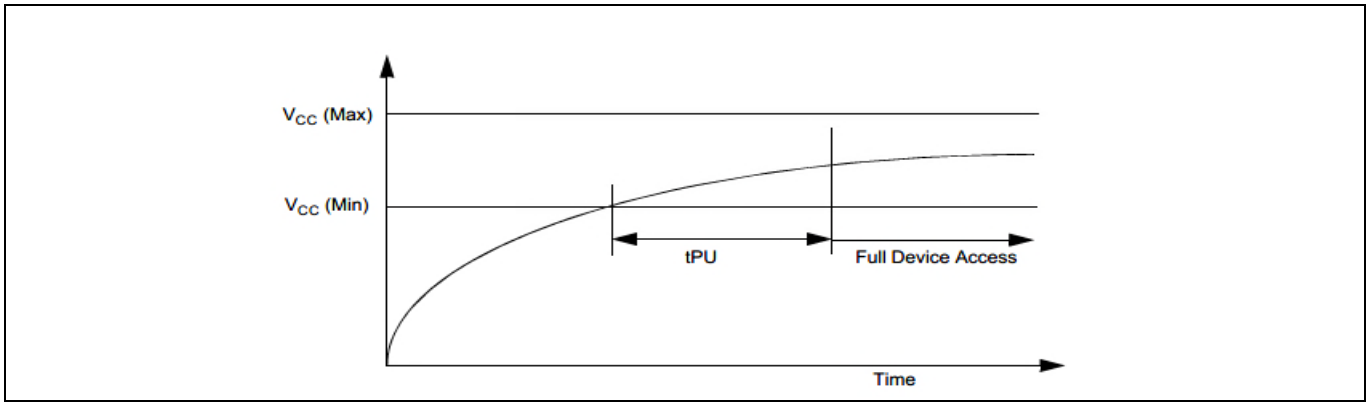

Figure 3 Power-up [5,6]

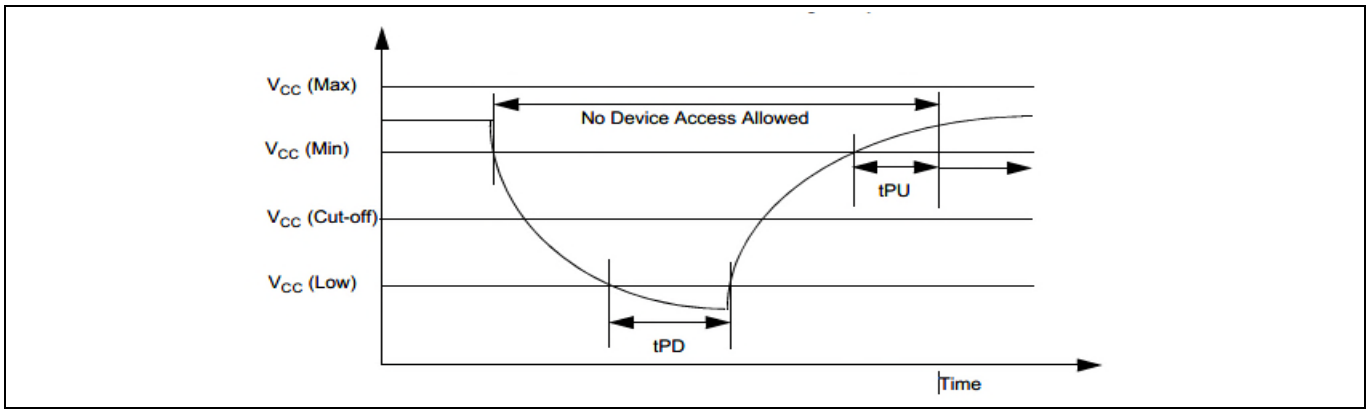

Figure 4 Power-down/Voltage Drop

[5] Re-initialization is needed if V_{CC} drops below 2.4 V.

[6] V_{CC} needs to go below 1.0 V for initialization to occur.

5 IS25LQ032B versus S25FL064L - Compatible Core Instruction/Command and Hex Code Values

Table 4 Comparison of Core Instructions/Command Values and Hex Codes

Command IS25LQ032B	Command S25FL064L	Hex Code IS25LQ032B	Hex Code S25FL064L	Operation IS25LQ032B	Operation S25FL064L
PP	PP	02h	02h	Serial Input Page Program	Serial Input Page Program
PPQ	QPP	32h, 38h	32h	QUAD input page program	QUAD input page program
SER	SE	D7h, 20h	20h	Sector Erase (4 KB)	Sector Erase (4 KB)
BER32	HBE	52h	52h	Block Erase (32 KB)	Half Block Erase (32 KB)
BER64	BE	D8h	D8h	Block Erase (64KB)	Block Erase (64KB)
CER	CE	C7h, 60h	C7h, 60h	Chip Erase	Chip Erase
WRSR	WRAR, WRR	01h	71h, 01h	Write Status Register	Write Any Register; Write Register
WRFR	WRAR, WRR	42h	71h, 01h	Write Function Register	Write Any Register; Write Register
IRP	IRPP	62h	2Fh	Program Information Row	Individual and Region Protection Register Program

5.1 IS25LQ032B Status Register versus S25FL064L Status Register-1 Nonvolatile (SR1NV)

Most bits are compatible. S25FL064L *Bit-6* (QUAD) is set in the Configuration Register-1 Nonvolatile CR1NV[1] Bit-1.

S25FL064L-related Commands:

- Nonvolatile Write Enable (WREN 06h)
- Write Disable (WRDI 04h)
- Write Registers (WRR 01h)
- Read Any Register (RDAR 65h)
- Write Any Register (WRAR 71h)

IS25LQ032B versus S25FL064L - Compatible Core Instruction/Command and Hex Code Values

Table 5 Compatible Core Instructions/Command Values and Hex Codes

Bit	Name		Default State		Type		Notes	
	IS25LQ032B	S25FL064L	IS25LQ032B	S25FL064L	IS25LQ032B	S25FL064L	IS25LQ032B	S25FL064L
Bit 0	WIP	WIP	0	0	V	NV	Write In Progress Bit: • "0" = device is ready (default) • "1" = write cycle in progress and the device is busy	Not user programmable. Write In Progress Bit: • "0" = device is ready (default) • "1" = write cycle in progress and the device is busy
Bit 1	WEL	WEL	0	0	V	NV	Write Enable Latch: • "0" = Device is not write-enabled (default) • "1" = Device is write-enabled	Not user programmable. Write Enable Latch: • "0" = device is not write-enabled (default) • "1" = device is write-enabled
Bit 2	BP0	BP0	000b	000b	NV	NV	Block Protection Bit (BP0): • "0" = Specific blocks are not write-protected (default) • "1" = Specific blocks are write-protected	Block Protection Bit (BP0): • "0" = Specific blocks are not write-protected (default) • "1" = Specific blocks are write-protected
Bit 3	BP1	BP1	000b	000b	NV	NV	Block Protection Bit (BP1): • "0" = Specific blocks are not write-protected (default)	Block Protection Bit (BP1): • "0" = Specific blocks are not write-protected (default) • "1" = Specific blocks are

IS25LQ032B versus S25FL064L - Compatible Core Instruction/Command and Hex Code Values

Bit	Name		Default State		Type		Notes	
	IS25LQ032B	S25FL064L	IS25LQ032B	S25FL064L	IS25LQ032B	S25FL064L	IS25LQ032B	S25FL064L
							• "1" = Specific blocks are write-protected	write-protected
Bit 4	BP2	BP2	000b	000b	NV	NV	Block Protection Bit (BP2): • "0" = Specific blocks are not write-protected (default) • "1" = Specific blocks are write-protected	Block Protection Bit (BP2): • "0" = Specific blocks are not write-protected (default) • "1" = Specific blocks are write-protected
Bit 5	BP3	TBPROT	0	0	NV	NV	Block Protect Bit: • "0" = Specific blocks are not write-protected (default) • "1" = Specific blocks are write-protected	TBPROT: Provides the default state for Top or Bottom Protect (TBPROT)
Bit 6	QE	SEC	0	0	NV	NV	Quad Enable bit: • “0” = Quad output function disable (default) • “1” = Quad output function enable	SEC: Provides the default state for Sector - Block Protect.
Bit 7	SRWD	SRP0	0	0	NV	NV	SRWD: Status Register Write Disable	Status Register Protect: • “0” = Status Register is not

IS25LQ032B versus S25FL064L - Compatible Core Instruction/Command and Hex Code Values

Bit	Name		Default State		Type		Notes	
	IS25LQ032B	S25FL064L	IS25LQ032B	S25FL064L	IS25LQ032B	S25FL064L	IS25LQ032B	S25FL064L
								Protected (default) • "1" = Status Register is Protected

5.2 IS25LQ032B = Function Register

S25FL064L does not have a Function Register.

Table 6 IS25LQ032B Function Register Default Settings

Bit	Name		Default IS25LQ032B	Type IS25LQ032B	Definition	
	IS25LQ032B	S25FL064L			IS25LQ032B	S25FL064L
Bit 0	Reserved	N/A	0	NV Read only	Reserved for Future Use	
Bit 1	Reserved	N/A	0	NV Read only	Reserved for Future Use	
Bit 2	PSUS	N/A	0	Volatile Read only	Program suspend bit: • "0" = Program is not suspended • "1" = Program is suspended	See SR2V for PS
Bit 3	ESUS	N/A	0	Volatile Read only	Erase suspend bit: • "0" = Erase is not suspended • "1" = Erase is suspended	See SR2V for ES
Bit 4	IR Lock 0	N/A	0	Volatile Read only	Lock Information Row 0: • "0" = Information Row can be programmed • "1" = Information Row cannot be programmed	Security Region Lock Bit LB0. See CR1NV.

IS25LQ032B versus S25FL064L - Compatible Core Instruction/Command and Hex Code Values

Bit	Name		Default IS25LQ032B	Type IS25LQ032B	Definition	
	IS25LQ032B	S25FL064L			IS25LQ032B	S25FL064L
Bit 5	IR Lock 1	N/A	0	READ/WRITE one-time programmable (OTP)	Lock Information Row 1: • "0" = Information Row can be programmed • "1" = Information Row cannot be programmed	Security Region Lock Bit LB1. See CR1NV.
Bit 6	IR Lock 2	N/A	0	READ/WRITE one-time programmable (OTP)	Lock Information Row 2: • "0" = Information Row can be programmed • "1" = Information Row cannot be programmed	Security Region Lock Bit LB2. See CR1NV.
Bit 7	IR Lock 3	N/A	0	READ/WRITE one-time programmable (OTP)	Lock Information Row 3: • "0" = Information Row can be programmed • "1" = Information Row cannot be programmed	Security Region Lock Bit LB3. See CR1NV.

5.3 S25FL064L = Status Register-1 Volatile (SR1V)

IS25LQ032B does not have volatile status register.

S25FL064L-related Commands:

- Read Status Register-1 (RDSR1 05h)
- Write Enable for Volatile (WRENV 50h)
- Write Registers (WRR 01h)
- Clear Status Register (CLSR 30h)
- Read Any Register (RDAR 65h)
- Write Any Register (WRAR 71h)

The Status Register-1, Volatile (SR1V) default state is set by Status Register-1, Non-Volatile (SR1NV).

Table 7 S25FL064L Status Register-1 Volatile (SR1V) Default Settings

Bit	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition S25FL064L
Bit 0	N/A	WIP	SRNV1	Volatile READ only	Write In Progress Bit (Not user programmable): • "0" indicates the device is ready (default) • "1" indicates a write cycle is in progress and the device is busy
Bit 1	N/A	WEL	SRNV1	Volatile READ only	Write Enable Latch (Not user programmable): • "0" indicates the device is not write enabled (default) • "1" indicates the device is write enabled
Bit 2	N/A	BP0	SRNV1	Volatile	Block Protection Bit: • "0" = Specific blocks are not write-protected (default) • "1" = Specific blocks are write-protected
Bit 3	N/A	BP1			
Bit 4	N/A	BP2			
Bit 5	N/A	TBPROT	SRNV1	Volatile	Provides the default state for Top or Bottom Protect (TBPROT)
Bit 6	N/A	SEC	SRNV1	Volatile	Provides the default state for Sector/Block Protect.
Bit 7	N/A	SRP0	SRNV1	Volatile	Status Register Protect (SRP0) • “0” = Status Register is not Protected (default) • “1” = Status Register is Protected

5.4 S25FL064L = Status Register-2 Volatile (SR2V)

IS25LQ032B does not have volatile status register-2.

S25FL064L-related Commands:

- Read Status Register 2 (RDSR2 07h)
- Read Any Register (RDAR 65h)

Status Register 2 does not have user-programmable nonvolatile bits; all defined bits have volatile read-only status. The default state of these bits is set by hardware.

Table 8 Status Register 2 Volatile (SR2V)

Bit	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition S25FL064L
Bit 0	N/A[7]	PS	0	Volatile READ Only	Program Suspend (PS) • "1" = In Program Suspend mode • "0" = Not in Program Suspend mode
Bit 1	N/A[7]	ES	0	Volatile READ Only	Erase Suspend (ES) • "1" = In Erase Suspend mode • "0" = Not in Erase Suspend mode
Bit 2	N/A	RFU	000		Reserved for Future Use
Bit 3	N/A	RFU			
Bit 4	N/A	RFU			
Bit 5	N/A	P_ERR	0	Volatile READ Only	Program Error (P_ERR) • "1" = Program Error Occur • "0" = No Error
Bit 6	N/A	E_ERR	0	Volatile READ Only	Erase Error (E_ERR) • "1" = Erase Error Occurred • "0" = No Error
Bit 7	N/A	RFU	0		Reserved for Future Use

[7] See Functional Register for PSUS.

6 S25FL064L = Configuration Register-1 Nonvolatile (CR1NV)

IS25LQ032B does not have Configuration Register-1 Nonvolatile; IS25LQ032B Bit-1 is set in Status Register Bit-6 (QE), *S25FL064L* Configuration Register 1 controls certain interface and data protection functions. The register bits can be changed using the WRR command with 16 input cycles or with the WRAR command.

Related Commands:

- Nonvolatile Write Enable (WREN 06h)
- Write Registers (WRR 01h)
- Read Any Register (RDAR 65h)
- Write Any Register (WRAR 71h)

Table 9 Configuration Register 1 Nonvolatile (CR1NV) Default Settings

Bit	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition
Bit 0	N/A	SRP1_D	0	OTP	***S25FL064L:*** Status Register Protect-1 Default (SRP1_D) When IRP[2:0]= "111" SRP1_D bit is programmable. Lock current state of SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV, and DLRV: • "1" = Registers permanently locked • "0" = Registers not protected by SRP1 after POR
Bit 1	N/A	QUAD_NV	0	Nonvolatile	IS25LQ032B: For QUAD Enable (QE) bit, see Status Register Bit-6 ***S25FL064L:*** QUAD_Nonvolatile (QUAD_NV) - Provides the default state for QUAD
Bit 2	N/A[8]	LB0	0	OTP	IS25LQ032B: For IR Lock x, see Function Register Bit-4, Bit-5, Bit-6, Bit-7 ***S25FL064L:*** Security Region Lock Bits (LB0, LB1, LB2, LB3)
Bit 3	N/A[9]	LB1	0		OTP lock Bits 3:0 for Security Regions 3:0: • "0" = Security Region not locked • "1" = Security Region permanently locked
Bit 4	N/A[10]	LB2	0		
Bit 5	N/A[11]	LB3	0		

[8] See Functional Register IR Lock 0.

[9] See Functional Register IR Lock 1.

[10] See Functional Register IR Lock 2.

[11] See Functional Register IR Lock 3.

S25FL064L = Configuration Register-1 Nonvolatile (CR1NV)

Bit	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition
Bit 6	N/A	CMP_NV	0	Nonvolatile	***S25FL064L:*** Provides the default state for **Complement Protection Default (CMP**)
Bit 7	N/A	SUS_D	0	Nonvolatile READ only	***S25FL064L:*** Provides default state for **Suspend Status (SUS_D).** Not user programmable.

6.1 S25FL064L = Configuration Register-1 Volatile (CR1V)

IS25LQ032B does not have Configuration Register-1 Volatile.

S25FL064L-related Commands:

- Read Configuration Register-1 (RDCR1 35h)
- Write Enable for Volatile (WRENV 50h)
- Write Registers (WRR 01h)
- Read Any Register (RDAR 65h)
- Write Any Register (WRAR 71h).

Table 10 Configuration Register 1 Volatile (CR1V) Default Settings

Bit	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition
Bit 0	N/A	SRP1	CR1NV	Volatile	***S25FL064L:*** Status Register Protect-1 (SRP1) Lock current state of SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV, and DLRV: • "1" = Registers locked • "0" = Registers unlocked
Bit 1	N/A	QUAD	CR1NV	Volatile	***S25FL064L:*** QUAD • "1" = Quad • "0" = Dual or Serial
Bit 2	N/A	LB0	CR1NV	Volatile READ only	***S25FL064L:*** Volatile copy of Security Region Lock bits (LB0, LB1, LB2, LB3) Not User writable. See CR1NV[5:2]. OTP lock Bits 3:0 for Security Regions 3:0: • "0" = Security Region not locked • "1" = Security Region permanently locked
Bit 3	N/A	LB1	CR1NV		
Bit 4	N/A	LB2	CR1NV		
Bit 5	N/A	LB3	CR1NV		

S25FL064L = Configuration Register-1 Nonvolatile (CR1NV)

Bit	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition
Bit 6	N/A	CMP	CR1NV	Volatile	***S25FL064L:*** Complement Protection (CMP): • "0" = Normal Protection Map • "1" = Inverted Protection Map
Bit 7	Functional Register	SUS	CR1NV	Volatile READ only	IS25LQ032B: for Program/Erase Suspend status, see Function Register. ***S25FL064L:*** Suspend Status (SUS): • "1" = Erase/Program suspended • "0" = Erase/Program not suspended

6.2 S25FL064L = Configuration Register-2 Nonvolatile (CR2NV)

IS25LQ032B does not have Configuration Register-2 Nonvolatile (CR2NV). The S25FL064L Configuration Register-2 controls certain interface functions. The register bits can be read and changed using the Read Any Register and Write Any Register commands. The nonvolatile version of the register provides the ability to set the POR, hardware reset, or software reset state of the controls. The volatile version of the register controls the feature behavior during normal operation.

Table 11 Configuration Register 2 Nonvolatile (CR2NV) Default Settings

Bit	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition
Bit 0	N/A	RFU	0		Reserved for Future Use
Bit 1	N/A	ADP_NV	0	Nonvolatile	***S25FL064L:*** Address Length at Power-up (ADP_NV) Provides the default state for Address Length at power-up: • "1" = 4-byte address • "0" = 3-byte address
Bit 2	N/A	WPS_NV	0	Nonvolatile	***S25FL064L:*** Write Protect Selection (WPS_NV) Provides the default state for Write Protect Selection (WPS): • "0" = Legacy Protection • "1" = Individual Block Lock
Bit 3	N/A	QPI_NV	0	Nonvolatile	***S25FL064L:*** QUAD Peripheral Interface Nonvolatile (QPI) Provides the default state for QPI mode: • "1" = Enabled -- QPI (4-4-4) protocol in use

S25FL064L = Configuration Register-1 Nonvolatile (CR1NV)

Bit	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition
					• "0" = Disabled -- Legacy SPI protocols in use, instruction is always serial on SI
Bit 4	N/A	RFU	0		Reserved for Future Use
Bit 5	N/A	OI_NV	1	Nonvolatile	***S25FL064L:*** Output Impedance - Provides the default Output Impedance (OI) state.
Bit 6	N/A	OI_NV	1	Nonvolatile	***S25FL064L:*** Output Impedance - Provides the default Output Impedance (OI) state.
Bit 7	N/A	IO3R_NV	0	Nonvolatile	***S25FL064L:*** I/O3/RESET_Nonvolatile (IO3R_NV): • "1" = Enabled -- IO3_RESET is used as IO3 / RESET# input when CS# is HIGH or Quad Mode is disabled CR1V[1] = 0 or QPI is disabled (CR3V[3] = 0) • "0" = Disabled -- IO3 has no alternate function, hardware reset is disabled. Provides the default state for the IO3/RESET# function enable.

6.3 S25FL064L = Configuration Register-2 Volatile (CR2V)

IS25LQ032B does not have Configuration Register-2 Volatile (CR2V).

S25FL064L-related Commands:

- Read Configuration Register-2 (RDCR2 15h)
- Read Any Register (RDAR 65h)
- Write Enable for Volatile (WRENV 50h)
- Write Register (WRR 01h)
- Write Any Register (WRAR 71h)
- Enter 4-Byte address mode (4BEN B7h)
- Exit 4-Byte address mode (4BEX E9h)
- Enter QPI (38h)
- Exit QPI (F5h)

Table 12 Configuration Register 2 Volatile (CR2V) Default Settings

Bit	Name				
	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition
Bit 0	N/A	ADS	CR2NV[1]	Volatile	***S25FL064L:*** Address Length Status (ADS). See CR2NV[1]. • "1" = 4-byte address

S25FL064L = Configuration Register-1 Nonvolatile (CR1NV)

Bit	Name				
	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition
					• “0” = 3-byte address
Bit 1	N/A	ADP	CR2NV	Volatile READ only	***S25FL064L:*** Address Length at Power-up (ADP) • “1” = 4-byte address • “0” = 3-byte address
Bit 2	N/A	WPS	CR2NV	Volatile	***S25FL064L:*** Write Protect Selection (WPS) • “0” = Legacy Protection • “1” = Individual Block Lock
Bit 3	N/A	QPI	CR2NV	Volatile	***S25FL064L:*** QUAD Peripheral Interface Nonvolatile (QPI). State for QPI mode: • ”1” = Enabled -- QPI (4-4-4) protocol in use • “0” = Disabled -- Legacy SPI protocols in use, instruction is always serial on SI
Bit 4	N/A	RFU	CR2NV		Reserved for Future Use
Bit 5	N/A	OI	CR2NV	Volatile	***S25FL064L:*** Output Impedance - Provides the default Output Impedance (OI) state.
Bit 6	N/A	OI	CR2NV	Volatile	***S25FL064L:*** Output Impedance - Provides the default Output Impedance (OI) state.
Bit 7	N/A	IO3_Reset	CR2NV	Volatile	***S25FL064L:*** IO3/RESET_Nonvolatile (IO3R_NV): • “1” = Enabled -- IO3_RESET is used as IO3 / RESET# input when CS# is HIGH or Quad Mode is disabled CR1V[1] = 0 or QPI is disabled (CR3V[3] = 0). • “0” = Disabled -- IO3 has no alternate function, hardware reset is disabled. Provides the default state for the IO3 / RESET# function enable.

S25FL064L = Configuration Register-1 Nonvolatile (CR1NV)

6.4 Configuration Register 3 Nonvolatile (CR3NV)

IS25LQ032B does not have Configuration Register-3 Nonvolatile (CR3NV). The S25FL064L Configuration Register-3 controls the main Flash array read commands burst wrap behavior and read latency. The burst wrap configuration does not affect commands reading from areas other than the main Flash array, for example, read commands for registers or Security Regions. The nonvolatile version of the register provides the ability to set the start-up (boot) state of the controls as the contents are copied to the volatile version of the register during the POR, hardware reset, or software reset. The volatile version of the register controls the feature behavior during normal operation. The register bits can be read and changed using Read Configuration 3 (RDCR3 33h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h). The volatile version of the register can also be written by the Set Burst Length (77h) command.

S25FL064L-related Commands:

- Nonvolatile Write Enable (WREN 06h)
- Write Registers (WRR 01h)
- Read Any Register (RDAR 65h)
- Write Any Register (WRAR 71h)

Table 13 Configuration Register 3 Nonvolatile (CR3NV) Default Settings

Bit	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition
Bit 0	N/A	RL_NV	0	Nonvolatile	***S25FL064L:*** READ Latency_Nonvolatile (RL_NV) 0 to 15 latency (dummy) cycles following read address or continuous mode bits.
Bit 1	N/A	RL_NV	0		
Bit 2	N/A	RL_NV	0		
Bit 3	N/A	RL_NV	1		
Bit 4	N/A	WE_NV	1	Nonvolatile	***S25FL064L:*** Wrap Enable (WE_NV) Default • "0" = Wrap Enabled • "1" = Wrap Disabled
Bit 5	N/A	WL_NV	1	Nonvolatile	***S25FL064L:*** Wrap Length (WL_NV) Default • "00" = 8-byte wrap • "01" = 16-byte wrap • "10" = 32-byte wrap • "11" = 64-byte wrap
Bit 6	N/A	WL_NV	1		
Bit 7	N/A	RFU	0	Nonvolatile	Reserved for Future

S25FL064L = Configuration Register-1 Nonvolatile (CR1NV)

6.5 Configuration Register 3 Volatile (CR3V)

IS25LQ032B does not have Configuration Register-2 Volatile (CR2V).

S25FL064L-related Commands:

- Read Configuration-3 (RDCR3 33h)
- Write Enable for Volatile (WRENV 50h)
- Write Registers (WRR 01h)
- Read Any Register (RDAR 65h)
- Write Any Register (WRAR 71h)
- Set Burst Length (SBL 77h). This is the register displayed by the RDCR3 command.

Table 14 Configuration Register 3 Volatile (CR3V) Default Settings

Bit	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition
Bit 0	N/A	RL	CR3NV	Volatile	***S25FL064L:*** READ Latency (RL) 0 to 15 latency (dummy) cycles following read address or continuous mode bits.
Bit 1	N/A	RL	CR3NV		
Bit 2	N/A	RL	CR3NV		
Bit 3	N/A	RL	CR3NV		
Bit 4	N/A	WE	CR3NV	Volatile	***S25FL064L:*** Wrap Enable (WE) Default • "0" = Wrap Enabled • "1" = Wrap Disabled
Bit 5	N/A	WL	CR3NV	Volatile	***S25FL064L:*** Wrap Length (WL) Default • "00" = 8-byte wrap • "01" = 16-byte wrap • "10" = 32-byte wrap • "11" = 64-byte wrap
Bit 6	N/A	WL	CR3NV		
Bit 7	N/A	RFU	CR3NV	Volatile	Reserved for Future Use

7 S25FL064L = Individual and Region Protection Register (IRP)

The default state of the IRP bits is programmed by Infineon.

S25FL064L-related Commands:

- IRP Read (IRPRD 2Bh) and IRP Program (IRPP 2Fh)
- Read Any Register (RDAR 65h)
- Write Any Register (WRAR 71h)

The IRP register is a 16-bit OTP memory location used to permanently configure the behavior of Individual and Region Protection (IRP) features. IRP does not have user programmable volatile bits; all defined bits are OTP.

Table 15 IRP Register (IRP) Default Settings

Bit	IS25LQ032B Name	S25FL064L Name	Default State (IFX)	Type (IFX)	Definition
Bit 0	N/A	PERMLB	1	OTP	***S25FL064L:*** Permanent Protection Lock Bit (PERMLB): • "0" = Permanent Protection Mode permanently enabled • "1" = Permanent Protection Mode not permanently enabled IRP[0] is programmable if IRP[2:0]= "111".
Bit 1	N/A	PSLMLB	1	OTP	***S25FL064L:*** Power Supply Lock-down Protection Mode Lock Bit (PSLMLB): • "0" = Power Supply Lock-down protection Mode permanently enabled. • "1" = Power Supply Lock-down protection Mode not permanently enabled. IRP[1] is programmable if this is enabled by IRP[2:0]= "111"
Bit 2	N/A	PWDMLB	1	OTP	***S25FL064L:*** Password Protection Mode Lock Bit (PWDMLB): • "0" = Password Protection Mode permanently enabled. • "1" = Password Protection Mode not permanently enabled. IRP[2] is programmable if IRP[2:0]= "111".
Bit 3	N/A	RFU	1		Reserved for Future Use
Bit 4	N/A	IBLLBB	1	OTP	***S25FL064L:*** IBL Lock Boot Bit (IBLLBB): • "0" = All individual IBL bits are set to "1" at power-up in the unprotected state

S25FL064L = Individual and Region Protection Register (IRP)

Bit	IS25LQ032B Name	S25FL064L Name	Default State (IFX)	Type (IFX)	Definition
					• "1" = All individual IBL bits are set to "0" at power-up in the protected state IRP[4] is programmable if IRP[2:0]= "111".
Bit 5	N/A	RFU	1		Reserved for Future Use
Bit 6	N/A	SECRRP	1	OTP	***S25FL064L:*** Security Regions Read Password Mode Enable (SECRRP): • "0" = Security Region 3 Read password mode selected • "1" = Security Region 3 Read Password not selected IRP[6] is programmable if IRP[2:0]= "111".
Bit 15 to 7	N/A	RFU	All bits are 'ONE'	OTP	Reserved for Future

8 S25FL064L = Password Register (PASS)

The Password Register (PASS) is a 64-bit OTP memory location used to permanently define a password for the Individual and Region Protection (IRP) feature. PASS does not have user programmable volatile bits; all defined bits are OTP.

A volatile copy of PASS is used to satisfy read latency requirements, but the volatile register is not user-writable or further described. The Password cannot be read or programmed after IRP[2] is programmed to “0”.

S25FL064L-related Commands:

- Password Read (PASSRD E7h) and Password Program (PASSP E8h)
- Read Any Register (RDAR 65h)
- Write Any Register (WRAR 71h)

Table 16 Password Register (PASS) Default Settings

Bit	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition
63 to 0	N/A	PWD	All bits are ‘ONE’	OTP	***S25FL064L:*** Password (PWD) - Nonvolatile OTP storage of 64-bit password. The password is no longer readable after the password protection mode is selected by programming IRP register bit 2 to zero.

9 S25FL064L = Protection Register (PR)

The Protection Register (PR) does not have separate user-programmable nonvolatile bits; all defined bits are volatile read-only status. The default state of the RFU bits is set by hardware. There is no nonvolatile version of the PR register.

The NVLOCK bit is used to protect the Security Regions 2 and 3 and Pointer Region Protection. When NVLOCK[0] = 0, the Security Regions 2 and 3 and Pointer Region Protection cannot be changed.

Related Commands:

- Protection Register Read (PRRD A7h) Protection Register Lock (PRL A6h)
- Read Any Register (RDAR 65h)

Table 17 Protection Status Register (PR) Default Settings

Bit	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition
Bit 0	N/A	NVLOCK	IRP[2] and IRP[0]	OTP	***S25FL064L:*** Protect Nonvolatile Configuration (NVLOCK): • "0" = Security Regions 2 and 3 and Pointer Region write protected • "1" = Security Regions 2 and 3 and Pointer Region may be written
Bit 1	N/A	RFU	1		Reserved for Future Use
Bit 2					
Bit 3					
Bit 4					
Bit 5					
Bit 6		SECRRP	IRP[6]	OTP	***S25FL064L:*** Security Regions READ Password (SECRRP) • "0" = Security Region 3 password protected from read when NVLOCK = 0 • "1" = Security Region 3 not password protected from read
Bit 7	N/A	RFU	00h		Reserved for Future Use

10 S25FL064L = Individual Block Lock Access Register (IBLAR)

IBLAR does not have user-programmable nonvolatile bits; all bits are a representation of the volatile bits in the IBL array. The default state of the IBL array bits is set by hardware. There is no nonvolatile version of the IBLAR register.

S25FL064L-related Commands:

- IBL Read (IBLRD 3Dh or 4IBLRD E0h)
- IBL Lock (IBL 36h or 4IBL E1h)
- IBL Unlock (IBLUL 39h or 4IBUL E2h)
- Global IBL lock (GBL 7Eh)
- Global IBL unlock (GBUL 98h)

Table 18 Individual Block Lock Access Register (IBLAR)

Bit	IS25LQ032B Name	S25FL064L Name	Default State IFX	Type IFX	Definition
7 to 0	N/A	IBL	IRP[4] = 1, then 00h, else FFh	Volatile	***S25FL064L:*** READ or WRITE IBL for Individual Sectors / Block (IBL): • "00h" = IBL for the sector/block addressed is set to "0" by the IBL, 4IBL, and GBL commands protecting that sector from program or erase operations • "FFh" = IBL for the sector/block addressed is cleared to "1" by the IBUL, 4IBUL, and GBUL commands not protecting that sector from program or erase operations

11 S25FL064L = Pointer Region Protection Register (PRPR)

Pointer Region Protection Register (PRPR) contains user-programmable nonvolatile bits. The default state of the PRPR bits is set by hardware. There is no volatile version of the PRPR register.

S25FL064L-related Commands:

- Set Pointer Region (SPRP FBh or 4SPRP E3h)
- Read Any Register (RDAR 65h)
- Write Any Register (WRAR 71h)

Table 19 PRP Register (PRPR) Default Settings

Bit	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition
A7 to A0	N/A	RFU	FFh		Reserved for Future Use
A8	N/A	RFU	1		Reserved for Future Use
A9	N/A	PRPTB	1	NV	***S25FL064L:*** Pointer Region Protection Top / Bottom (PRPTB): • "0" = Pointer Region Protection starts from the top (high address) • "1" = Pointer Region Protection starts from the bottom (low address)
A10	N/A	PRPEN	1	NV	***S25FL064L:*** Pointer Region Protection Enable (PRPEN): • "0" = Enable Pointer Region Protection • "1" = Disable Pointer Region Protection
A11	N/A	PRPALL	1	NV	***S25FL064L:*** Pointer Region Protection Protect ALL (PRPALL): • "0" = Protect Pointer Region selected sectors • "1" = Protect All sectors
A15 to A12	N/A		Fh	NV	***S25FL064L:*** Pointer Region Protection Address (PRPAD) - Pointer Address A15 to A12
A23 to A16	N/A	PRPAD	FFh	NV	***S25FL064L:*** Pointer Region Protection Address (PRPAD) - Pointer Address A23 to A16
A31 to A24	N/A	RFU	11111111b		Reserved for Future Use

12 S25FL064L = Nonvolatile Data Learning Register (DLRNV)

The Data Learning Pattern (DLP) resides in an 8-bit Nonvolatile Data Learning Register (DLRNV) as well as an 8-bit Volatile Data Learning Register (DLRV). When shipped from Infineon, the DLRNV value is 00h. Once programmed, the DLRNV cannot be reprogrammed or erased; a copy of the data pattern in the DLRNV will also be written to the DLRV. The DLRV can be written to at any time, but on hardware and software reset or power cycles the data pattern will revert to the contents of DLRNV. During the learning phase, the DLP will come from the DLRV. Each IO will output the same DLP value for every clock edge. For example, if the DLP is 34h (or binary 00110100) then during the first clock edge all IOs will output 0; subsequently, during the second clock edge, all I/Os will output 0, during the third, will output 1, and so on. When the DLRV value is 00h, no preamble data pattern is presented during the dummy phase in the DDR commands.

S25FL064L-related Commands:

- Program DLRNV (PDLRNV 43h)
- Write DLRV (WDLRV 4Ah)
- Data Learning Pattern Read (DLPRD 41h)
- Read Any Register (RDAR 65h)
- Write Any Register (WRAR 71h)

Table 20 Nonvolatile Data Learning Register (DLRNV) Default Settings

Bit	IS25LQ032B Name	S25FL064L Name	Default State S25FL064L	Type S25FL064L	Definition
7 to 0	N/A	NVDLP	00h	OTP	***S25FL064L:*** Nonvolatile Data Learning Pattern (NVDLP) - OTP value that may be transferred to the host during DDR read command latency (dummy) cycles to provide a training pattern to help the host more accurately center the data capture point in the received data bits.

12.1 S25FL064L = Volatile Data Learning Register (DLRV)

The DLRV can be written to at any time, but on hardware and software reset or power cycles the data pattern will revert to the contents of DLRNV. During the learning phase, the DLP will come from the DLRV. Each IO will output the same DLP value for every clock edge. For example, if the DLP is 34h (or binary 00110100), then during the first clock edge all IOs will output 0; subsequently, during the second clock edge, all I/Os will output 0, during the third will output 1, and so on. When the DLRV value is 00h, no preamble data pattern is presented during the dummy phase in the DDR commands.

Table 21 Volatile Data Learning Register (DLRV)

Bit	IS25LQ032B Name	S25FL064L Name	Default State IFX	Type IFX	Definition
7 to 0	N/A	VDLP	Takes the value of DLRNV during POR or Reset	Volatile	***S25FL064L:*** Volatile Data Learning Pattern (VDLP) - Volatile copy of the NVDLP used to enable and deliver the Data Learning Pattern (DLP) to the

S25FL064L = Nonvolatile Data Learning Register (DLRNV)

Bit	IS25LQ032B Name	S25FL064L Name	Default State IFX	Type IFX	Definition
					outputs. The VDLP may be changed by the host during system operation.

13 Conclusion

Migration from ISSI IS25LQ032B to the Infineon S25FL064L requires special attention to the different register requirements and settings, and to the command Hex values. Migration is not straight forward and requires either system software, hardware accommodation, or both. Once accommodations are made, the S25FL064L Flash can enable use of higher memory densities with greater performance in existing systems.

References

[1] S25FL064L Datasheet - Doc. Number: 002-12878 Rev. *F

[2] IS25LQ032B Datasheet - Rev. H5 (09/03/2019)

Revision history

Document version	Date of release	Description of changes

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