

## OTP Memory Programming and NVRAM Development - CYW4373

**Author: DK Chen****Associated Part Family: CYW4373**

This application note describes the method for creating an *nvr.am.txt* file, which is then used to test a new board design, optimize NVRAM values, and program the one-time programmable (OTP) nonvolatile memory in the CYW4373 device using the USB or SDIO host interface for WLAN.

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## 1 Introduction

The Cypress CYW4373 is a single-chip IEEE 802.11a/b/g/n/ac + BT 5.0 device for embedded and IoT applications. OTP nonvolatile memory is included in the WLAN section of the device to store board-specific information such as SDIO header, product ID, manufacturer ID, and MAC address. Excluding the internal header information, up to 768 bytes of user accessible OTP memory is available on CYW4373 for WLAN information. The application note provides OTP programming information for both USB and SDIO host interfaces.

The OTP memory content, along with an editable NVRAM file (*nvr.am.txt* file), provides all configuration information used by the WLAN device driver to initialize and configure CYW4373.

### 1.1 IoT Resources

Cypress provides a wealth of data at <http://www.cypress.com/internet-things-iot> to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (<http://community.cypress.com/>).

## 2 OTP Memory Programming Considerations

In embedded designs, the host and device are permanently connected, which is typically done using a hardwired USB or SDIO interface. The only entry which is mandatory to be programmed into the OTP memory is the SDIO header. This is because there are certain SDIO function settings which are read before the firmware and NVRAM are downloaded. To properly set these settings, the SDIO header must be programmed into their OTP memory.

Other than the SDIO header, all other NVRAM parameters can be stored in the host's nonvolatile memory rather than in the OTP memory. For non-embedded devices that may be installed on different hosts, the OTP memory can be programmed to protect the unique MAC address and prevent end-users from altering the power control parameters, such as maximum output power.

The initial state of all OTP bits in an unprogrammed device is 0. Individual bits can be set to 1, but once set, the bits can never be reset to 0. The entire OTP array can be programmed in a single-write cycle using the `w1` commands provided with the USB or SDIO driver. As an alternative, multiple write cycles can be used to selectively program specific fields. However, only the bits that are still in the 0 state can be set to the 1 state during each programming cycle.

The OTP programming process is irreversible, so it is recommended that you finalize all NVRAM parameters before programming any parameter into the OTP memory. Test the boards and modules using only the editable `nvr.am.txt` file.

The driver loads the parameters stored in the `nvr.am.txt` file onto an on-chip RAM, allowing the chip to be tested even if the OTP memory has only been programmed with the SDIO header. This method allows you to tune the RF components and alter critical parameters using different versions of the `nvr.am.txt` file while testing boards. Optionally, a few basic parameters, such as the board type and MAC address, can be programmed into the OTP memory prior to testing the board during development.

**Note:** If a parameter is present in both the on-chip OTP memory and the `nvr.am.txt` file, the value in the OTP memory takes priority over the value in the `nvr.am.txt` file.

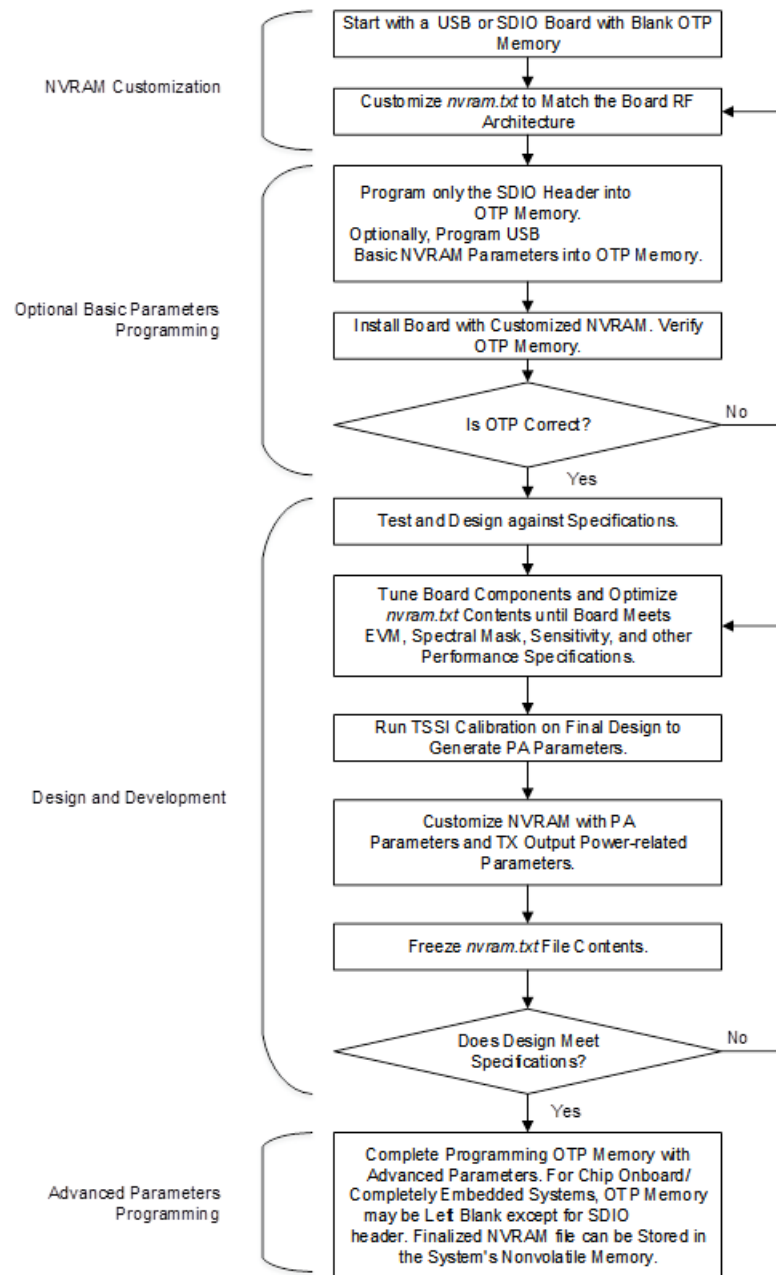
**Note:** The programming process of an OTP memory is irreversible. Cypress strongly recommends conducting development on boards using the parameters provided in the editable `nvr.am.txt` file. Do not program the OTP memory until the contents of the `nvr.am.txt` file have been verified and the file has been finalized for production use. The one exception to this is the SDIO header, which must be programmed into OTP memory for full SDIO functionality.

### 3 NVRAM Content Development and Memory Programming Flow

Figure 1 shows the `nvr.am.txt` file content development and the OTP memory programming flow. Parameters in the `nvr.am.txt` file can be divided into basic (see Table 3) and advanced (see Table 2) categories.

**Note:** Conduct the NVRAM development and OTP programming flow shown in Figure 1 on fewer boards/modules during the product development stage. Once this process is complete and the production version of the `nvr.am.txt` file and OTP memory file is approved for production use, programming can begin for high volume mass production as defined by each manufacturer.

Figure 1. NVRAM Development and Programming Flow of OTP Memory



## 4 Customizing *nvram.txt* File

This section describes customizing, editing, and finalizing the *nvram.txt* file for OTP memory programming.

### 4.1 Using *nvram.txt* File Template

For each reference board design, Cypress provides an *nvram.txt* file for the specific board design. Typically, the file is named in accordance with the board it supports (for example, *cyw989373w/psd.txt*).

The *nvr.am.txt* file might be included with the reference board design package or the driver release. You can download the latest version of the file from the [Cypress Developer Community](#).

Table 1 provides a list of parameters in a typical *nvr.am.txt* file that are common to dual-band 802.11ac USB or SDIO reference design boards.

Parameters in the *nvr.am.txt* file do not need to be entered in any specific order.

**Note:** The parameters listed in Table 1 are used and specified by Cypress and should only be changed by Cypress. It is important that Cypress reviews a customer's design early in the development process. Some of the parameters in Table 1 may need to be changed by Cypress to accommodate differences in the RF front end between the customer's design and the Cypress reference design from which it was derived.

Table 1. Cypress-specific NVRAM Parameters

NVRAM Parameter	Example Data	Description
sromrev	11	SROM revision for 802.11ac chips
boardtype	0x83d	This is a critical parameter that should be copied from a similar Cypress reference board design.
tssipos2g	1	This represents if TSSI has positive slope for 2.4 GHz. For CYW4373, set the value to 1.
tssipos5g	1	This represents if TSSI has positive slope for 5 GHz. For CYW4373, set the value to 1.
rxchain	1	This specifies the number of rx paths (bit mask). For CYW4373, set the value to 1.
txchain	1	This specifies the number of tx paths (bit mask). For CYW4373, set the value to 1.
venid	0x14e4	PCI Vendor ID
devid	0x4418	Chip ID, CYW4373
manfid	0x2d0	Manufacturer ID
nocrc	1	Check for CRC errors when loading firmware
boardflags boardflags2 boardflags3	0x00000001 0x00800000 0x44202100	Board configuration flag that defines the power topology, external components (iPA/iLNA or ePA/eLNA), and so on
tworangetssi2g tworangetssi5g	0 0	2.4 GHz and 5 GHz TSSI dual power range flag, which iPA chips support
xtalfreq	37400	Describes the reference oscillator frequency in kHz. '37400' stands for 37.4 MHz
extpagain2g	2	Supports 2.4 GHz external PA. Use 2 for iPA boards, and use 0 for ePA boards.
extpagain5g	2	Supports 5 GHz external PA. Use 2 for iPA boards, and use 0 for ePA boards.
aa2g, aa5g	1	Number of antennas available for the 2.4 GHz and 5 GHz bands, respectively, in bit-mapped binary format: <ul style="list-style-type: none"> <li>1 = 01b for one antenna</li> <li>3 = 11b for two antennas</li> </ul>
sub-band5gver	0x4	Defines 5 GHz sub-band allocation
tempthresh	105	This parameter is for Cypress internal use only <b>Note:</b> Do not modify.
temps_tx duty_lowlimit	0	This parameter is for Cypress internal use only <b>Note:</b> Do not modify.
phycal_tempdelta	15	This parameter is for Cypress internal use only <b>Note:</b> Do not modify.
temps_period	1	This parameter is for Cypress internal use only <b>Note:</b> Do not modify.
temps_hysteresis	20	This parameter is for Cypress internal use only <b>Note:</b> Do not modify.
AvVmid_c0	1, 115, 1, 120, 1, 120, 1, 120, 1, 120	This parameter is for Cypress internal use only. <b>Note:</b> Do not modify.

NVRAM Parameter	Example Data	Description
swctrlmap_2g, swctrlmap_5g, swctrlmapext_2g/5g	0x00000010, 0x00000050, 0x00000000, 0x000000	Describes how to control the external 2.4 GHz and 5 GHz FEM (front-end module) or TR-SW.

The design variables listed in [Table 2](#) must be reviewed prior to beginning board or module testing. During the development phase, start with the default power amplifier (PA) parameters listed in the provided *nvrmap.txt* file. The PA parameters are eventually optimized using Cypress transmit signal strength indicator (TSSI) calibration tools.

The parameters in [Table 2](#) typically require tuning for each board-specific or module design. This is not an exhaustive list. Cypress might add additional parameters at any time to control the RF performance-related attributes of the driver. Always check with Cypress for the latest version of the *nvrmap.txt* file for the reference design before starting any board customization efforts.

**Note:** To avoid unexpected operating results, contact a technical support representative before attempting to add NVRAM parameters.

Table 2. NVRAM Parameters Requiring Customization

NVRAM Parameter	Example Data	Description
boardrev	0x1306	Board revision used by the WLAN driver. Examples: 0x1107 converts to P107 0x1306 converts to P306
ccode	0	Country code for regulatory. Specifies which regulatory tables are to be loaded. <b>Note:</b> Together, the ccode and regrev parameters set the power and other limitations necessary to meet the country-specific regulatory requirements.
regrev	0	The regulatory revision code for regulatory use, and specifies which regulatory tables are to be loaded. <b>Note:</b> Together, the ccode and regrev parameters set the power and other limitations necessary to meet the country-specific regulatory requirements.
rxgains2gtrelnabypa0	1	This variable indicates whether an external LNA bypass is used instead of a TR switch when transmitting. Set to 1 if using an external LNA bypass (for 2.4 GHz).
rxgains5gtrelnabypa0	1	This variable indicates whether an external LNA bypass is used instead of a TR switch when transmitting. Set to 1 if using an external LNA bypass (for 5 GHz). Applies to the low sub-band.
rxgains5gmtrelnabypa0	1	This variable indicates whether an external LNA bypass is used instead of a TR switch when transmitting. Set to 1 if using an external LNA bypass (for 5 GHz). Applies to the mid sub-band.
rxgains5ghtrelnabypa0	1	This variable indicates whether an external LNA bypass is used instead of a TR switch when transmitting. Set to 1 if using an external LNA bypass (for 5 GHz). Applies to the high/X1 sub-band.
rxgains2gelnagaina0	3	This variable defines the 2.4 GHz eLNA gain. Gain (dB) = 2 × rxgains2gelnagaina0 + 6. For rxgains2gelnagaina0 = 3, the gain is 12 dB.
rxgains2gtrisoa0	6	This variable defines the 2.4 GHz isolation provided by the TR switch when transmitting. Isolation (dB) = 2 × rxgains2gtrisoa0 + 8. For rxgains2gtrisoa0 = 6, the isolation is 20 dB.
rxgains5gelnagaina0	3	This variable defines the 5 GHz, low sub-band, eLNA gain. Gain (dB) = 2 × rxgains5gelnagaina0 + 6. For rxgains5gelnagaina0 = 3, the gain is 12 dB

NVRAM Parameter	Example Data	Description
rxgains5gtrisoa0	6	This variable defines the 5 GHz, low sub-band isolation provided by the TR switch when transmitting. Isolation (dB) = $2 \times \text{rxgains5gtrisoa0} + 8$ . For rxgains5gtrisoa0 = 6, the isolation is 20 dB.
rxgains5gelnagaina0	3	This variable defines the 5 GHz, mid sub-band, eLNA gain. Gain (dB) = $2 \times \text{rxgains5gelnagaina0} + 6$ . For rxgains5gelnagaina0 = 3, the gain is 12 dB
rxgains5gmtrisoa0	6	This variable defines the 5 GHz, mid sub-band isolation provided by the TR switch when transmitting. Isolation (dB) = $2 \times \text{rxgains5gtrisoa0} + 8$ . For rxgains5gtrisoa0 = 6, the isolation is 20 dB.
rxgains5ghelnagaina0	3	This variable defines the 5 GHz, high/X1 sub-band, eLNA gain. Gain (dB) = $2 \times \text{rxgains5gelnagaina0} + 6$ . For rxgains5gelnagaina0 = 3, the gain is 12 dB
rxgains5ghtrisoa0	6	This variable defines the 5 GHz, high/X1 sub-band isolation provided by the TR switch when transmitting. Isolation (dB) = $2 \times \text{rxgains5gtrisoa0} + 8$ . For rxgains5gtrisoa0 = 6, the isolation is 20 dB.
agbg0, aga0	0x7f	Antenna gain (in dBi) defined by converting hexadecimal to 8-bit binary: (agba0: 2.4 GHz antenna gain, aga0: 5 GHz antenna gain) <ul style="list-style-type: none"> <li>Lower 0–5 bits = signed 2s complement in units of dB.</li> <li>Higher 6–7 bits = unsigned number in units of quarter dB.</li> </ul> Examples: 0x82 = 2.5 dB ( $2 + 2 \times 0.25$ ) 0x7f = -0.75 dB ( $-1 + 1 \times 0.25$ )
pa2ga0	-148, 5828, -679	PA parameters for the 2.4 GHz band based on TSSI calibration. pa2ga0 – OFDM
pa5ga0	83, 6045, -553, 57, 5940, -566, 12, 5919, -605, -17, 5899, -640	PA parameters for the 5 GHz band based on TSSI calibration (Low / Mid / High / X1). Sub-band frequency range. Channel Range: <ul style="list-style-type: none"> <li>Low 5180 to 5240 36-48</li> <li>Mid 5260 to 5320 52-64</li> <li>High 5500 to 5700 100-140</li> <li>X1 5745 to 5825 149-165 (pa5ga0)</li> </ul>
pdoffset40ma0	0x0000	5 GHz, 40 MHz BW power detect (PD) offset (1/4 dB steps) in 2s complement format. 4 bits for each sub-band. The most significant nibble is the X1 sub-band offset.
pdoffset80ma0	0x0000	5 GHz, 80 MHz BW PD offset (in 1/4 dB steps) in 2s complement format 4 bits for each sub-band. The most significant nibble is the X1 sub-band offset.
maxp2ga0	0x46	Maximum output power for the 2.4 GHz band in hexadecimal format. Units of 0.25 dB. This applies to all complementary code keying (CCK) rates as measured at antenna port. The nominal target power in dBm for CCK packets is $(0.25 \times \text{maxp2ga0 in decimal}) - 1.5$ dB. The value can be entered in either hexadecimal or decimal formats. In the example shown for 0 x 46, the maximum output power is $(16 \times 4 + 6)/4 = 17.5$ dBm, and the nominal power is $17.5 - 1.5 = 16.0$ dBm.
cckbw202gpo	0x0000	CCK unsigned power offsets (in 1/2 dB steps) for the 20 MHz rates (11, 5.5, 2, 1 Mbps). The most significant nibble is the 11 Mbps offset.

NVRAM Parameter	Example Data	Description
cckbw20ul2gpo	0x0000	CCK unsigned power offsets in 1/2 dB steps for 20 U/L rates (11, 5.5, 2, 1 Mbps). The most significant nibble is the 11 Mbps offset
pdoffsetcckma0	0x4	Core 0 2g CCK PD offset (1/4 dB steps) in 2's complement format - For example, if 1dB reduction is required then the value is 0x4, but if 1dB higher offset is required then it is 0xc.
dot11agofdmhrbw202gpo	0x6666	OFDM unsigned power offsets in 1/2 dB steps for 54, 48, 36, and 24 Mbps. The most significant nibble is the 54 Mbps rate offset
ofdmrlbw202gpo	0x0033	OFDM 2.4 GHz, unsigned power offsets in 1/2 dB steps: <ul style="list-style-type: none"> <li>• MCS1 and MCS2: 11n and 11ac 40 MHz BW</li> <li>• (most significant nibble)</li> <li>• MCS1 and MCS2: 11n and 11ac 20 MHz BW</li> <li>• 12 and 18 Mbps: 11g</li> <li>• 6 and 9 Mbps: 11g</li> </ul>
mcsbw202gpo	0xAA886664	11n/ac MCS0/1/2, 3-7, C8, C9 2.4 MHz unsigned power offsets in 1/2 dB steps – C9/C8/M7/M6/M5/M4/M3/M0-2. (If separate control of MCS1 and MCS2 is required, then use ofdmrlbw202gpo).
maxp5ga0	0x4A, (low) 0x4A, (mid) 0x4A, (high) 0x4A (X1)	Maximum output power for the 5 GHz band in hexadecimal format. Units of 0.25 dB. This applies to all legacy orthogonal frequency division multiplexing (OFDM) rates as measured at antenna port. The nominal target power in dBm is (0.25 × maxp5ga0 in decimal) – 1.5 dB. The value can be entered in either hexadecimal or decimal format.
mcslr5glpo	0x0000	5 GHz band low sub-band 12/18 Mbps and MCS1/2, unsigned power offsets in 1/2 dB steps: <ul style="list-style-type: none"> <li>• (0) 20 MHz (least significant nibble)</li> <li>• (1) 40 MHz</li> <li>• (2) 80 MHz</li> <li>• (3) 160 MHz</li> </ul>
mcsbw205glpo	0xAA886662	5 GHz, low sub-band, 11n/ac, 20 MHz, unsigned power offsets in 1/2 dB steps. The most significant nibble is the power offset for MCS9 and the least significant nibble is for MCS0–2. <ul style="list-style-type: none"> <li>• C9/C8/M7/M6/M5/M4/M3/M0-2</li> </ul>
mcsbw405glpo	0xAA886664	5 GHz, low sub-band, 11n/ac, 40 MHz, unsigned power offsets in 1/2 dB steps. The most significant nibble is the power offset for MCS9 and the least significant nibble is for MCS0–2. <ul style="list-style-type: none"> <li>• C9/C8/M7/M6/M5/M4/M3/M0-2</li> </ul>
mcsbw805glpo	0xAA886664	5 GHz, low sub-band, 11n/ac, 80 MHz, unsigned power offsets in 1/2 dB steps. The most significant nibble is the power offset for MCS9 and the least significant nibble is for MCS0–2. <ul style="list-style-type: none"> <li>• C9/C8/M7/M6/M5/M4/M3/M0-2</li> </ul>
mcslr5gmpo	0x0000	5 GHz, mid sub-band, 11ag/11n/11ac, QPSK, unsigned power offsets in 1/2 dB steps with respect to BPSK: MCS1/2 with respect to MCS0/1/2, and 12/18 Mbps with respect to 6/9 Mbps. <ul style="list-style-type: none"> <li>• (0) 20 MHz (least significant nibble)</li> <li>• (1) 40 MHz</li> <li>• (2) 80 MHz</li> <li>• (3) 160 MHz</li> </ul>
mcsbw205gmpo	0xAA886664	5 GHz, mid sub-band, 11n/ac, 20 MHz, unsigned power offsets in 1/2 dB steps. The most significant nibble is the power offset for MCS9 and the least significant nibble is for MCS0–2. <ul style="list-style-type: none"> <li>• C9/C8/M7/M6/M5/M4/M3/M0-2</li> </ul>
mcsbw405gmpo	0xAA886664	5 GHz, mid sub-band, 11n/ac, 40 MHz, unsigned power offsets in 1/2 dB steps. The most significant nibble is the power offset for MCS9 and the least significant nibble is for MCS0–2. <ul style="list-style-type: none"> <li>• C9/C8/M7/M6/M5/M4/M3/M0-2</li> </ul>

NVRAM Parameter	Example Data	Description
mcsbw805gmpo	0xAA886664	5 GHz, mid sub-band, 11n/ac, 80 MHz, unsigned power offsets in 1/2 dB steps. The most significant nibble is the power offset for MCS9 and the least significant nibble is for MCS0–2. <ul style="list-style-type: none"> <li>• C9/C8/M7/M6/M5/M4/M3/M0-2</li> </ul>
mcslr5ghpo	0x0000	5 GHz, high/X1 band 11ag/11n/11ac, QPSK, unsigned power offsets in 1/2 dB steps with respect to BPSK: MCS1/2 with respect to MCS0/1/2, and 12/18 Mbps with respect to 6/9 Mbps. <ul style="list-style-type: none"> <li>• (0) 20 MHz (least significant nibble)</li> <li>• (1) 40 MHz</li> <li>• (2) 80 MHz</li> <li>• (3) 160 MHz</li> </ul>
mcsbw205ghpo	0xAA886664	5 GHz, high/X1 sub-band, 11n/ac, 20 MHz, unsigned power offsets in 1/2 dB steps. The most significant nibble is the power offset for MCS9 and the least significant nibble is for MCS0–2. <ul style="list-style-type: none"> <li>• – C9/C8/M7/M6/M5/M4/M3/M0-2</li> </ul>
mcsbw405ghpo	0xAA886664	5 GHz, high/X1 sub-band, 11n/ac, 40 MHz, unsigned power offsets in 1/2 dB steps. The most significant nibble is the power offset for MCS9 and the least significant nibble is for MCS0–2. <ul style="list-style-type: none"> <li>• C9/C8/M7/M6/M5/M4/M3/M0-2</li> </ul>
mcsbw805ghpo	0xAA886664	5 GHz, high/X1 sub-band, 11n/ac, 80 MHz, unsigned power offsets in 1/2 dB steps. The most significant nibble is the power offset for MCS9 and the least significant nibble is for MCS0–2. <ul style="list-style-type: none"> <li>• C9/C8/M7/M6/M5/M4/M3/M0-2</li> </ul>
sb20in40hrpo	0	20in40 OFDM signed power offsets (in 1/2 dB steps) with respect to 20in20 for 64 QAM and above. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>• (0) 2.4 GHz band</li> <li>• (1) 5 GHz low sub-band</li> <li>• (2) 5 GHz mid sub-band</li> <li>• (3) 5 GHz high/X1 sub-band</li> </ul>
sb20in80and160hr5glpo	0	20in40 OFDM signed power offsets (in 1/2 dB steps) with respect to 20in20 for 64 QAM and above. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>• (0) 2.4 GHz band</li> <li>• (1) 5 GHz low sub-band</li> <li>• (2) 5 GHz mid sub-band</li> <li>• (3) 5 GHz high/X1 sub-band</li> </ul>
sb20in80and160hr5glpo	0	5 GHz low sub-band 20in80, 20in160 OFDM signed power offsets (in 1/2 dB steps) for 64 QAM and above. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>• (0) 20in80 with respect to 20in20</li> <li>• (1) 20in160 with respect to 20in20</li> <li>• (2) 20in80 - 20LL/UU with respect to 20LU/UL</li> <li>• (3) 20in160 - 20LLL/UUU with respect to other 20in160 sub-bands</li> </ul>
sb40and80hr5glpo	0	5 GHz low sub-band 40in80, 40in160 OFDM signed power offsets (in 1/2 dB steps) for 64 QAM and above. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>• (0) 40in80 with respect to 40in40</li> <li>• (1) 40in160 with respect to 40in40</li> <li>• (2) 80in160 with respect to 80in80</li> <li>• (3) 40in160 -40LL/UU with respect to 40LU/UL</li> </ul>
sb20in80and160hr5gmpo	0	5 GHz mid sub-band 20in80, 20in160 OFDM signed power offsets (in 1/2 dB steps) for 64 QAM and above. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>• (0) 20in80 with respect to 20in20</li> <li>• (1) 20in160 with respect to 20in20</li> <li>• (2) 20in80 - 20LL/UU with respect to 20LU/UL</li> <li>• (3) 20in160 - 20LLL/UUU with respect to other 20in160 sub-bands</li> </ul>



NVRAM Parameter	Example Data	Description
sb40and80hr5gmpo	0	5 GHz mid sub-band 40in80, 40in160 OFDM signed power offsets (in 1/2 dB steps) for 64 QAM and above. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>• (0) 40in80 with respect to 40in40</li> <li>• (1) 40in160 with respect to 40in40</li> <li>• (2) 80in160 with respect to 80in80</li> <li>• (3) 40in160 -40LL/UU with respect to 40LU/UL</li> </ul>
sb20in80and160hr5ghpo	0	5 GHz high/X1 sub-band 20in80, 20in160 OFDM signed power offsets (in 1/2 dB steps) for 64 QAM and above. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>• (0) 20in80 with respect to 20in20</li> <li>• (1) 20in160 with respect to 20in20</li> <li>• (2) 20in80 - 20LL/UU with respect to 20LU/UL</li> <li>• (3) 20in160 - 20LLL/UUU with respect to other 20in160 sub-bands</li> </ul>
sb40and80hr5ghpo	0	5 GHz high/X1 sub-band 40in80, 40in160 OFDM signed power offsets (in 1/2 dB steps) for 64 QAM and above. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>• (0) 40in80 with respect to 40in40</li> <li>• (1) 40in160 with respect to 40in40</li> <li>• (2) 80in160 with respect to 80in80</li> <li>• (3) 40in160 -40LL/UU with respect to 40LU/UL</li> </ul>
sb20in40lrpo	0	20in40 OFDM signed power offsets (in 1/2 dB steps) with respect to 20in20 for 16 QAM and below. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>• (0) 2.4 GHz band</li> <li>• (1) 5 GHz low sub-band</li> <li>• (2) 5 GHz mid sub-band</li> <li>• (3) 5 GHz high/X1 sub-band</li> </ul>
sb20in80and160lr5glpo	0	5 GHz low sub-band 20in80, 20in160 OFDM signed power offsets (in 1/2 dB steps) for 16 QAM and below. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>• (0) 20in80 with respect to 20in20</li> <li>• (1) 20in160 with respect to 20in20</li> <li>• (2) 20in80 - 20LL/UU with respect to 20LU/UL</li> <li>• (3) 20in160 - 20LLL/UUU with respect to other 20in160 sub-bands</li> </ul>
sb40and80lr5glpo	0	5 GHz mid sub-band 20in80, 20in160 OFDM signed power offsets (in 1/2 dB steps) for 64 QAM and above. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>• (0) 20in80 with respect to 20in20</li> <li>• (1) 20in160 with respect to 20in20</li> <li>• (2) 20in80 - 20LL/UU with respect to 20LU/UL</li> <li>• (3) 20in160 - 20LLL/UUU with respect to other 20in160 sub-bands</li> </ul>
sb40and80hr5gmpo	0	5 GHz mid sub-band 40in80, 40in160 OFDM signed power offsets (in 1/2 dB steps) for 64 QAM and above. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>• (0) 40in80 with respect to 40in40</li> <li>• (1) 40in160 with respect to 40in40</li> <li>• (2) 80in160 with respect to 80in80</li> <li>• (3) 40in160 -40LL/UU with respect to 40LU/UL</li> </ul>
sb20in80and160hr5ghpo	0	5 GHz high/X1 sub-band 20in80, 20in160 OFDM signed power offsets (in 1/2 dB steps) for 64 QAM and above. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>• (0) 20in80 with respect to 20in20</li> <li>• (1) 20in160 with respect to 20in20</li> <li>• (2) 20in80 - 20LL/UU with respect to 20LU/UL</li> <li>• (3) 20in160 - 20LLL/UUU with respect to other 20in160 sub-bands</li> </ul>

NVRAM Parameter	Example Data	Description
sb40and80hr5ghpo	0	5 GHz high/X1 sub-band 40in80, 40in160 OFDM signed power offsets (in 1/2 dB steps) for 64 QAM and above. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>(0) 40in80 with respect to 40in40</li> <li>(1) 40in160 with respect to 40in40</li> <li>(2) 80in160 with respect to 80in80</li> <li>(3) 40in160 -40LL/UU with respect to 40LU/UL</li> </ul>
sb20in40lrpo	0	20in40 OFDM signed power offsets (in 1/2 dB steps) with respect to 20in20 for 16 QAM and below. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>(0) 2.4 GHz band</li> <li>(1) 5 GHz low sub-band</li> <li>(2) 5 GHz mid sub-band</li> <li>(3) 5 GHz high/X1 sub-band</li> </ul>
sb20in80and160lr5glpo	0	5 GHz low sub-band 20in80, 20in160 OFDM signed power offsets (in 1/2 dB steps) for 16 QAM and below. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>(0) 20in80 with respect to 20in20</li> <li>(1) 20in160 with respect to 20in20</li> <li>(2) 20in80 - 20LL/UU with respect to 20LU/UL</li> <li>(3) 20in160 - 20LLL/UUU with respect to other 20in160 sub-bands</li> </ul>
sb40and80lr5glpo	0	5 GHz low sub-band 40in80, 40in160 OFDM signed power offsets (in 1/2 dB steps) for 16 QAM and below. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>(0) 40in80 with respect to 40in40</li> <li>(1) 40in160 with respect to 40in40</li> <li>(2) 80in160 with respect to 80in80</li> <li>(3) 40in160 -40LL/UU with respect to 40LU/UL</li> </ul>
sb20in80and160lr5gmpo	0	5 GHz mid sub-band 20in80, 20in160 OFDM signed power offsets (in 1/2 dB steps) for 16 QAM and below. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>(0) 20in80 with respect to 20in20</li> <li>(1) 20in160 with respect to 20in20</li> <li>(2) 20in80 - 20LL/UU with respect to 20LU/UL</li> <li>(3) 20in160 - 20LLL/UUU with respect to other 20in160 sub-bands</li> </ul>
sb40and80lr5gmpo	0	5 GHz mid sub-band 40in80, 40in160 OFDM signed power offsets (in 1/2 dB steps) for 16 QAM and below. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>(0) 40in80 with respect to 40in40</li> <li>(1) 40in160 with respect to 40in40</li> <li>(2) 80in160 with respect to 80in80</li> <li>(3) 40in160 -40LL/UU with respect to 40LU/UL</li> </ul>
sb20in80and160lr5ghpo	0	5 GHz high/X1 sub-band 20in80, 20in160 OFDM signed power offsets (in 1/2 dB steps) for 16 QAM and below. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>(0) 20in80 with respect to 20in20</li> <li>(1) 20in160 with respect to 20in20</li> <li>(2) 20in80 - 20LL/UU with respect to 20LU/UL</li> <li>(3) 20in160 - 20LLL/UUU with respect to other 20in160 sub-bands</li> </ul>
sb40and80lr5ghpo	0	5 GHz high/X1 sub-band 40in80, 40in160 OFDM signed power offsets (in 1/2 dB steps) for 16 QAM and below. LSB nibble to MSB nibble: <ul style="list-style-type: none"> <li>(0) 40in80 with respect to 40in40</li> <li>(1) 40in160 with respect to 40in40</li> <li>(2) 80in160 with respect to 80in80</li> <li>(3) 40in160 - 40LL/UU with respect to 40LU/UL</li> </ul>
dot11agduphrpo	0	11a/g duplicate mode signed power offsets (in 1/2 dB steps) for 64 QAM. Common power offset for Dup40, Dup40in80, and Dup40in160 with respect to 40in40 11n/11ac, Quad80 and Quad80in160 with respect to 11ac 80in80, Oct160 with respect to 11ac 160in160. LSB to MSB nibble: <ul style="list-style-type: none"> <li>(0) 2.4 GHz band</li> <li>(1) 5 GHz low sub-band</li> <li>(2) 5 GHz mid sub-band</li> <li>(3) 5 GHz high/X1 sub-band</li> </ul>

NVRAM Parameter	Example Data	Description
dot11agduplrpo	0	Bits 11a/g duplicate mode signed power offsets (in 1/2 dB steps) for 16 QAM and below. Common power offset for Dup40, Dup40in80, and Dup40in160 with respect to 40in40 11n/11ac, Quad80 and Quad80in160 with respect to 11ac 80in80, Oct160 with respect to 11ac 160in160. LSB to MSB nibble: <ul style="list-style-type: none"> <li>(0) 2.4 GHz band</li> <li>(1) 5 GHz low sub-band</li> <li>(2) 5 GHz mid sub-band</li> <li>(3) 5 GHz high/X1 sub-band</li> </ul>
mux_enab	0x11	Specifies GPIO pin for out-of-band (OOB) interrupts.
btc_mode	1	Specifies BT-COEX mode. Needed only for sLNA configuration.
ltecmux	0x534201	Specifies LTE Coex settings.
cckdigfilttype	4	Specifies filter type for 11b mode.
rss_delta_2g_c0	-1, -1, -1, -1	Array of measured delta from expected power (in 1 dB step) during cal for 2G (recommended channel 6); first two for 20 MHz, and next two for 40 MHz. There are two for gi 1 and 4 in each bandwidth mode. LSB to MSB nibble: <ul style="list-style-type: none"> <li>(0) 40MHz BW, -70dBm ref signal power</li> <li>(1) 40MHz BW, -25dBm ref signal power</li> <li>(2) 20MHz BW, -70dBm ref signal power</li> <li>(3) 20MHz BW, -25dBm ref signal power</li> </ul>
rss_delta_5gl_c0	-2, -2, -4, -4, -3, -3	Array of measured delta from expected power (in 1 dB step) during cal for 5G (lower sub-band, recommended channel 5180 MHz); first two for 20MHz, next two for 40 MHz, and last two for 80 MHz. There are two for gi 1 and 4 in each bandwidth mode. LSB to MSB nibble: <ul style="list-style-type: none"> <li>(0) 80MHz BW, -70dBm ref signal power</li> <li>(1) 80MHz BW, -25dBm ref signal power</li> <li>(2) 40MHz BW, -70dBm ref signal power</li> <li>(3) 40MHz BW, -25dBm ref signal power</li> <li>(4) 20MHz BW, -70dBm ref signal power</li> <li>(5) 20MHz BW, -25dBm ref signal power</li> </ul>
rss_delta_5gml_c0	-2, -2, -4, -4, -4, -4	Array of measured delta from expected power (in 1 dB step) during cal for 5G (mid-low sub-band, recommended channel 5500 MHz); first two for 20 MHz, next two for 40 MHz, and last two for 80 MHz. There are two for gi 1 and 4 in each bandwidth mode. LSB to MSB nibble: <ul style="list-style-type: none"> <li>(0) 80MHz BW, -70dBm ref signal power</li> <li>(1) 80MHz BW, -25dBm ref signal power</li> <li>(2) 40MHz BW, -70dBm ref signal power</li> <li>(3) 40MHz BW, -25dBm ref signal power</li> <li>(4) 20MHz BW, -70dBm ref signal power</li> <li>(5) 20MHz BW, -25dBm ref signal power</li> </ul>
rss_delta_5gmu_c0	-2, -2, -4, -4, -2, -2	Array of measured delta from expected power (in 1 dB step) during cal for 5G (mid-upper sub-band, recommended channel 5640 MHz); first two for 20 MHz, next two for 40 MHz, and last two for 80 MHz. There are two for gi 1 and 4 in each bandwidth mode. LSB to MSB nibble: <ul style="list-style-type: none"> <li>(0) 80MHz BW, -70dBm ref signal power</li> <li>(1) 80MHz BW, -25dBm ref signal power</li> <li>(2) 40MHz BW, -70dBm ref signal power</li> <li>(3) 40MHz BW, -25dBm ref signal power</li> <li>(4) 20MHz BW, -70dBm ref signal power</li> <li>(5) 20MHz BW, -25dBm ref signal power</li> </ul>

NVRAM Parameter	Example Data	Description
rssi_delta_5gh_c0	-2, -2, -3, -3, -2, -2	Array of measured delta from expected power (in 1 dB step) during cal for 5G (upper sub-band, recommended channel 5795 MHz); first two for 20 MHz, next two for 40 MHz, and last two for 80 MHz. There are two for gi 1 and 4 in each bandwidth mode. LSB to MSB nibble: <ul style="list-style-type: none"> <li>(0) 80MHz BW, -70dBm ref signal power</li> <li>(1) 80MHz BW, -25dBm ref signal power</li> <li>(2) 40MHz BW, -70dBm ref signal power</li> <li>(3) 40MHz BW, -25dBm ref signal power</li> <li>(4) 20MHz BW, -70dBm ref signal power</li> <li>(5) 20MHz BW, -25dBm ref signal power</li> </ul>
powoffs2gtna0	-3, -2, 0, 0, 0, 0, 0, 0, 0, 0, 0, -5, -5	Specifies power offset per channel in 2.4 GHz (Channel 1 to 13).

## 4.2 Editing nvram.txt File

Edit the *nvram.txt* file using a properly formatted text editor such as Notepad++ or WordPad++ to preserve the original format of the file. Using a non-formatted text editor such as Notepad could corrupt the format of the NVRAM map, causing the driver to incorrectly read the *nvram.txt* file.

## 4.3 Finalizing nvram.txt File

After the final PA parameters have been generated, edit the *nvram.txt* file to update the PA parameters derived using the Cypress TSSI tool, and then adjust the Tx output power-related parameters in the file. Using the updated *nvram.txt* file, run output power tests to verify that the parameters are providing the correct output power. Also, verify that RF performance (EVM, spectral mask, and PER) meets design specifications.

Cypress recommends running a regulatory pre-scan to verify that the required output power can be delivered without violating the band-edge limits. If the band-edge limits cannot be met, it may be necessary to reduce the output power at the band-edge channels.

After all prototype tests have passed and all *nvram.txt* file parameters have been optimized and finalized, the required parameters can be selected and the OTP memory programmed for production.

**Note:** The CYW4373 has 368 bytes of space in the OTP memory available for user data and this is for Wifi only (CIS dump). Total OTP contents are 768 bytes (OTP dump). Given the limited space in the OTP memory, it is impossible to program the entire *nvram.txt* file to the OTP memory. Make sure that you select only the necessary parameters that go into the OTP memory.

Parameters that typically go into the OTP memory are those that are unique to the board (such as MAC address) and those that are required to satisfy local regulatory requirements, which are usually output power-related parameters such as maximum output power, power offset per-rate, PA parameters, and country code. Alternately, with many embedded systems, various NVRAM variables are stored in the system's nonvolatile memory as opposed to OTP memory.

## 5 Programming OTP Memory

One item that is required in the OTP memory is the SDIO header. When using the SDIO interface with the CYW4373, there are certain SDIO function settings which are read before the firmware and NVRAM are downloaded. To properly set these settings, the SDIO header must be programmed into their OTP, nonvolatile memory.

Note that the SDIO header should be created as a collaboration between Cypress and the customer. A majority of the SDIO header fields are either generic (and do not need to be changed) or Cypress-specific. There are a few fields that are customer-specific. Coordinate with the Cypress Hardware Applications team supporting the design to confirm the appropriate SDIO header. Note that the SDIO header is a set block of data with a predetermined order. It does not use tuples.

## 5.1 Programming Basic Parameters into OTP Memory

Parameters in the *nvr.am.txt* file that are to be programmed into the OTP memory must be entered in the OTP binary map after the SDIO header. A CIS tuple is required for each parameter in the CIS structure. Most parameters in the *nvr.am.txt* file have a unique identifier called the CIS tuple tag. The driver recognizes and parses each CIS tuple by its tag number.

**Note:** The SDIO header does not use tuples, but is a set block of data with a specific ordering.

Table 3 lists the basic NVRAM parameters, the associated tag number, and the number of bytes each parameter occupies in the OTP memory. Basic parameters typically have fixed values specific to a particular device or board. The value of these parameters is often retained throughout the life of the device/board. For this reason, it is generally acceptable to program these basic parameters into the OTP memory early in the development, before the design is finalized.

Table 3. Basic NVRAM Parameters and CIS Tuple Tags

NVRAM Parameter	CIS Tuple Tag	Length of Value (in Bytes)
Sromrev	0x00	1
Boardrev	0x02	2
Broadtype	0x1b	2
Macaddr	0x19	6
ccode <sup>1</sup>	0x0a	2
sub-band5gver	0x8A	2
sub-band5gver, maxp2ga0, pa2ga0, maxp5ga0, pa5ga0	0x59	38

In the OTP binary map, each tuple is formed by the four fragments described in Table 4.

Table 4. CIS Tuple Format

Fragment	Description
80	Indicates the beginning of a new tuple. 0x80 is specific to Cypress tuple subtags.
Length	Defines the total size (in bytes) of the tag plus the value of the tuple that occupies the OTP memory space.
Tag	Identifies a parameter in the <i>nvr.am.txt</i> file. A tag usually takes one byte in memory.
Value	Specifies the value of the parameter in little-endian format (first byte is the least significant byte).

For example, the tuple is defined by the fragments that follow:

80                      03                      02                      07                      11

- 80 – Beginning of a new tuple.
- 03 – The tag (1 byte) and the value (2 bytes) occupy 3 bytes (total) in the OTP memory.
- 02 – Tag of 0x02 is the identifier for boardrev in the *nvr.am.txt* file.
- 07 11 – The value of boardrev in reverse hexadecimal byte or 0x1107.

Table 5 and Table 6 provide an example OTP binary map for a CYW4373 that contains the SDIO header and some of the *nvr.am.txt* file parameters listed in Table 3.

**Note:** CIS tuples do not have to be listed in any order because each tuple begins with a unique identifier.

**Note:** OTP bytes can be written only once. Only blank and zero-programmed bytes can be programmed during subsequent write cycles.

**Note:** The SDIO header is a set block of data with a predetermined order. Do not use tuples in the SDIO header order. The tuples must be programmed into OTP memory for all SDIO functions to operate properly.

<sup>1</sup> The value for ccode in the *nvr.am.txt* file is in ASCII format. This value must be converted to hexadecimal format before entering it into the OTP binary map (for example, "US" = "0x55 0x53").

Table 5. CYW4373 OTP Map for USB (Required in OTP)

Offset	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xa	0xb	0xc	0xd	0xe	0xf
00000000	80	02	00	0b	80	03	02	07	11	80	03	1b	4a	08	80	07
00000010	19	66	55	44	33	22	11	00	00	00	00	00	00	00	00	00
00000020	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000030	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000040	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000050	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000060	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000070	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000080	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000090	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000a0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000b0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000c0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000d0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000e0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000f0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000100	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000110	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000120	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000130	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000140	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000150	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000160	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

← Other NVRAM Variables (Optional in OTP)

macaddr=66:55:44:33:22:11

boardtype = 0x084a

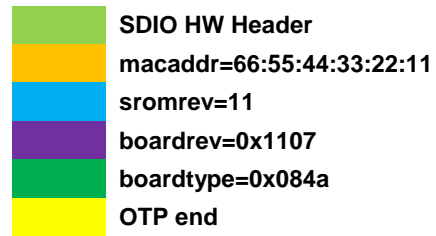
boardrev = 0x1107

sromrev = 11

↑  
**OTP End**

Table 6. CYW4373 OTP Map for SDIO

Offset	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xa	0xb	0xc	0xd	0xe	0xf
00000000	5b	00	ff	ff	00	00	20	04	d0	02	73	43	80	07	19	66
00000010	55	44	33	22	11	80	03	02	07	11	80	02	00	0b	80	03
00000020	1b	4a	08	00	00	00	00	00	00	00	00	00	00	00	00	00
00000030	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000040	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000050	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000060	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000070	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000080	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000090	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000a0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000b0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000c0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000d0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000e0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000f0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000100	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000110	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000120	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000130	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000140	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000150	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000160	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00



**Max WLAN SW/HW Region size = 368 bytes**



## 5.2 Creating and Editing OTP Binary Map

Use a hexadecimal text editor to create and edit an OTP binary map. A hexadecimal text editor preserves formatting of the *nvr.am.txt* file. Writing to the OTP memory requires a bin file that fits in the OTP memory space.

For the CYW4373, the maximum size of the OTP memory is 368 bytes.

**Note:** Do not use Notepad to edit the *nvr.am.txt* file. Edit the *nvr.am.txt* file using a properly formatted text editor such as Notepad++ or WordPad++ to preserve the original format of the file. Using a non-formatted text editor such as Notepad could corrupt the format of the NVRAM map, causing the driver to incorrectly read the *nvr.am.txt* file.

1. Add or edit each byte in the OTP binary map to populate the CIS tuple, as described in the OTP binary map instructions provided in Programming Basic Parameters into OTP Memory.

**Note:** The OTP binary map file (see [Table 7](#) and [Table 8](#)) has been edited to match the example CYW4373 OTP binary map described in [Table 5](#) and [Table 6](#).

2. Save the OTP binary map as a binary image file (*.bin* extension) to the directory containing the *wl* file.

**Note:** Save the file with a *.bin* file extension so that the data it contains can be programmed into the OTP memory. In this application note, this file is referred as *4373\_OTP.bin*.

[Table 7](#) and [Table 8](#) show the hexadecimal OTP binary map template for the CYW4373 USB revision and SDIO revision, respectively.

Table 7. CYW4373 USB Hexadecimal OTP Binary Map Template

Offset	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xa	0xb	0xc	0xd	0xe	0xf
00000000	80	02	00	0b	80	03	02	07	11	80	03	1b	4a	08	00	00
00000010	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000020	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000030	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000040	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000050	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000060	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000070	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000080	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000090	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000a0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000b0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000c0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000d0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000e0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000f0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000100	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000110	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000120	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000130	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000140	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000150	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000160	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

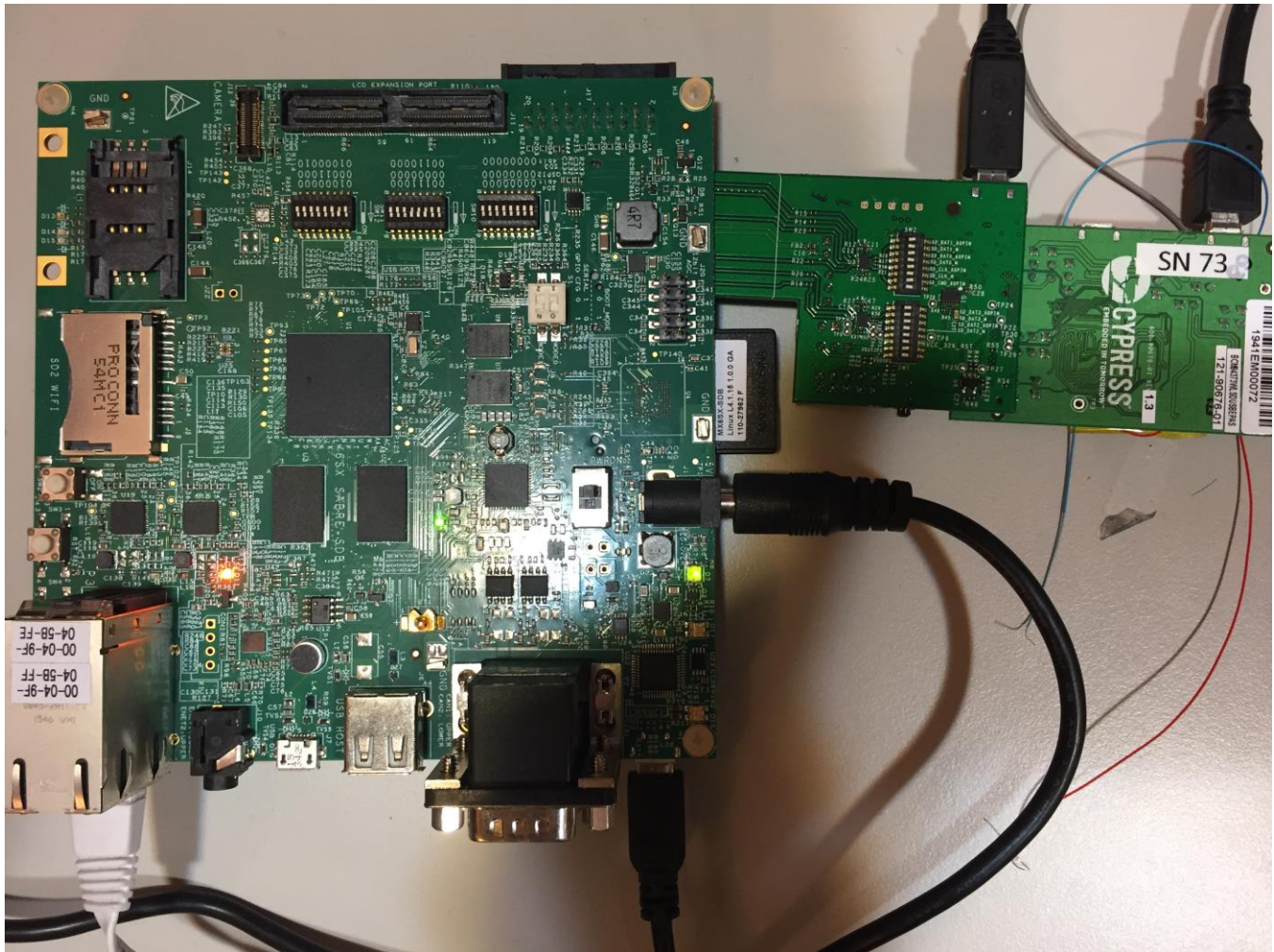
Table 8. CYW4373 SDIO Hexadecimal OTP Binary Map Template

Offset	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xa	0xb	0xc	0xd	0xe	0xf
00000000	5b	00	ff	ff	00	00	20	04	d0	02	73	43	80	07	19	66
00000010	55	44	33	22	11	80	03	02	07	11	80	02	00	0b	80	03
00000020	1b	4a	08	00	00	00	00	00	00	00	00	00	00	00	00	00
00000030	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000040	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000050	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000060	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000070	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000080	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000090	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000a0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000b0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000c0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000d0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000e0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
000000f0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000100	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000110	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000120	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000130	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000140	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000150	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000160	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

## 6 Programming CYW4373 OTP Memory Using iMAX6sx

This section outlines the procedure to program the SDIO header to the OTP of a CYW4373 device using an iMAX6sx FMAC system PC.

Figure 2. iMAX6sx FMAC System Example



The required hardware includes:

- 1x CYW4373 SDIO board – this is the “DUT”
- 1x iMAX6sx system with Cypress image that has FMAC Kernel installed (4.14.0 or later) in SD card
- 1x Ethernet cable
- 1x CYW9SDIOAD\_1 interposer card (inserted into the SD3 slot on iMAX6sx)

The required software includes:

- Cypress SDIO MFG driver package containing driver files for CYW4373 in FMAC (4.14.0) platform (typically provided by Cypress).
- *OTP.bin* file containing the CYW4373 SDIO header information. Follow the procedure in Programming OTP Memory to program OTP memory using the *OTP\_bin* file.

## 6.1 Programming OTP Memory

Use MFG firmware and follow these steps to program the OTP memory:

1. While powered OFF, connect the iMAX6sx to Ethernet.
2. Connect DUT to the 60-pin connector located in the iMAX6sx.
3. Plug in the power to the iMAX6sx and the iMAX6sx system will be turned ON automatically.
4. At prompt, with a specific COM port for iMAX6sx, log in as "root".
5. Copy the CYW4373 driver files and the *OTP.bin* file to a desired directory.
6. Go to the directory where you copied the CYW4373 driver files. Issue the driver load command as you would normally do on a FMAC system, or:

```
> insmod compat.ko
> insmod mmc_core.ko
> modprobe sdhci-pci
> modprobe rfkill
> insmod cfg80211.ko
> insmod brcmutil.ko
> insmod brcmfmac.ko debug=0x100004
> ifconfig wlan0 192.168.1.101 up
> ./wl ver
```

**Note:** If driver loads successfully, the command `wl ver` will return the WL version and the driver version.

7. Once the driver is loaded successfully, you are ready to program OTP.
  - a. Run the following command to check the CIS dump in the OTP:

```
> ./wl cisdump
```

- b. If your CYW4373 device has never been programmed with the SDIO header in the OTP, check if the cisdump is similar to the following:

Source: 2 (Internal OTP)

Maximum length: 368 bytes

```
Byte 0: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 8: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 16: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 24: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 32: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 40: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 48: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 56: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 64: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 72: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 80: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 88: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 96: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 104: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 112: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 120: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 128: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 136: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 144: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 152: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 160: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 168: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 176: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 184: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 192: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 200: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 208: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 216: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 224: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 232: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 240: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 248: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 256: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 264: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 272: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
```

```

Byte 280: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 288: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 296: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 304: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 312: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 320: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 328: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 336: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 344: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 352: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 360: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

```

- c. If you can confirm that CYW4373 device has never been programmed, then your device has blank CIS and is ready to be programmed. Go to the directory where you copied the *OTP.bin* file.

Run the following command:

```
>./wl ciswrite OTP.bin
```

- d. After programming is completed, confirm the OTP by dumping CIS again:

```
>./wl cisdump
```

If programming is successful, you should see the dump that looks similar to the following (for SDIO OTP):

**Note:** Depending on the contents of your *.bin* file, the CIS dump might vary.

```

Source: 2 (Internal OTP)
Maximum length: 368 bytes
Byte 0: 0x5b 0x00 0xff 0xff 0x00 0x00 0x20 0x04
Byte 8: 0xd0 0x02 0x73 0x43 0x80 0x07 0x19 0x66
Byte 16: 0x55 0x44 0x33 0x22 0x11 0x80 0x03 0x02
Byte 24: 0x07 0x11 0x80 0x02 0x00 0x0b 0x80 0x03
Byte 32: 0x1b 0x4a 0x08 0x00 0x00 0x00 0x00 0x00
Byte 40: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 48: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 56: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 64: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 72: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 80: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 88: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 96: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 104: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 112: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 120: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 128: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 136: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

```

```
Byte 144: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 152: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 160: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 168: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 176: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 184: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 192: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 200: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 208: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 216: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 224: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 232: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 240: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 248: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 256: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 264: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 272: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 280: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 288: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 296: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 304: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 312: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 320: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 328: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 336: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 344: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 352: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 360: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
```

If the CIS dump matches your *OTP.bin* file, the OTP programming is successful, and the SDIO header is correctly programmed to your CYW4373 device.

**Note:** Make sure that you remove the device from the USB or SDIO slot before power cycling.



## 7 Programming CYW4373 OTP BD Address

### Command:

```
#./wl otpraw <bitoffset> <length> <value>
```

### Bit offset:

The offset of BD address will change when the OTP patch changes. It is recommended that you follow these steps to calculate the bit offset dynamically:

1. Check the value at 16-bits offset 0x0228. If the value is 0x4f50 (Signature), the OTP contents are valid.
2. Check the value at 8-bits offset 0x022a. If the value is 0xab, it indicates OTP patch.
3. Check the value at 8-bits offset 0x022b. The value indicates the length of OTP patch.
4. Bit offset of OTP BD address = 0x022b + length of OTP patch + 0x01.

For example:

The value at 16-bits offset 0x0228 is 0x4f50.

The value at 8-bits offset 0x022a is 0xab.

The value at 8-bits offset 0x022b is 0x4e.

The bit offset of OTP BD address = 0x022b + 0x4e + 0x01 = 0x027a.

### Length:

"64"

### Value:

10 // Header. Use fixed value of 0x10.

06 // Size of OTP after this byte itself. If you need to program only the BD ADDR, use the size value of 0x06.

ff // BDADDR, 6 bytes; Assuming BD address is 0xaabbccddeeff, and bit offset is 0x027a (= 5072 bits).

ee // BDADDR, 6 bytes.

dd // BDADDR, 6 bytes.

cc // BDADDR, 6 bytes.

bb // BDADDR, 6 bytes.

aa // BDADDR, 6 bytes.

<i>Bit offset:</i>	0x027a	0x027b	0x027c	0x027d	0x027e	0x027f	0x0280	0x0281
<i>Values:</i>	10	06	ff	ee	dd	cc	bb	aa

### Command example:

```
#./wl otpraw 5072 64 0xaabbccddeeff0610
```

## Document History

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Revision	ECN	Submission Date	Description of Change
**	6838397	03/26/2020	New Application Note.
*A	6903281	06/22/2020	Modified SDIO header 0x0 to '5b' from '4b' in the hex value corresponds to - device in SDIO 3.0 mode with Max F2 block size as 256

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