Migrating from S70KL1281/S70KS1281 to S70KL1282/S70KS1282

About this document

Scope and purpose

This application note discusses the key differences that need to be considered when migrating from S70KL1281/S70KS1281 to S70KL1282/S70KS1282. This application note explains how S70KL1282/S70KS1282 is a replacement for S70KL1281/S70KS1281.

Intended audience

This document is primarily intended for anyone who wants to migrate from S70KL1281/S70KS1281 to S70KL1282/S70KS1282.

Associated part family

S70KL1281/S70KS1281, S70KL1282/S70KS1282

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1 Introduction

S70KL1282/S70KS1282, a 128-Mbit HYPERRAM™, is a replacement device for S70KL1281/S70KS1281. For all designs, S70KL1282/S70KS1282 can be considered as a superset of S70KL1281/S70KS1281. The two devices are pin-to-pin compatible and identical in terms of package composition and dimensions and read/write functionality. This application note discusses the key differences between the two devices that need to be considered when migrating from S70KL1281/S70KS1281 to S70KL1282/S70KS1282.

2 Drop-in replacement or not?

From a hardware point of view, no PCB modification is required. From a software point of view, the key difference between the two devices are configuration register 1 and device ID. See **Critical considerations** for more details.

S70KL1282/S70KS1282 adds many features like deep power down (DPD) capability, lower standby current, and higher speed capability. **Table 1** shows the compatibility chart of S70KL1281/S70KS1281 and S70KL1282/S70KS1282. For a detailed comparison, see **Table 4**.

Table 1 Compatibility chart

S70KL1281/S70KS1281 feature or spec	S70KL1282/S70KS1282 compatible?
Package	Yes
Pinout	Yes
Temperature range	Yes
Operating voltage	Yes
Operating current	Yes
Standby current	Yes
Read/write function	Yes
Timing/frequency	Yes
Default ID and CR settings	No

3 Ordering part numbers

Table 2 lists the recommended S70KL1282/S70KS1282 ordering part numbers (OPN) that correspond to S70KL1281/S70KS1281 ordering part numbers.

Table 2 Recommended ordering part numbers for migration

S70KL1281/S70KS1281		S70KL1282/S70KS1282		Comments
OPN	**Status**	**OPN**	**Status**	
S70KS1281	Not recommended for new designs	S70KS1282	In production	No hardware change required. Both devices are pin-to-pin compatible.
S70KL1281	Not recommended for new designs	S70KL1282	In production	No hardware change required. Both devices are pin-to-pin compatible.

4 Detailed comparison of S70KL1281 and S70KL1282

Table 3 Detailed comparison

	S70KL1281	S70KL1282	Comments
Pinout/package outline	24-ball FBGA	24-ball FBGA	Identical
Temperature range	–40°C to +85°C	–40°C to +85°C	Identical
Operating voltage range	2.7 V to 3.6 V	2.7 V to 3.6 V	Identical
DC characteristics	**Table 9** shows the detailed comparison of DC parameters.		
AC characteristics	**Table 11** shows the detailed comparison of AC characteristics.		
Standby current (ICC4I)	400 µA @ 85 °C	500 µA @ 85 °C	S70KL1282 has a higher standby current.
DPD current	–	250 µA	S70KL1282 has a lower DPD current.
Hybrid sleep current	–	480 µA	New feature/spec in the S70KL1282 device. Not supported in the previous generation device.
CS# HIGH to enter hybrid sleep (t_{HSIN})	–	3 µs	New feature/spec in the S70KL1282 device. Not supported in the previous generation device.
Differential clock	Not applicable at V_{CC} = 3 V	Applicable for all operating voltage ranges	CK# of S70KL1282 can be left floating if not used.
Die manufacture information	–	36-byte die manufacture information available	This information can be read as a register with an address offset of 0x1800. New feature/spec in the S70KL1282 device. Not supported in the previous generation device.
Clock frequency (Max)	100 MHz	200 MHz	Higher speed offered in S70KL1282. For timing comparison, see **Table 12**.
Default latency	6 clock cycles	7 clock cycles	Critical difference. See **Latency cycles**.
Configuration register 1	This register is used to configure the distributed refresh interval only.	This register is used to configure the distributed refresh interval along with some other user configuration options.	See **Table 8**
V_{DD} minimum and RESET# HIGH to first access (t_{VCS})	150 µs/V	150 µs/V	Identical

Detailed comparison of S70KL1281 and S70KL1282

	S70KL1281	S70KL1282	Comments
Power down period for part to initialize correctly (t_{PD})	50	50	Identical
V_{DD} required to ensure initialization (V_{RST})	0.8	0.7	S70KL1282 offers a lower V_{RST}.
V_{DD} lock-out below which require initialization (V_{LKO})	2.7	2.4	S70KL1282 offers a lower V_{LKO}.
V_{DD} power-down ramp rate (t_{VF})	50 µs / V	50 µs / V	Identical
Reset pulse width (t_{RP})	200 ns	200 ns	Identical
Time between RESET# HIGH and CS# LOW (t_{RH})	200 ns	200 ns	Identical
Time between RESET# LOW to CS# LOW (t_{RPH})	400 ns	400 ns	Identical
Device ID0	Die 0: 0x0C81 Die 1: 0x4C81	Die 0: 0x0C81 Die 1: 0x4C81	Identical
Device ID1	0x0000	0x0001	Critical difference. See **Device ID**.

5 Detailed comparison of S70KS1281 and S70KS1282

Table 4 Detailed comparison

	S70KS1281	S70KS1282	Comments
Pinout/package outline	24-ball FBGA	24-ball FBGA	Identical
Temperature range	–40 °C to +85 °C	–40 °C to +85 °C	Identical
Operating voltage range	1.7 V to 1.95 V	1.7 V to 2.0 V	S70KS1282 offers wide operating range.
DC characteristics	**Table 10** shows the detailed comparison of DC parameters.		
AC characteristics	**Table 12** shows the detailed comparison of AC characteristics.		
Standby current	400 µA @ 85 °C	440 µA @ 85 °C	S70KS1282 has a higher standby current.
DPD current	–	220 µA	Identical
Hybrid sleep current	–	420 µA	New feature/spec in the S70KS1282 device. Not supported in the previous generation device.
Differential clock (CK#)	Differential clock is required	Differential clock is optional	CK# of S70KS1282 can be left floating if not used.
CS# HIGH to enter hybrid sleep (t_{HSIN})	–	3 µs	New feature/spec in the S70KS1282 device. Not supported in the previous generation device.
Die manufacture information	–	36 bytes die manufacture information available	This information can be read as a register with an address offset of 0x1800. New feature/spec in the S70KL1282 device. Not supported by the earlier generation device.
Clock frequency (Max)	166 MHz	200 MHz	Higher speed offered in S70KS1282. For timing comparison, see **Table 12**.
Default latency	6 clock cycles	7 clock cycles	Critical difference. See **Latency cycles**.
Configuration register 1	This register is used to configure the distributed refresh interval only.	This register is used to configure the distributed refresh interval along with some other user configuration options.	See **Table 8**
V_{DD} minimum and RESET# HIGH to first access (t_{VCS})	150 µs / V	150 µs / V	Identical
Power down period for part to initialize correctly (t_{PD})	50	50	Identical

Detailed comparison of S70KS1281 and S70KS1282

	S70KS1281	S70KS1282	Comments
V_{DD} required to ensure initialization (V_{RST})	0.8	0.7	S70KS1282 offers a lower V_{RST}.
V_{DD} lock-out below which require initialization (V_{LKO})	1.7	1.5	S70KS1282 offers a lower V_{LKO}.
V_{DD} power-down ramp rate (t_{VF})	50 µs / V	50 µs / V	Identical
Reset pulse width (t_{RP})	200 ns	200 ns	Identical
Time between RESET# HIGH and CS# LOW (t_{RH})	200 ns	200 ns	Identical
Time between RESET# LOW to CS# LOW (t_{RPH})	400 ns	400 ns	Identical
Device ID0	Die 0: 0x0C81 Die 1: 0x4C81	Die 0: 0x0C81 Die 1: 0x4C81	Identical
Device ID1	0x0000	0x0001	Critical difference. See **Device ID**.

6 Critical considerations

You must consider all parameter differences mentioned in **Table 3** and **Table 4** while migrating to S70KL1282/S70KS1282. This section discusses the critical differences between S70KL1281/S70KS1281 and S70KL1282/S70KS1282. System designers should also review the datasheet when migrating to the new part.

6.1 Device ID (ID0 and ID1)

S70KL1281/S70KS1281 and S70KL1282/S70KS1282 incorporate a two, double-word (4-byte), read-only Device ID to identify the product uniquely. Device ID allows the host to determine the manufacturer, product density, and product type. **Table 5** gives the Device IDs of S70KL1281/S70KS1281 and S70KL1282/S70KS1282, where the difference is highlighted in bold.

Table 5 Device ID

	S70KL1281/S70KS12821	**S70KL1282/S70KS1282**
Device ID 0	Die 0: 0x0C81 Die 1: 0x4C81	Die 0: 0x0C81 Die 1: 0x4C81
Device ID 1	0x0000	0x00**01**

6.2 Deep power down

S70KL1282/S70KS1282 uses the MSB of CR0 register (CR0[15]) to enter the DPD mode. In S70KL1281/S70KS1281, this bit is not used. Migrating to S70KL1282/S70KS1282 requires a firmware check to avoid an unintended entry into DPD mode.

Table 6 Comparing CR0[15]

CR0 bit	**S70KL1281/S70KS1281**	**S70KL1282/S70KS1282**	**Comments**
[15]	Reserved for Future Use	1b (default): Normal operation 0b: DPD mode enabled	DPD functionality enabled in S70KL1282/S70KS1282.

6.3 Latency cycles

Configuration register 0 (CR0) is used to set latency cycles. S70KL1281/S70KS1281 has a latency setting of six clocks by default, while S70KL1282/S70KS1282 has a latency setting of seven clocks by default. Migrating to S70KL1282/S70KS1282 requires a firmware update to take care of the additional one clock cycle, if using the default latency settings.

Table 7 Comparing CR0

CR0 bit	**S70KL1281/S70KS1281**	**S70KL1282/S70KS1282**	**Comments**
[7:4]	0001b -- 6 clock latency (default)	0010b: 7 clock latency (default)	Default value is different.

6.4 Configuration register 1

In S70KL1281/S70KS1281, configuration register 1 (CR1) is used to define the distributed refresh interval for this HYPERRAM™ device. A few additional features are added in S70KL1282/S70KS1282, which are configurable through CR1 of S70KL1282/S70KS1282. **Table 8** compares CR1 of S70KL1281/S70KS1281 and S70KL1282/S70KS1282.

Table 8 Comparing CR1

CR1 bit	S70KL1281/S70KS1281	S70KL1282/S70KS1282	Comments
[15:8]	0x00 (default)	0xFF (default)	Not used, but the default value is different.
[7]	0 (default)	1 (default)	
[6]	0 (default)	Master clock type: 1 = Single ended (default) 0 = Differential	Default value in S70KX1281 configures S70KX1282 in differential clock mode. However, even if the differential clock in S70KX1282 is enabled, toggling of CK# is optional. Make sure CK# input remains static (either HIGH or LOW), but not floating to prevent it from picking unnecessary noise.
[5]	0 (default)	Hybrid sleep: 0 = normal operation (default) 1 = enter hybrid sleep	In S70KX1282, use this bit to enter hybrid sleep. Retain the default if the feature is not used.
[4:2]	000b (default)	Partial array refresh: 000b = Full array (default)	In S70KX1282, use these bits to restrict the refresh operation to a portion of the memory.
[1:0]	Distributed refresh interval 10b – 4 µs (default) 11b – 1.5 times default 00b – 2 times default 01b – 4 times default	Distributed refresh interval 10b = 1 µs (only applicable for industrial plus (105 °C) devices) 11b = Reserved 00b = Reserved 01b = 4 µs	For S70KX1282, CR[1:0] are read-only bits determined and configured by the device internally based on its refresh interval variation across the Process, Voltage, Temperature (PVT) corners. You can probe these two bits prior to every HYPERRAM™ access (write or read) to determine whether refresh interval should be 10b (1 µs) or 01b (4 µs) for the current cycle and set the t_{CSM} for the host controller accordingly. Alternatively, if the host controller does not want to access CR1 prior to every memory access, it can set t_{CSM} to 4 µs (fixed), as per datasheet recommendations at 85 °C.

6.5 DC characteristics (S70KL1281 and S70KL1282)

Table 9 compares the DC parameters of S70KL1281 with S70KL1282. S70KL1282 has some higher DC characteristic values; you should consider these differences in DC characteristics at the system level for a proper migration.

Table 9 Comparing DC characteristics

Parameter	Description	Test condition	S70KL1281		S70KL1282		Unit
			Typ	Max	Typ	Max	
I_{LI4}	Input leakage current 3.3 V device reset signal low only	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	+40	–	+15	µA
I_{CC1}	V_{CC} active read current	CS# = V_{IL}, V_{CC} = 3.6 V	32	47	30	60	mA
I_{CC2}	V_{CC} active write current	CS# = V_{IL}, V_{CC} = 3.6 V	27	47	30	60	mA
I_{CC4I}	V_{CC} standby current	CS# = V_{IL}, V_{CC} = 3.6 V	286	400	180	500	µA
I_{CC5}	Reset current	CS# = V_{IH}, RESET# = V_{IL}, V_{CC} = V_{CC} max	–	40	–	1.5	mA
I_{CC6I}	Active clock stop current	CS# = V_{IH}, RESET# = V_{IL}, V_{CC} = V_{CC} max	11	16	10	13	mA
I_{CC7}	Vcc current during power up	CS# = V_{IH}, V_{CC} = V_{CC} max, V_{CC} = V_{CCQ} = 3.6V	–	70	–	70	mA
I_{DPD}	Deep power down current	CS# = V_{IH}, V_{CC} = V_{CC} max, V_{CC} = V_{CCQ} = 3.6 V	–	–	–	250	µA
I_{HS}	Hybrid sleep current	CS# = V_{IH}, VCC = V_{CC} max, V_{CC} = V_{CCQ} = 2.0 V	–	–	115	480	µA

6.6 DC characteristics (S70KS1281 and S70KS1282)

Table 10 compares the DC parameters of S70KS1281 with S70KS1282. S70KS1282 has some higher DC characteristic values; you should consider these differences in the DC characteristics at the system level for a proper migration.

Table 10 Comparing DC characteristics

Parameter	Description	Test condition	S70KS1281		S70KS1282		Unit
			Typ	Max	Typ	Max	
I_{LI4}	Input leakage current 1.8 V device reset signal LOW only	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	+40	–	+15	µA
I_{CC1}	V_{CC} active read current	CS# = V_{IL}, @200 MHz, V_{CC} = 2.0 V	29	72	30	50	mA
I_{CC2}	V_{CC} active write current	CS# = V_{IL}, @200 MHz, V_{CC} = 2.0 V	23	72	30	50	mA
I_{CC4I}	V_{CC} standby current	CS# = V_{IL}, @200 MHz, V_{CC} = 2.0 V	286	400	160	440	µA
I_{CC5}	Reset current	CS# = V_{IH}, RESET# = V_{IL}, V_{CC} = V_{CC} max	–	40	–	1.5	mA
I_{CC6I}	Active clock stop current	CS# = V_{IH}, RESET# = V_{IL}, V_{CC} = V_{CC} max	11	16	10	13	mA

Critical considerations

Parameter	Description	Test condition	S70KS1281		S70KS1282		Unit
			Typ	Max	Typ	Max	
I_{CC7}	Vcc current during power up	CS# = V_{IH}, V_{CC} = V_{CC} max, V_{CC} = V_{CCQ} = 2.0V	–	70	–	70	mA
I_{DPD}	Deep power down current	CS# = V_{IH}, V_{CC} = V_{CC} max, V_{CC} = V_{CCQ} = 2.0 V	–	–	–	220	µA
I_{HS}	Hybrid sleep current	CS# = V_{IH}, V_{CC} = V_{CC} max, V_{CC} = V_{CCQ} = 2.0 V	–	–	105	420	µA

6.7 AC characteristics (S70KL1281 and S70KL1282)

Table 11 compares the AC parameters of S70KL1281 with S70KL1282. Migrating to S70KL1282 requires no timing adjustment at system level due to its improved AC characteristics values.

Table 11 Comparing timing parameters

Parameter	Symbol	S70KL1281 (100 MHz)		S70KL1282 (166 MHz)		S70KL1282 (200 MHz)		Unit
		Min	Max	Min	Max	Min	Max	
Chip select HIGH between transactions	t_{CSHI}	10		6	–	6	–	ns
HYPERRAM™ read-write recovery time	t_{RWR}	40		36	–	35	–	ns
Chip select setup to next CK rising edge	t_{CSS}	3		3	–	4	–	ns
Data strobe valid	t_{DSV}	–	12	-	12	–	6.5	ns
Input setup	t_{IS}	1		0.6	–	0.5	–	ns
Input hold	t_{IH}	1		0.6	–	0.5	–	ns
HYPERRAM™ read initial access time	t_{ACC}	40		36	–	35	–	ns
Clock to DQs low Z	t_{DQLZ}	0		0	–	0	–	ns
CK transition to DQ valid (128 Mb)	t_{CKD}	–	7	–	7	–	6.5	ns
CK transition to DQ invalid (128 Mb)	t_{CKDI}	–	5.2	–	5.6	–	5.7	ns
Data valid (t_{DV} min = the lessor of: t_{CKHP} min - t_{CKD} max + t_{CKDI} max) or t_{CKHP} min - t_{CKD} min + t_{CKDI} min)	t_{DV}	2.7		1.3	-	1.45	–	ns
CK transition to RWDS valid (128 Mb)	t_{CKDS}	1	7	1	7	–	6.5	ns
RWDS transition to DQ valid	t_{DSS}	–	0.8	-	0.8	–	0.4	ns
RWDS transition to DQ invalid	t_{DSH}	–	0.8	-	0.8	–	0.4	ns
Chip select hold after CK falling edge	t_{CSH}	0		0	-	0	-	ns
Chip select inactive to RWDS High-Z	t_{DSZ}	–	7	-	7	–	6.5	ns
Chip select inactive to DQ High-Z	t_{OZ}	–	7	-	7	–	6.5	ns
HYPERRAM™ chip select maximum low time (85 °C)	t_{CSM}	–	4	-	4	–	4	µs
Refresh time	t_{RFH}	40	–	36	–	35	–	ns
HYPERBUS™ CK transition to RWDS LOW @CA phase @read (128 Mb)	t_{CKDSR}	–	–	1	7	1	7	ns

6.8 AC characteristics (S70KS1281 and S70KS1282)

Table 12 compares the AC parameters of S70KS1281 with S70KS1282. Migrating to S70KS1282 requires no timing adjustment at system level due to its improved AC characteristics values except t_{CSS} timing parameter. You must modify the system-level timing to meet the t_{CCS} timing requirement.

Table 12 Comparing timing parameters

Parameter	Symbol	S70KS1281 (166 MHz)		S70KS1282 (200 MHz)		Unit
		Min	Max	Min	Max	
Chip select HIGH between transactions	t_{CSHI}	6	–	6	–	ns
HYPERRAM™ read-write recovery time	t_{RWR}	36	–	35	–	ns
Chip select setup to next CK rising edge	t_{CSS}	3		4	–	ns
Data strobe valid	t_{DSV}	–	12	-	5	ns
Input setup	t_{IS}	0.6		0.5	–	ns
Input hold	t_{IH}	0.6		0.5	–	ns
HYPERRAM™ read initial access time	t_{ACC}	36		35	–	ns
Clock to DQs Low Z	t_{DQLZ}	0		0	–	ns
CK transition to DQ valid (128 Mb)	t_{CKD}	–	5.5	–	5	ns
CK transition to DQ invalid (128 Mb)	t_{CKDI}	–	4.6	–	4.2	ns
Data valid (t_{DV} min = the lessor of: t_{CKHP} min - t_{CKD} max + t_{CKDI} max) or t_{CKHP} min - t_{CKD} min + t_{CKDI} min)	t_{DV}	1.7	–	1.45	–	ns
CK transition to RWDS valid (128 Mb)	t_{CKDS}	1	5.5	1	5	ns
RWDS transition to DQ valid	t_{DSS}	–	0.45	-	0.4	ns
RWDS transition to DQ invalid	t_{DSH}	–	0.45	-	0.4	ns
Chip select hold After CK falling edge	t_{CSH}	0	–	0	–	ns
Chip select inactive to RWDS High-Z	t_{DSZ}	–	6	–	5	ns
Chip select inactive to DQ High-Z	t_{OZ}	–	6	–	5	ns
HYPERRAM™ chip select maximum low time (85 °C)	t_{CSM}	–	4	–	4	µs
Refresh time	t_{RFH}	36	–	35	–	ns
HYPERBUS™ CK transition to RWDS low @CA phase @read (128 Mb)	t_{CKDSR}	–	–	1	5.5	ns

References

[1] **S70KL1281/S70KS1281, 3.0 V/1.8 V, 64 Mb (8 MB)/128 Mb (16 MB), HYPERRAM™ self-refresh DRAM**

[2] **S70KL1282/S70KS1282, 3.0 V/1.8 V, 128 Mb (16 MB), HYPERRAM™ self-refresh DRAM**

[3] **HYPERBUS™ specification low signal count, high performance DDR bus**

Revision history

Document version	Date of release	Description of changes
**	2020-03-10	New application note.
*A	2021-09-21	Migrated to Infineon template.

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