Enabling Infineon QSPI Flash to Configure Intel Cyclone 10 GX FPGA

About this document

Scope and purpose

This application note describes how to enable Infineon S25HS512T QSPI Flash for configuring Intel Cyclone 10 GX FPGA under Active Serial (AS) mode by using the Intel Quartus Prime Pro Generic Flash Programmer tool. The same method also applies to enable other Infineon QSPI Flash families by configuring the flash according to the respective flash datasheet.

Intended audience

This is intended for customers who use Infineon QSPI flash memory as configuration device for the Intel Cyclone 10 GX FPGA.

Table of contents

1 Introduction

The document is written assuming the reader is familiar with Intel FPGA development.

Intel's Generic Flash Programmer tool in Quartus Prime 19.1 and later versions provides a way to configure third-party QSPI flash as a FPGA Configuration Device.

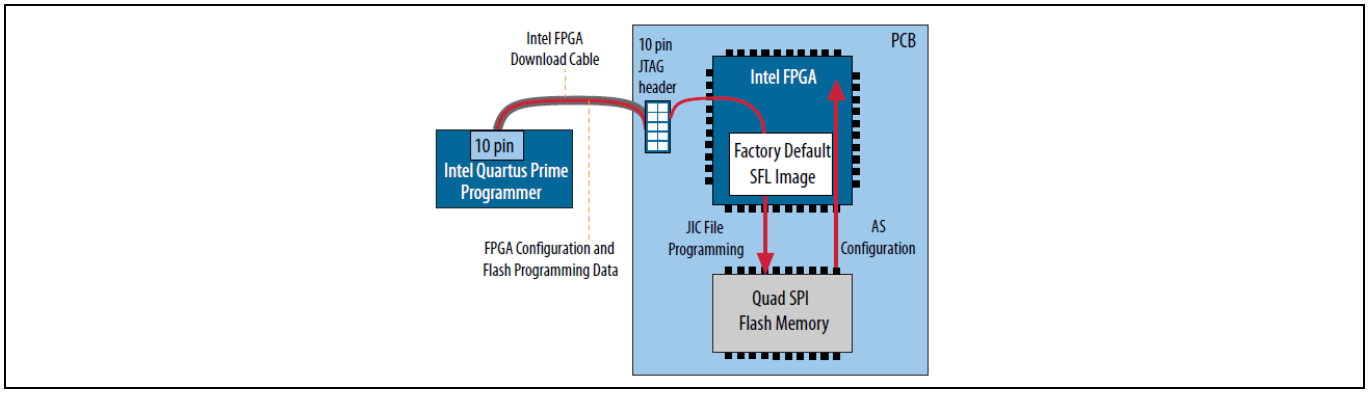
This application note describes how to use the Generic Flash Programmer tool to load an FPGA configuration bitstream file into Infineon S25HS512T QSPI flash. The Infineon QSPI flash subsequently loads the configuration data into the target FPGA via Active Serial (AS) configuration.

The procedures introduced in this application note were verified on the Intel Cyclone 10 GX FPGA Development Kit with Infineon SEMPER Flash with Quad SPI Interface – specifically the S25HS512T – by using Quartus Prime Pro 19.2. The procedures are expected to apply to all other Quartus Prime version 19.1 and later. The procedures should also apply to other Infineon QSPI Flash families and Intel Arria 10 FPGA devices by configuring the flash and FPGA device according to the respective datasheet.

2 Background Information

The Intel Generic Flash Programmer supports Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX FPGA devices. However, for Intel Stratix 10 devices, the Secure Device Manager (SDM) firmware controls the flash programming flows; you cannot modify these flows. Thus, the procedure introduced in this application note does not apply to Intel Stratix 10 FPGA devices.

The following diagram shows the Generic Flash Programmer Configuration data flows in red.



3 Procedures

You can access settings and controls for the Generic Flash Programmer from the Quartus Prime **Programmer**, **Convert Programming File** dialog box.

Generic Flash Programming with the Convert Programming File dialog box includes the following high-level steps:

1. Generate *.sof FPGA configuration file.
2. Define a new Configuration Device
3. Convert *.sof file to *.jic file which is used to program Infineon QSPI flash to store the configuration data.
4. Use the Intel Quartus Prime Programmer and connect the Intel FPGA download cable to program the *.jic configuration data into the Infineon QSPI flash device.

3.1 Generate *.sof FPGA configuration file

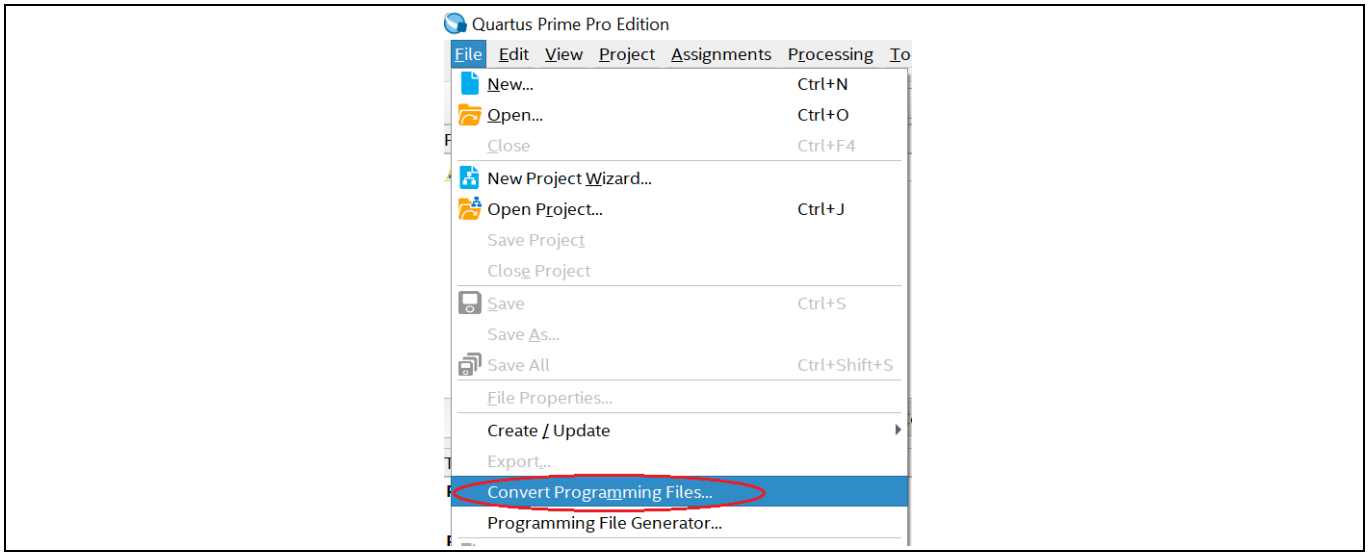
This step is NOT covered in this document. It assumes you have a *.sof file already generated. See relevant Intel documents for generating *.sof files.

3.2 Define the new Configuration Device

While defining the new Configuration Device, the Quartus Prime software stores the collection of settings in an *.xml file in the **Device database directory** location of your choice. This configuration only needs to be done once; the new Configuration Device template can be reused just as the default Configuration Device templates listed in the Quartus Prime.

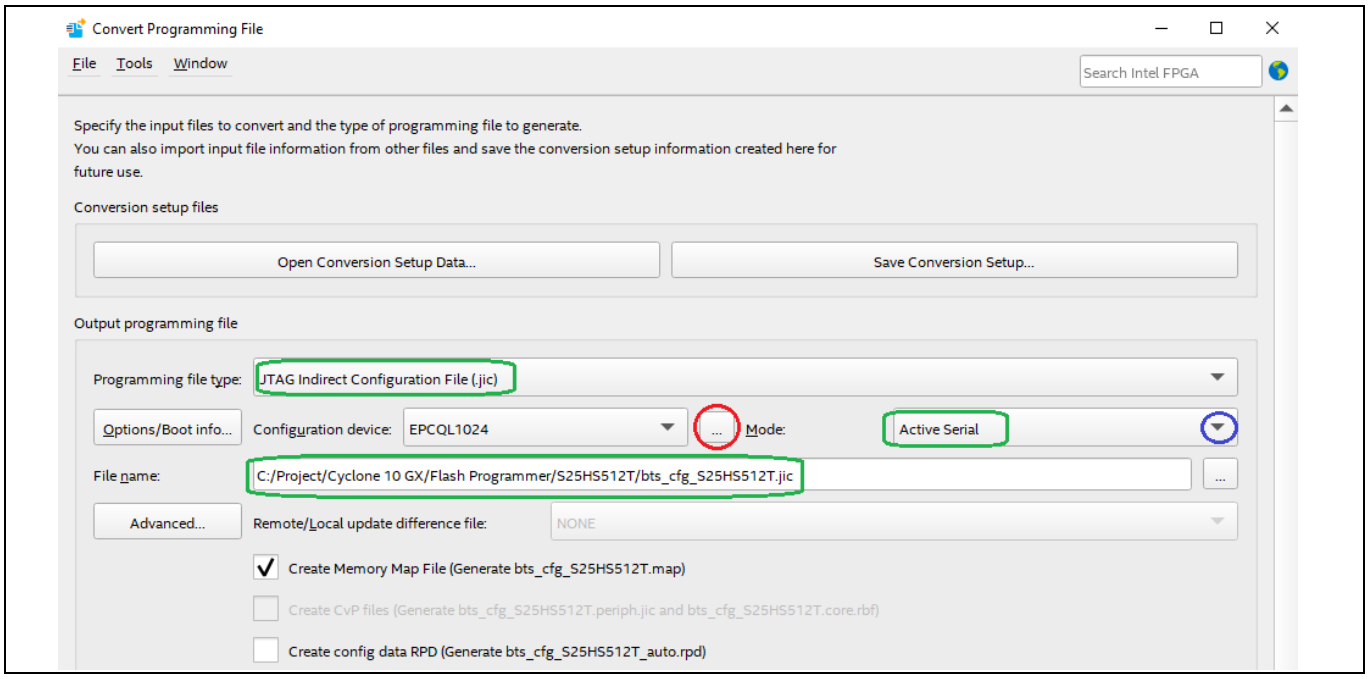
3.2.1 Add the new Configuration Device

1. Open Quartus Prime Pro software, and select **File** > **Convert Programming Files…**.



Procedures

2. Do the following in the **Convert Programming File** screen:



a) Select the *.jic file type in Programming file type.

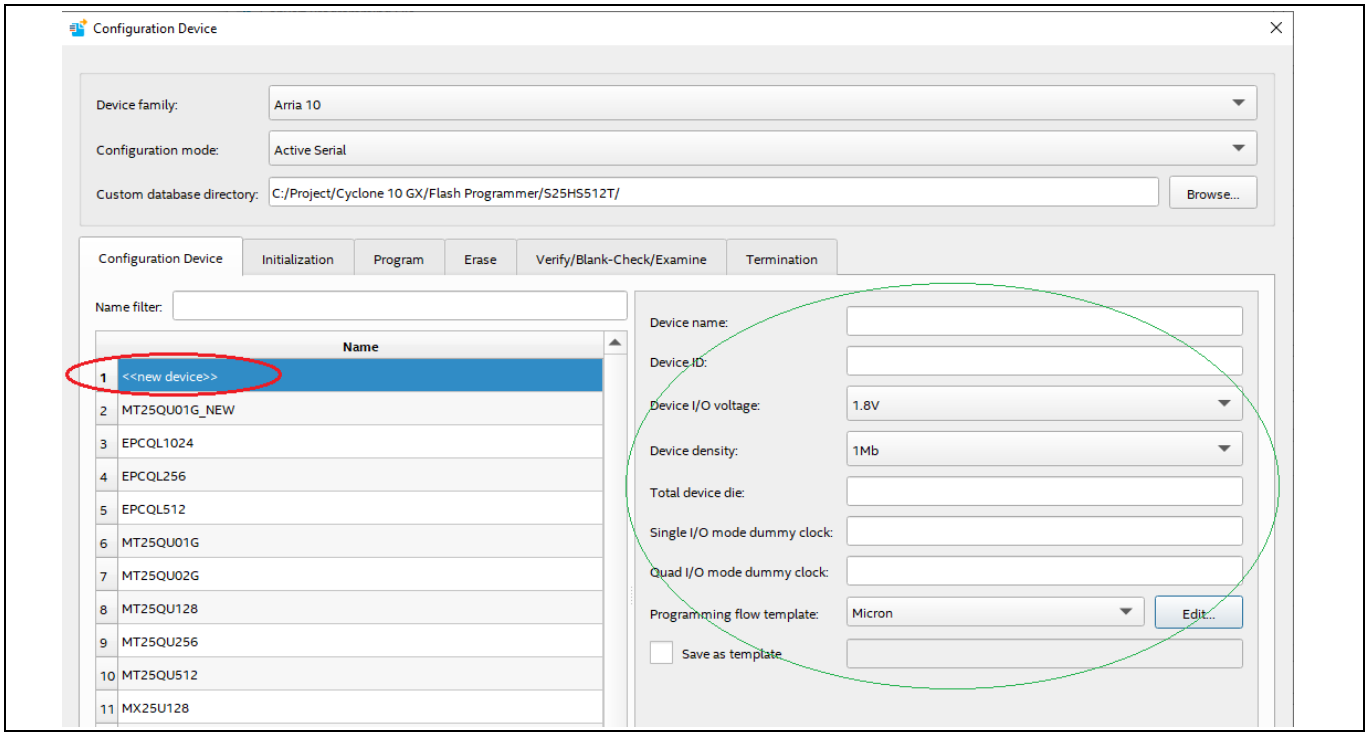
*Note: You can select the Mode option only if *.jic is selected.*

b) In the File name field, specify the location to store the converted *.jic file.

c) Click the pull-down menu in the blue circle, and select **Active Serial**.

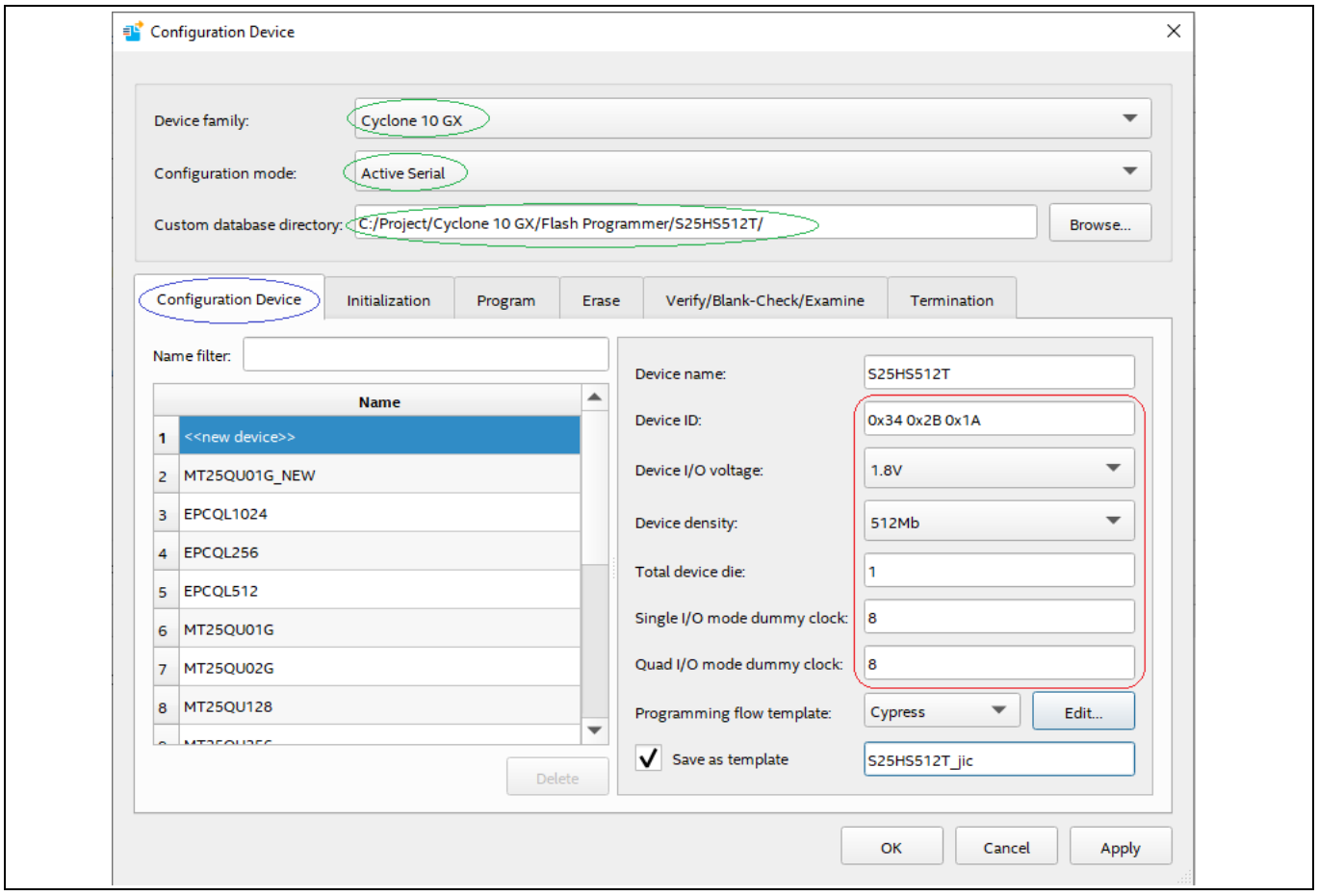
d) Click in the red circle.

3. Click **<<new device>>**. Configurable fields in the green circle appear.



Procedures

4. Make the following changes:



- Configure the FPGA **Device family** and **Configuration mode** according to the FPGA device.
- Specify the **Custom database directory** where the *.xml file will be stored.
- Configure the flash device parameters according to the QSPI Flash device datasheet:
  - Device ID
  - Device I/O voltage
  - Device density
  - Total device die
  - Single I/O mode dummy clock
  - Quad I/O mode dummy clock

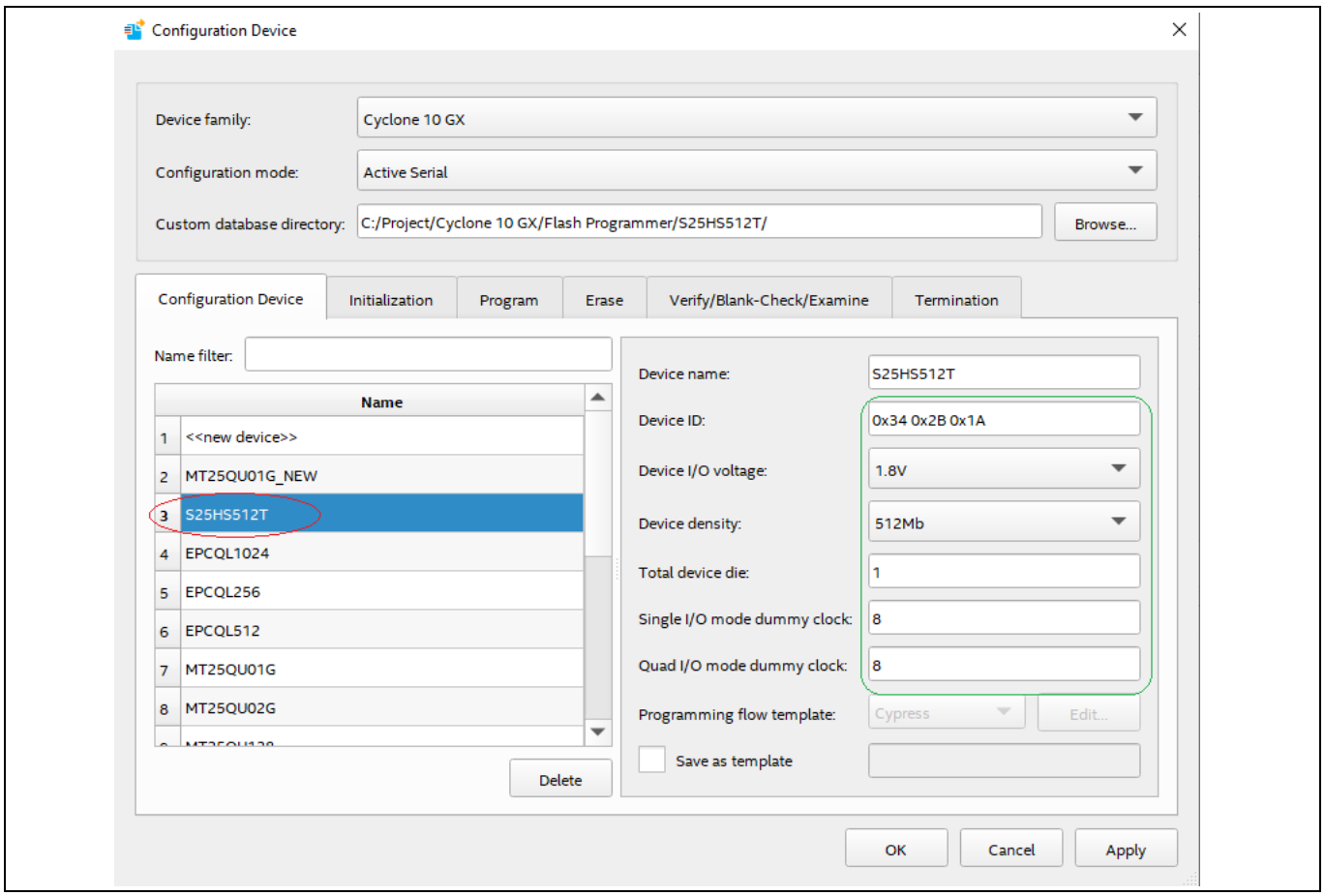
  For example, for the S25HS512T device, enter these parameters from the S25HS512T datasheet.

5. Click **Apply**. The new device “S25HS512T” is automatically added in the list on the left.

Note:

- In the flash parameter configuration, **Device name** and template name (“Save as template”) cannot be the same. Otherwise, an error message “Template name xxxxxx conflicts with the device name xxxxxx” appears when you click the **Apply** button.
- The **Device ID** is a 3-byte hex data in the format 0xAB 0xCD 0xEF.

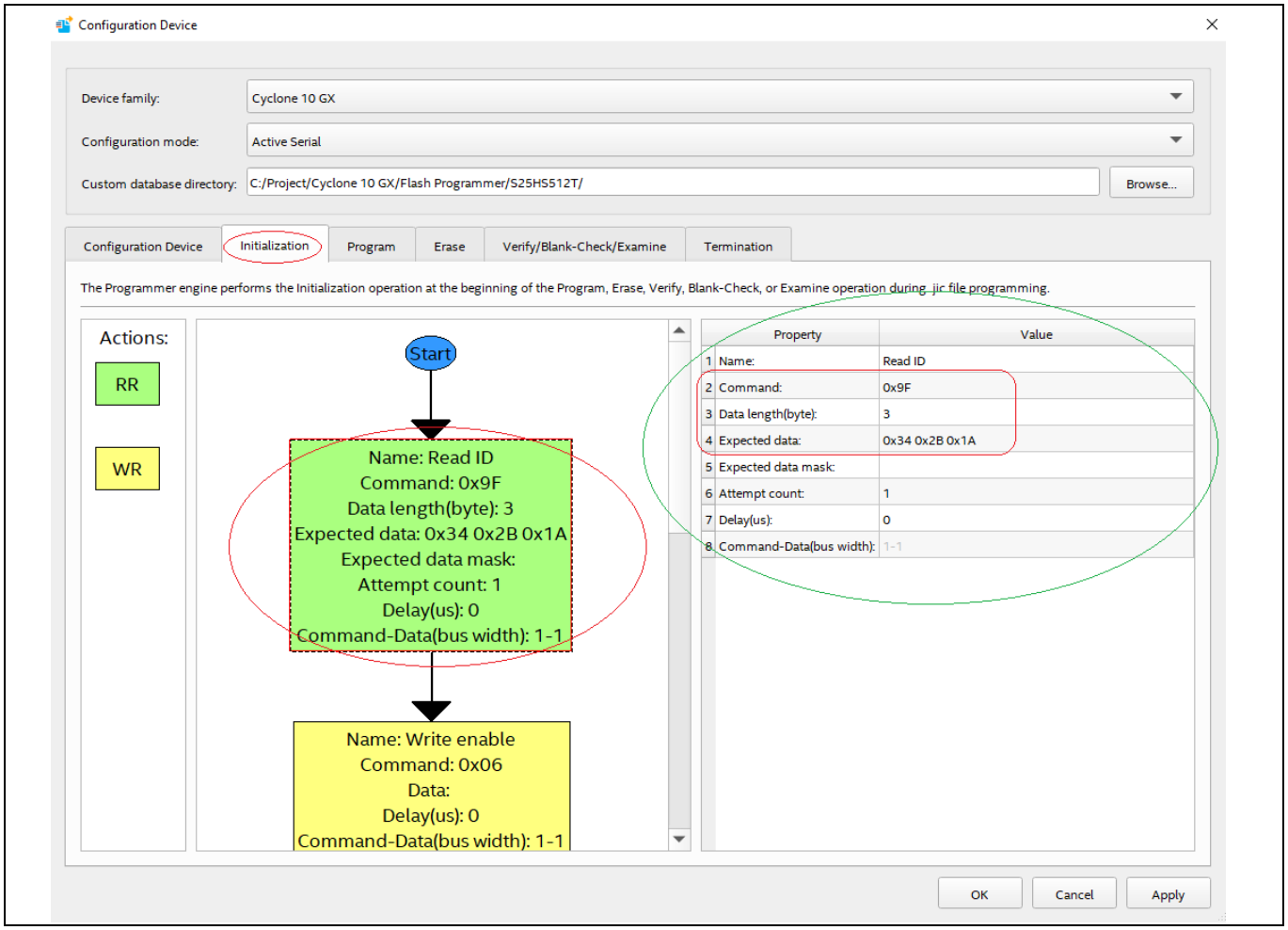
3.2.2 Modify Initialization Flow Template



1. Select the Configuration Device that you created (i.e., S25HS512T), and then click the **Initialization** tab.

   The Initialization tab shows the flash initialization flow template. You can add, delete, or modify an action in the template. This shows the changes for the S25HS512T device based on the default flow template. You can define your own initialization flow template if required.

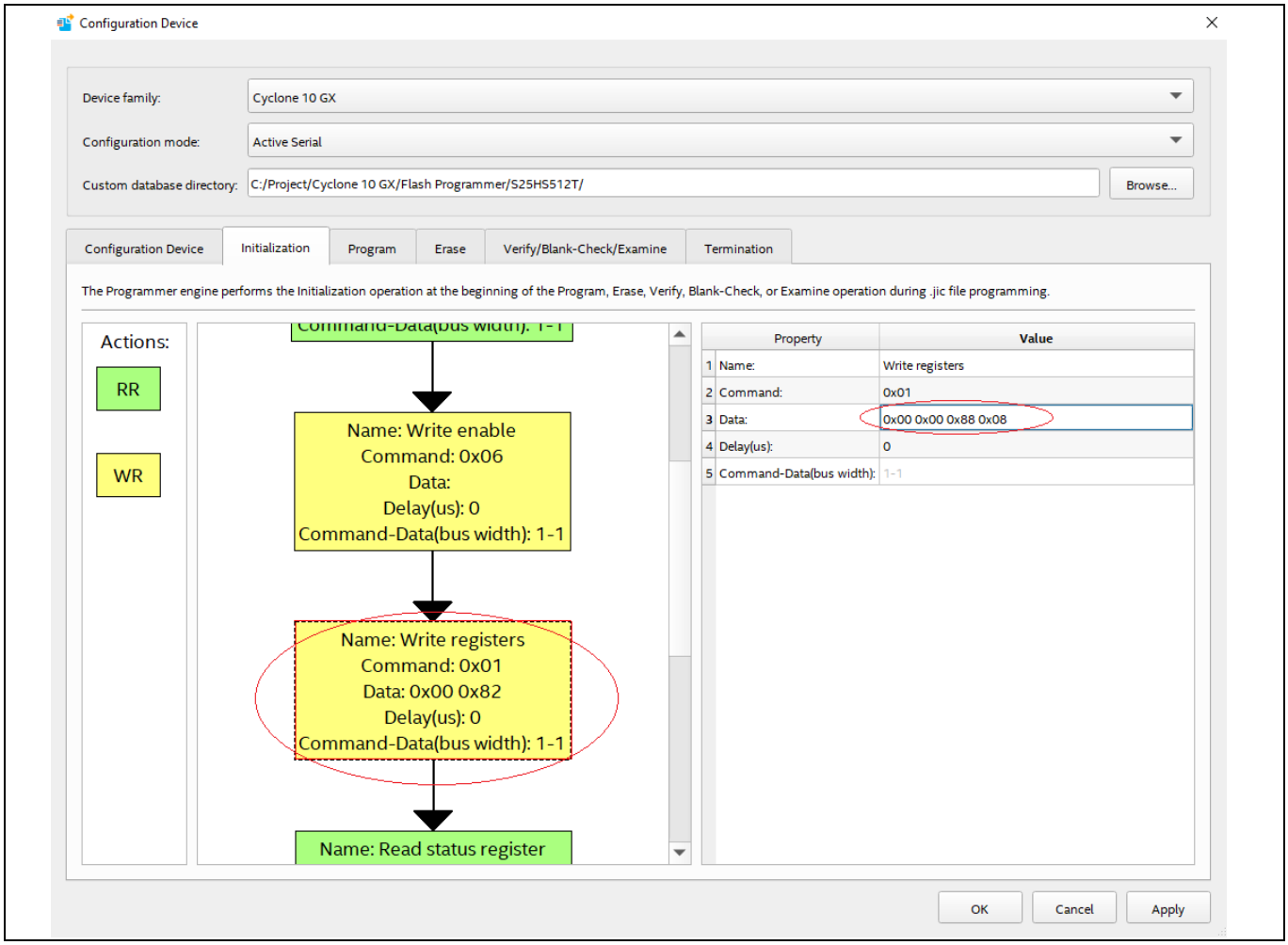
Procedures



2. Click the **Read ID** action in the left pane. Configure the properties on the right (in green circle) according to the flash device datasheet.
3. Click **Apply** after action properties are configured.

   The default “Write enable” action is the same as that of S25HS512T; this field is not modified for this example.

Procedures



4. Scroll down the left window, and then click the **Write registers** action. Edit the properties to configure the flash register.

   In this example, configure the S25HS512T to 4-byte address mode, and set the sector architecture as uniform 256KB.

   The S25HS512T Write Register command sequence is: Write Register Command (0x01) + STR1 (Status Register-1) value + CFR1 (Configuration Register-1) value + CFR2 (Configuration Register-2) value + CFR3 (Configuration Register-3) value.

   The STR1 default value is 0x00; CFR1 default is 0x00.

   The CFR2 default value is 0x08. Set CFR2[7] to '1' for 4-byte address mode. The new value for CFR2 is 0x88.

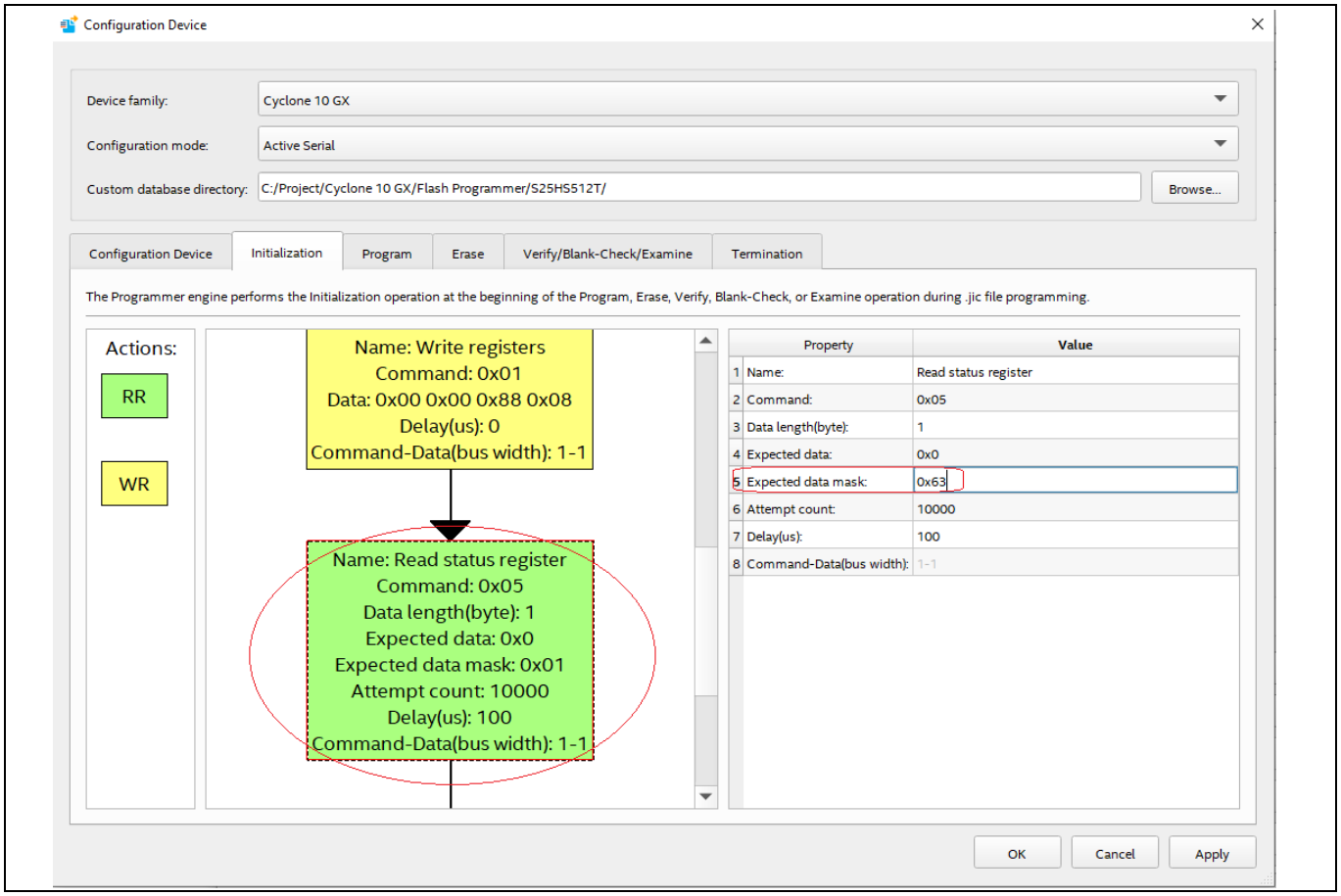
   The CFR3 default value is 0x00 (Hybrid Sector Architecture 4KB + 256KB sectors). Set CFR3[3] to '1' for uniform 256KB sector. The new value for CFR3 is 0x08.

   Thus, the data that follows the 0x01 command is 0x00 0x00 0x88 0x08 (as shown in above screenshot in the red circle on the right side). See the S25HS512T datasheet for register details.

Procedures

Note:

- Intel Cyclone 10 GX and Arria 10 devices require 4-byte addressing flash memory; the flash must support 4-byte addressing and should be configured to 4-byte address mode.
- The default erase flow template is for uniform 256KB sector architecture. To simplify the erase flow, set the flash as uniform 256KB sector architecture in the initialization flow. If not, the erase flow will not be able to completely erase the flash array; note that this may happen without an error message.

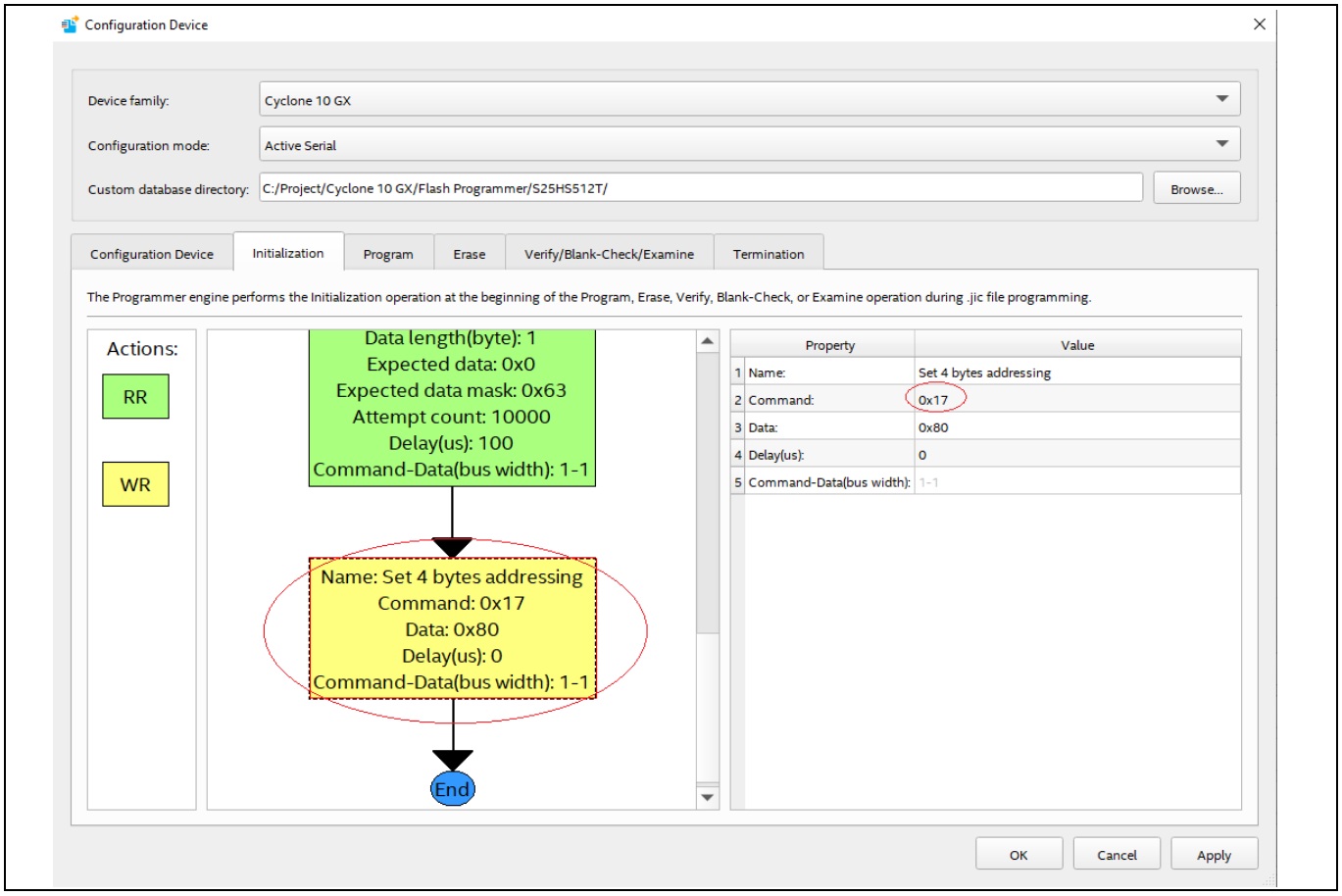


5. After Write Register action, read the status register to check the status of the write operation.

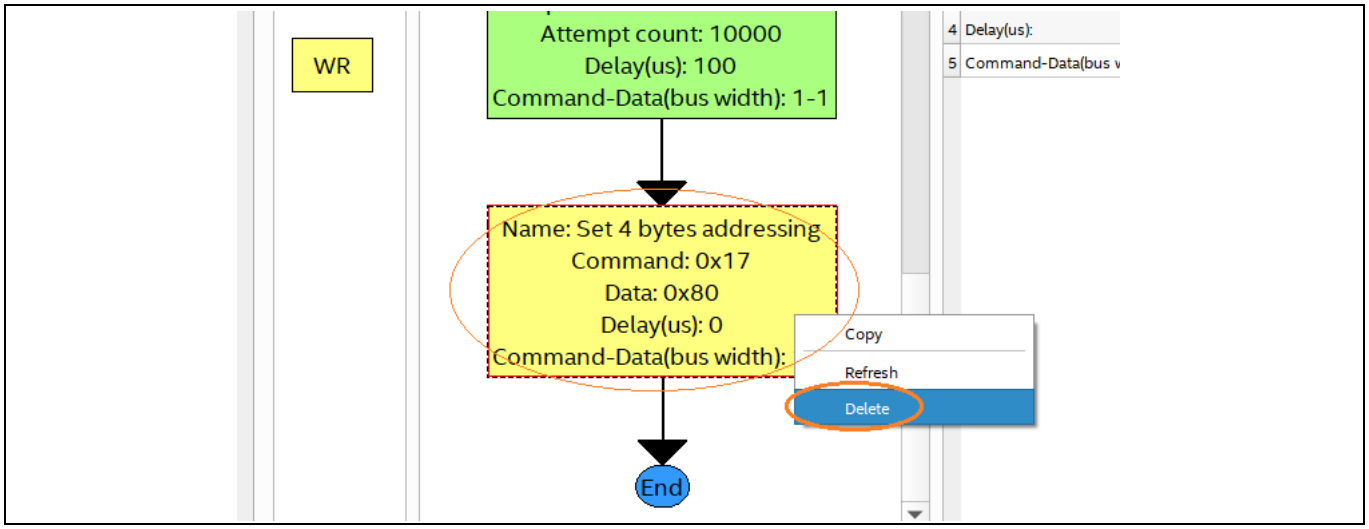
   STR1[6] is P_ERR, STR1[5] is E_ERR, STR1[1] is WEL, STR1[0] is RDYBSY. When the program operation completes successfully, these four bits should be all 0s; other bits are don't care. Therefore, the Expected data mask is 0110 0011b (0x63). The masked expected data is 0x0. See the S25HS512T datasheet for definition of Status Register bits.

   This Action (Read Status Register) is the same for checking the status of the flash array program/erase operation. It can also be used in Program and Erase flow template.

Procedures

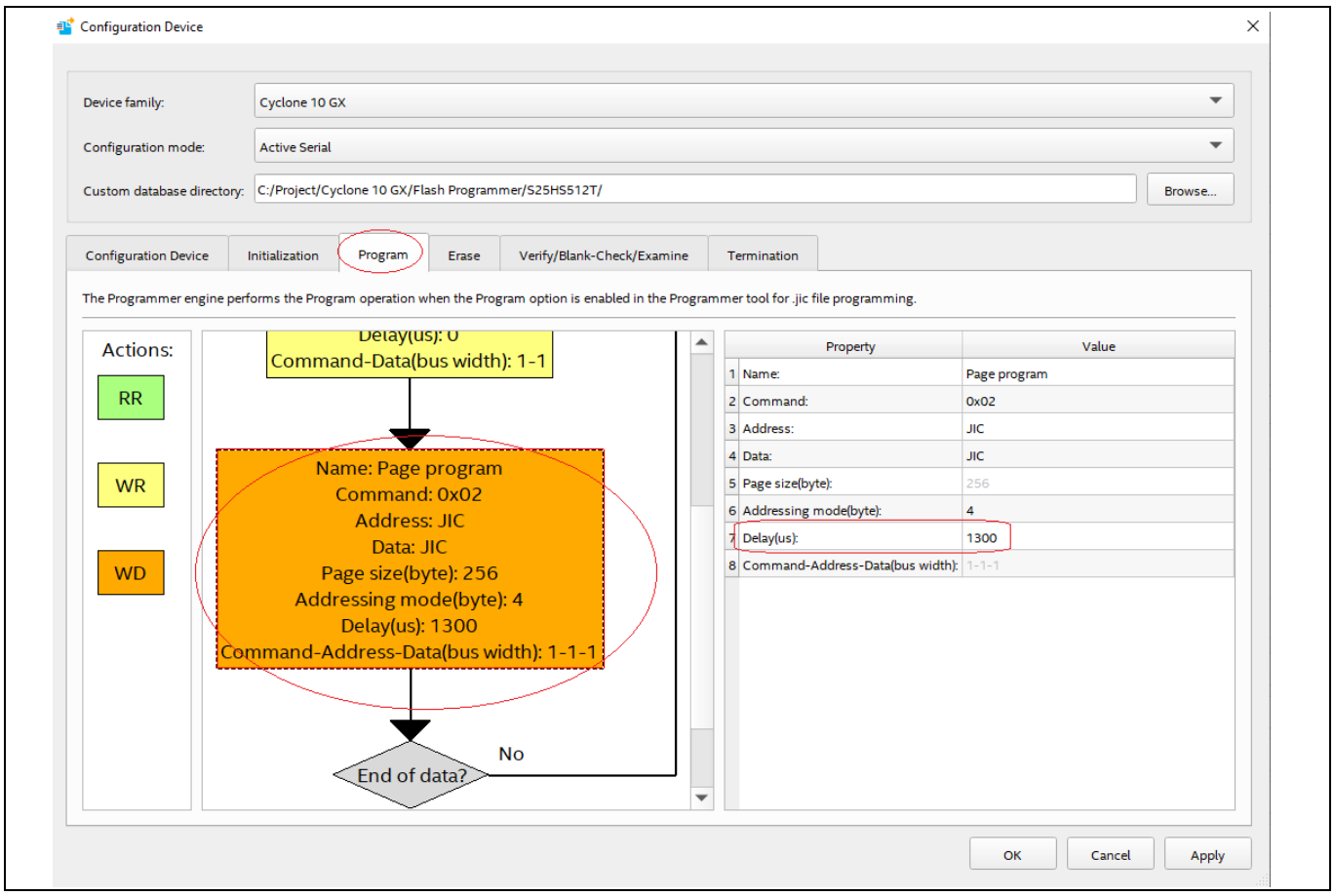


6. Right-click the **Set 4 bytes addressing** action and click **Delete**, and then click **Apply** to save the changes. This is because this command is not applicable to Infineon flash devices. For Infineon flash (S25HS512T), setting 4-byte addressing already done in the previous Write Register action.



3.2.3 Modify Program Flow Template

1. Click the **Program** tab, and then click the **Page Program** action.

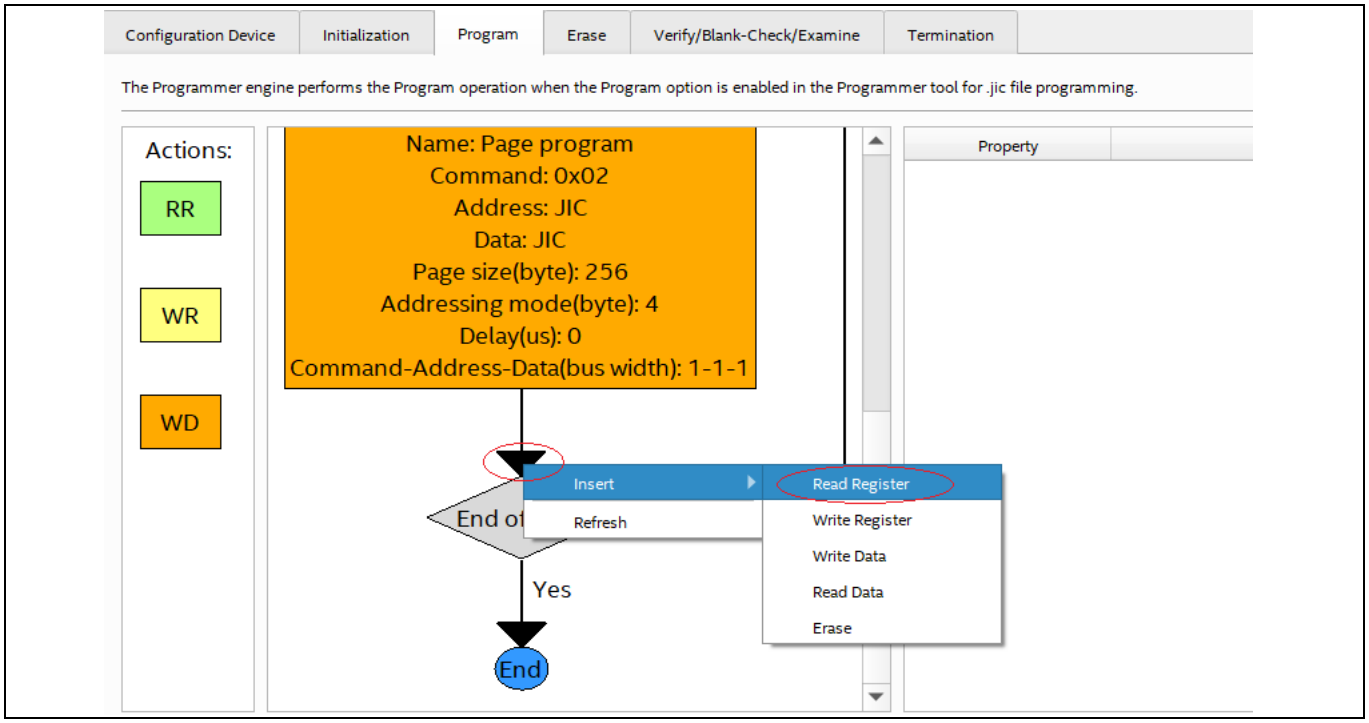


2. Modify the **Delay** value according to the maximum Page Program time specified in the flash datasheet. For example, for S25HS512T, the maximum Page Program time is 2175 µs.

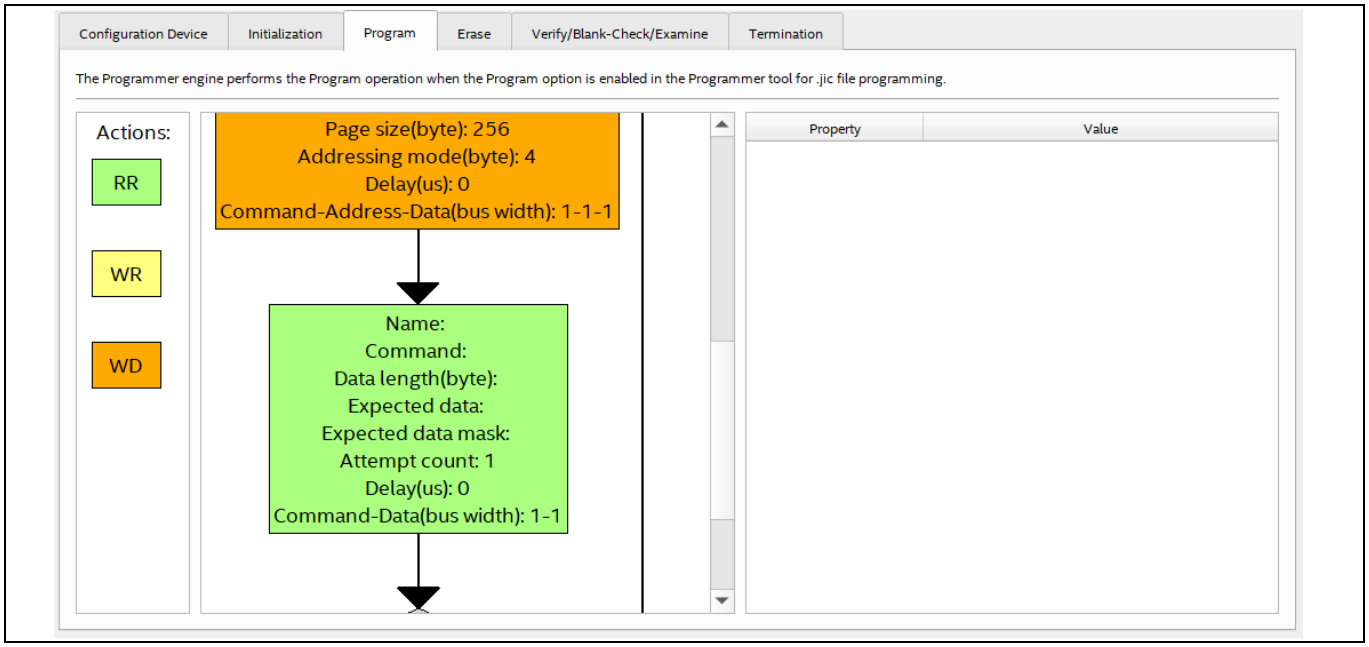
   Another option is to set the Delay value to '0' and add a Read Status Register action to check the status of the Page Program operation as follows.

   The Page Program size is the same for the default Program flow template and S25HS512T: 256 bytes. S25HS512T also supports larger Page Program size of 512 bytes. You can configure this value to 512 bytes by setting CFR3x[4]=1. To use the Page Program size of 512 bytes for S25HS512T, configure the value in the Write Register action in the Initialization Flow template.

Procedures

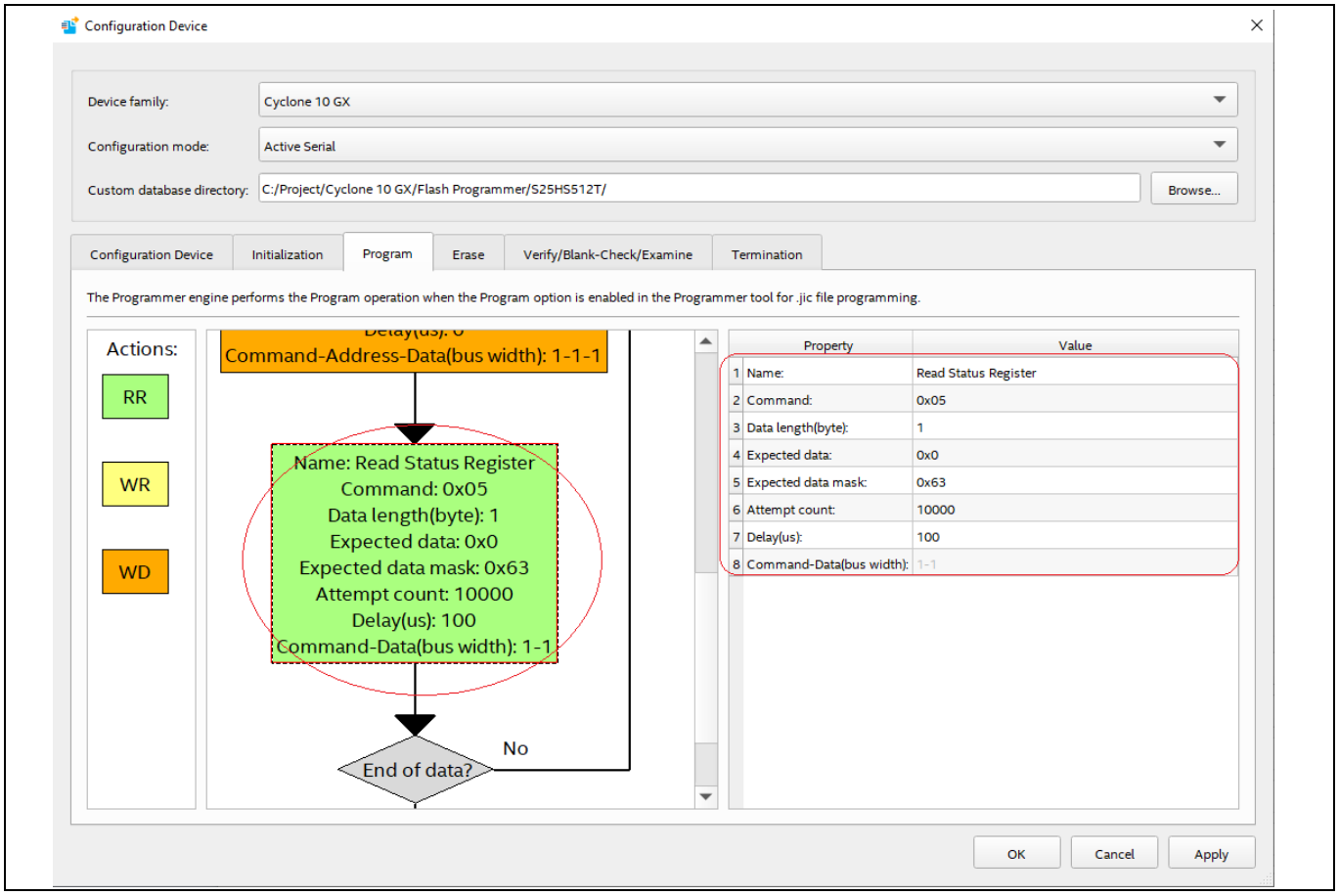


a) Right-click the arrow, and select **Insert** > **Read Register** to add the Read Register action to the flow.



b) Click the action that you added and configure its properties.

Procedures

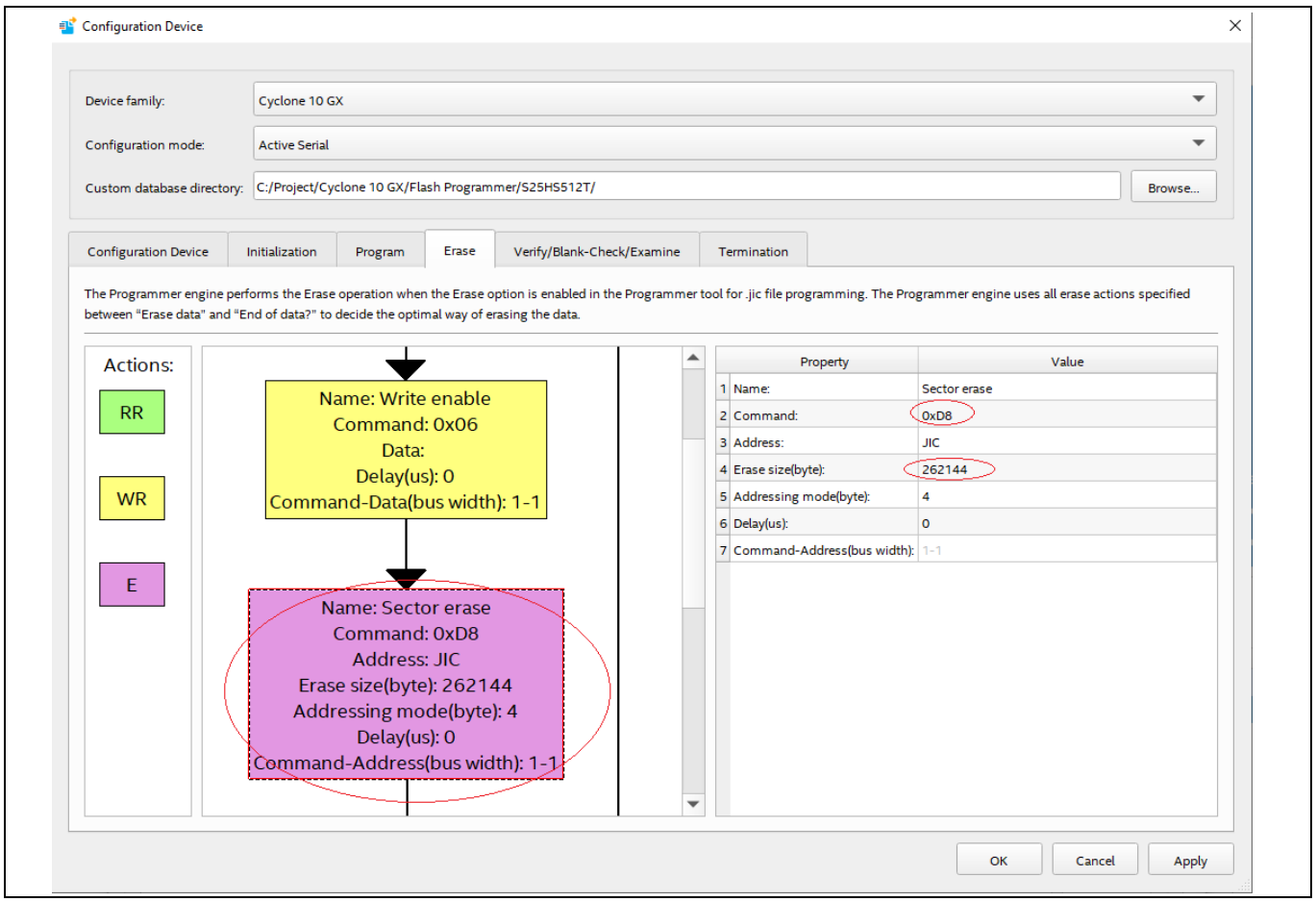


c) Configure the properties according to the flash datasheet. This is the same as the configuration shown in the Initialization template.

The time (Delay x Attempt count) must be larger than the maximum Page Program time specified in the flash datasheet. For example, for S25HS512T, the maximum Page Program time is 2175 µs; therefore, the Delay x Attempt count value must be larger than 2175us. You can enter a larger value because after the Read Register Action returns the Expected masked data, the flow will go to the next step without reaching the maximum attempt count.

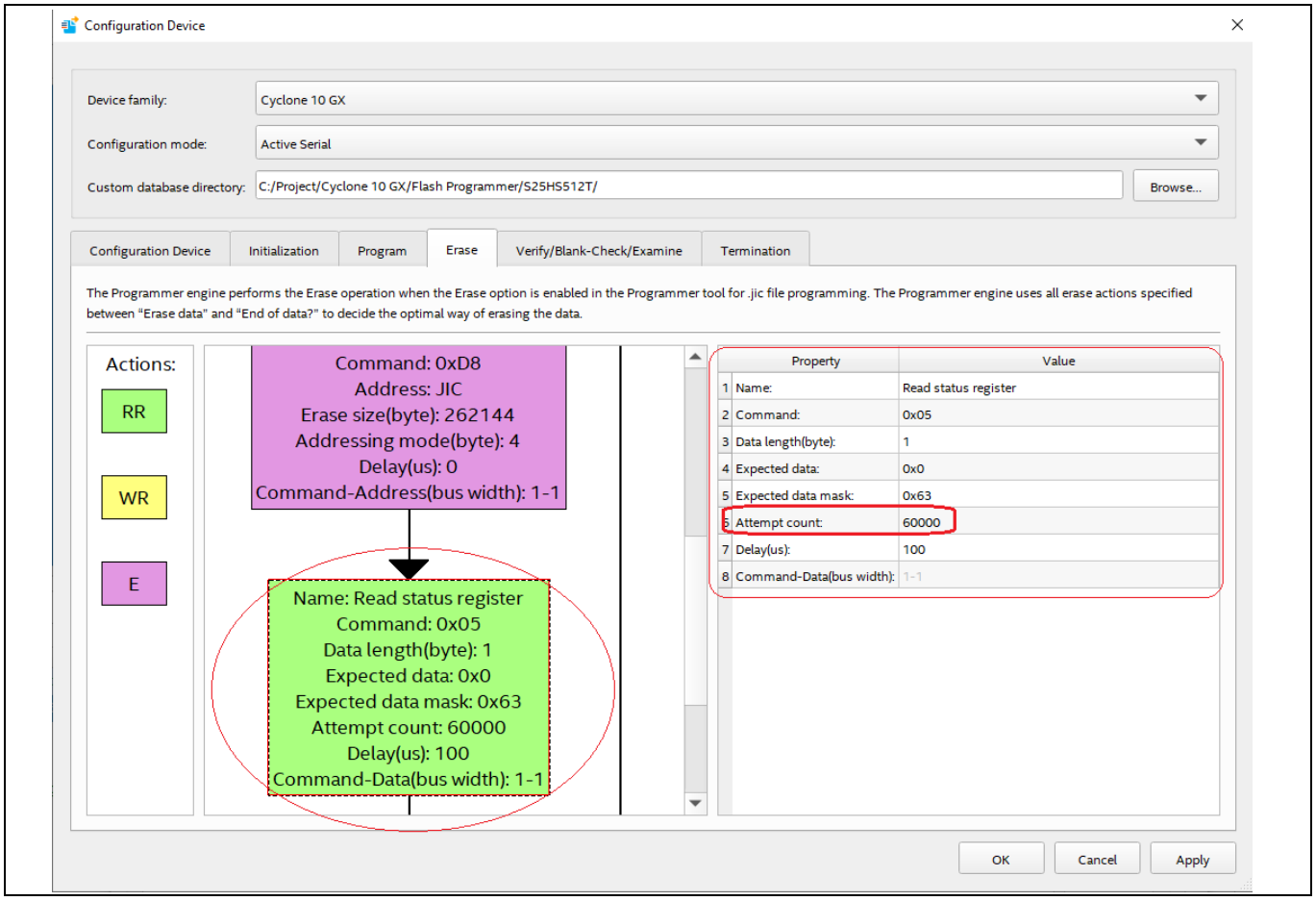
d) After configuring the properties, click **Apply**.

3.2.4 Modify Erase Flow Template



The default “Write enable” and “Sector erase” actions are compatible with S25HS512T uniform 256KB sector erase operation. You can leave these values unchanged because S25HS512T is already configured to uniform 256KB sector architecture in the Write Register action in Initialization flow template.

Procedures



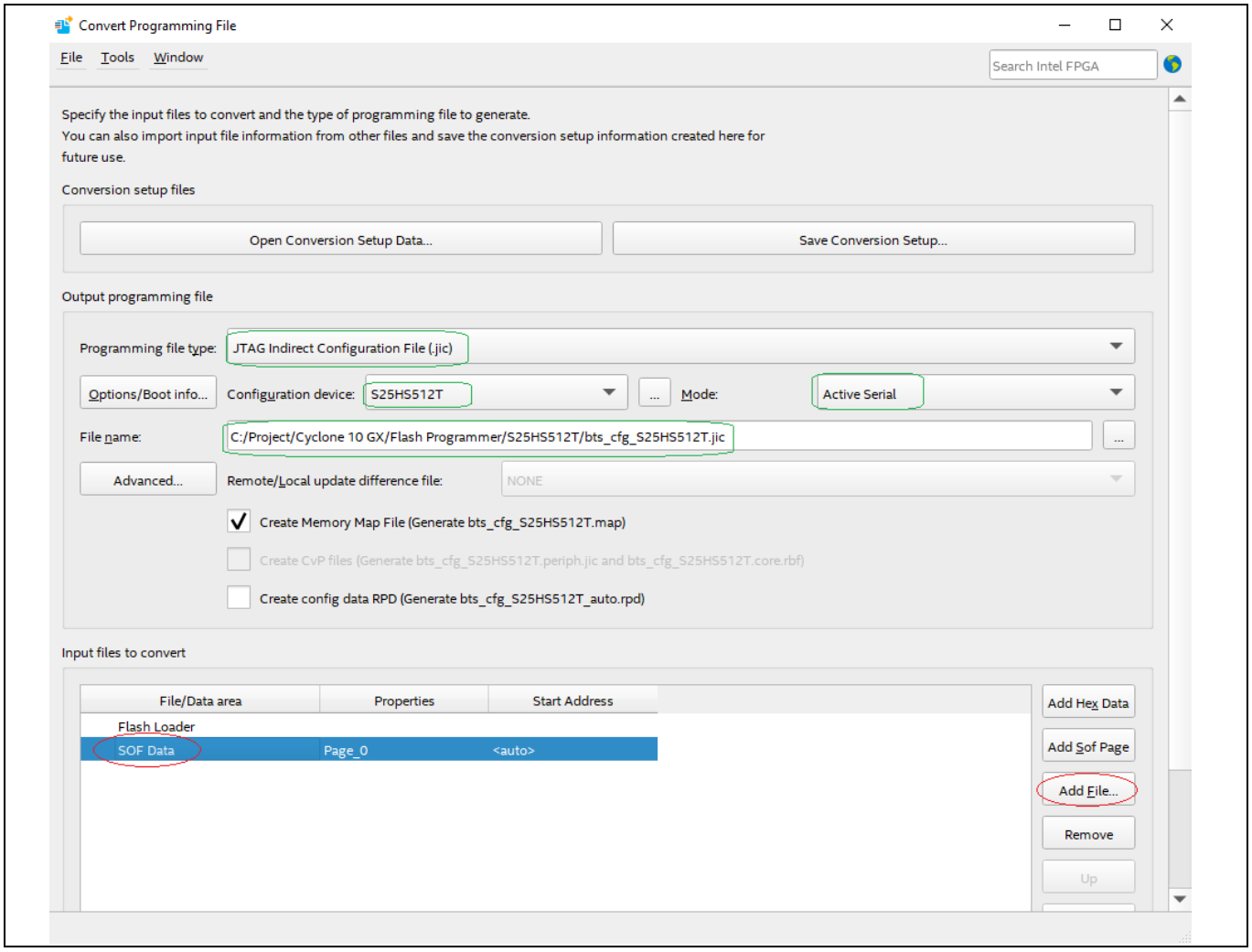
1. Click the **Read status register** action, and update the properties for S25HS512T such as command, expected data, and data mask. This action is similar to the **Read status register** action in the Initialization and Program flows.

Note: *The (Delay x Attempt count) must be larger than the maximum 256KB sector erase time specified in the flash datasheet. For S25HS512T, it is 5869 ms if the 256KB EnduraFlex™ architecture is enabled. See S25HS512T the datasheet for details.*

2. Click **OK** to save changes.

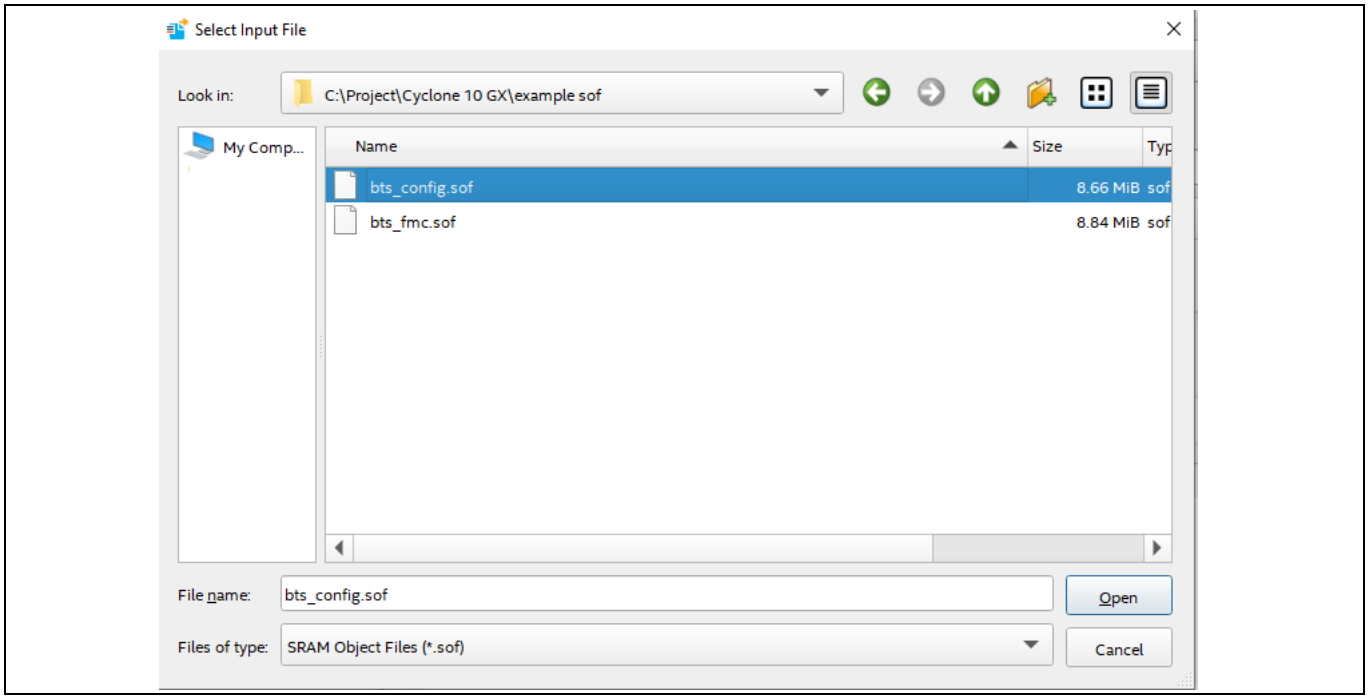
After these actions are configured, set up the Configuration Device to convert an .sof file to a .jic file that can be loaded to the flash device.

3.3 Convert the .sof File to Generate the .jic File



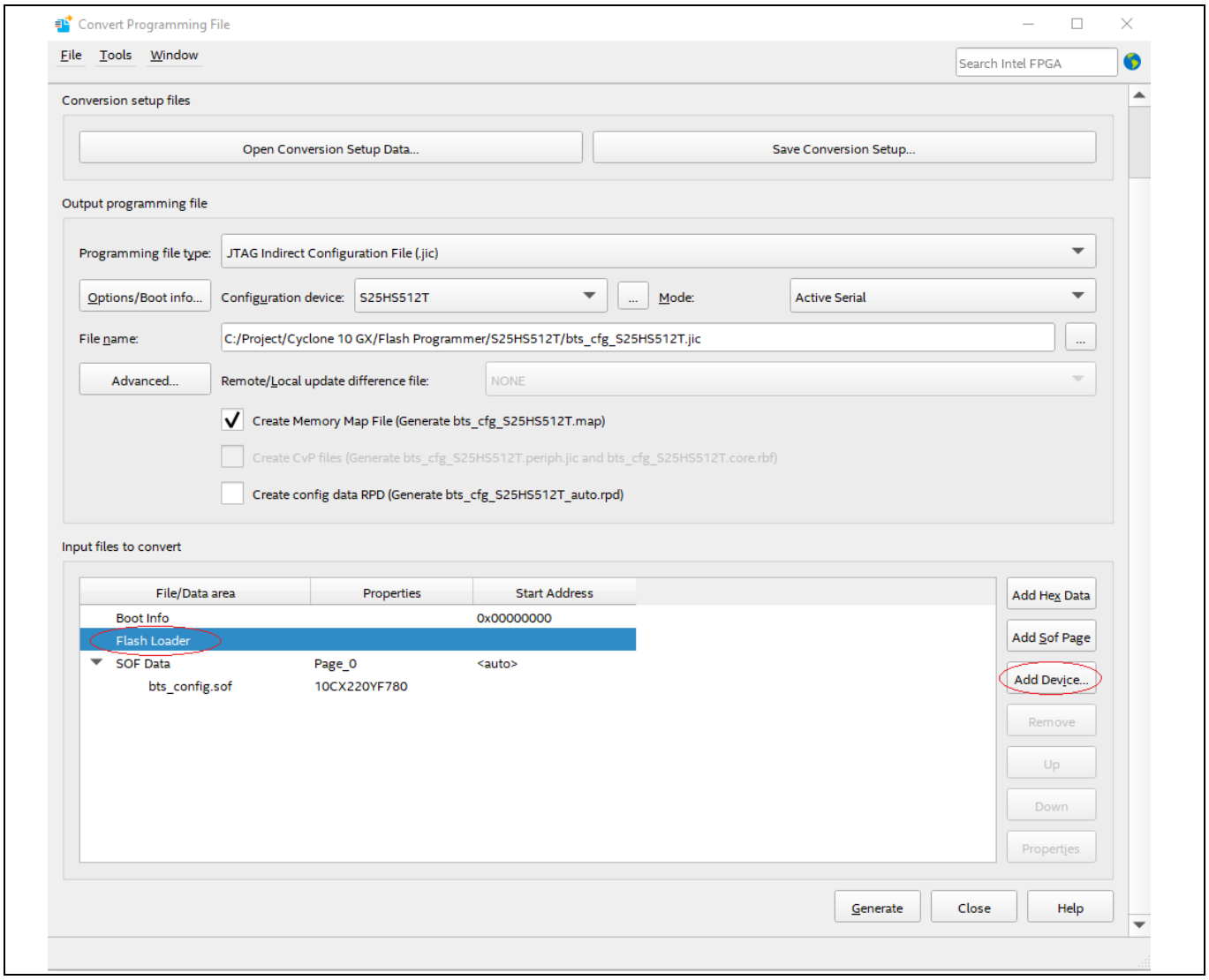
1. Set **Programming file type** to JTAG Indirect Configuration File (.jic).
2. Select S25HS512T (created in previous steps) as the Configuration device.
3. Select mode as **Active Serial**.
4. Specify the .jic file name to be generated and the location where the generated .jic file will be stored.
5. Select **SOF Data**, and then click **Add File…**.
6. Select the .sof file you are going to convert.

Procedures


Select Input File
Look in:
C:\Project\Cyclone 10 GX\example sof
My Comp...
Name
Size
Typ
bts_config.sof
8.66 MiB
sof
bts_fmc.sof
8.84 MiB
sof
File name:
bts_config.sof
Open
Files of type:
SRAM Object Files (*.sof)
Cancel

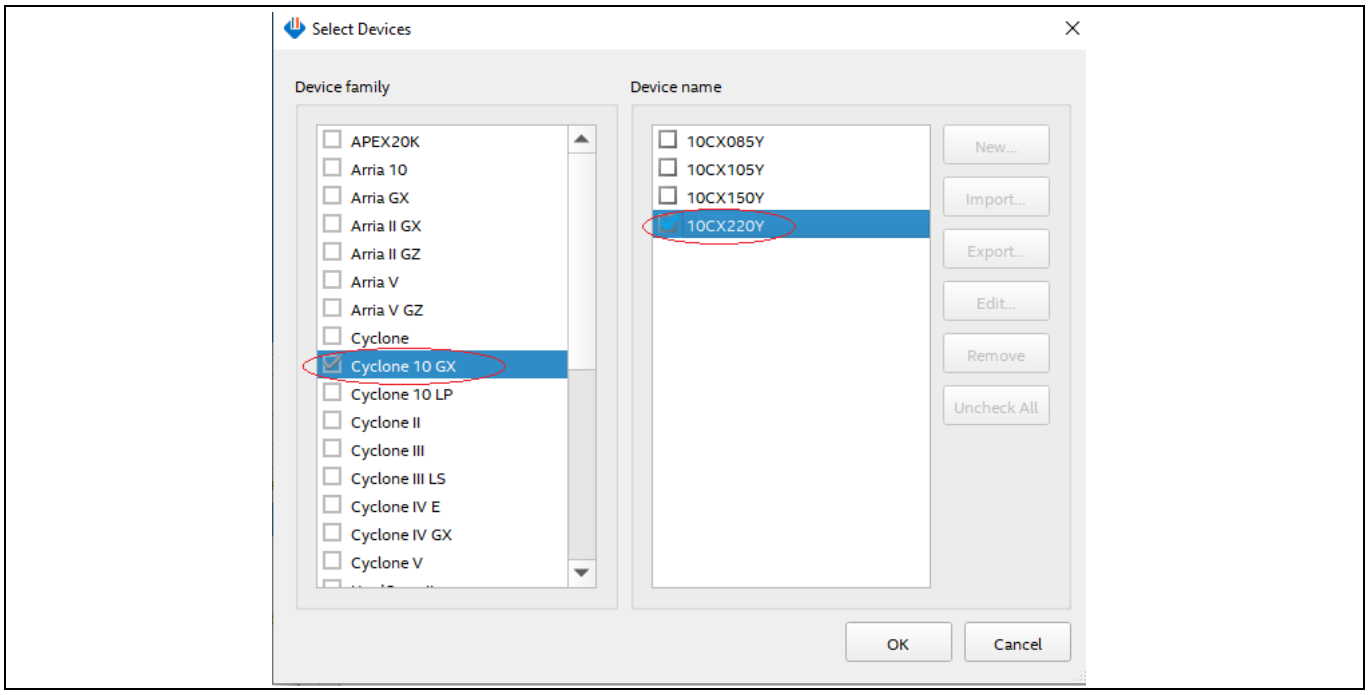
Procedures

7. After adding the .sof file, select **Flash Loader**, and then click **Add Device…**.



Procedures

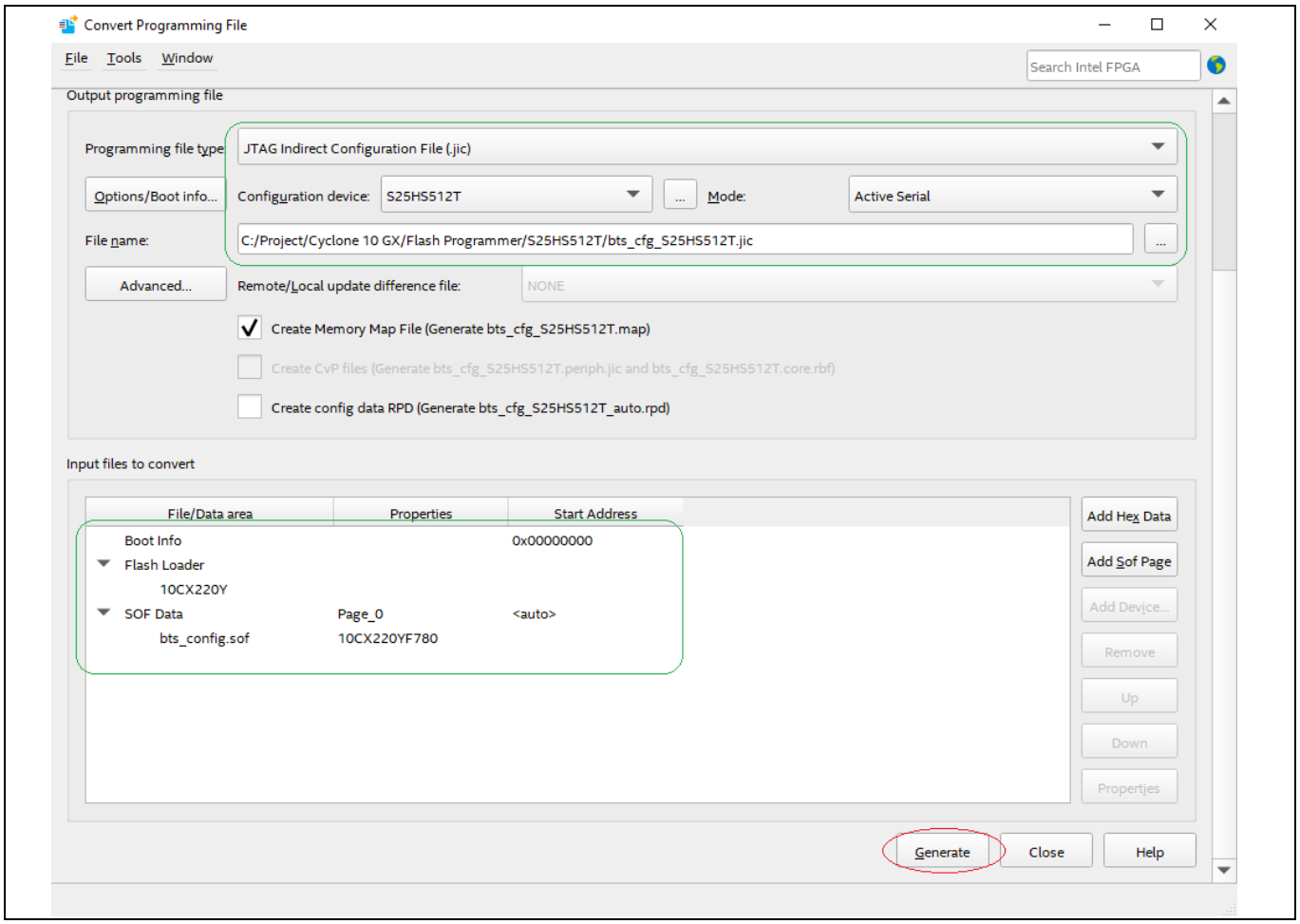
8. Select the device according to the FPGA device you are working on, and click **OK**.



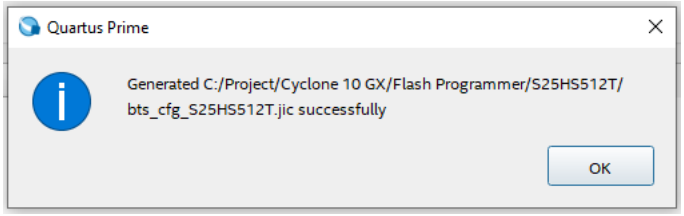
In this application note, the instructions are verified on Cyclone10 GX Dev Kit with Cyclone10 GX 10CX220Y FPGA device.

Procedures

9. Click **Generate**.



After a little while, you will see a popup window that indicates that the .jic file is generated successfully.



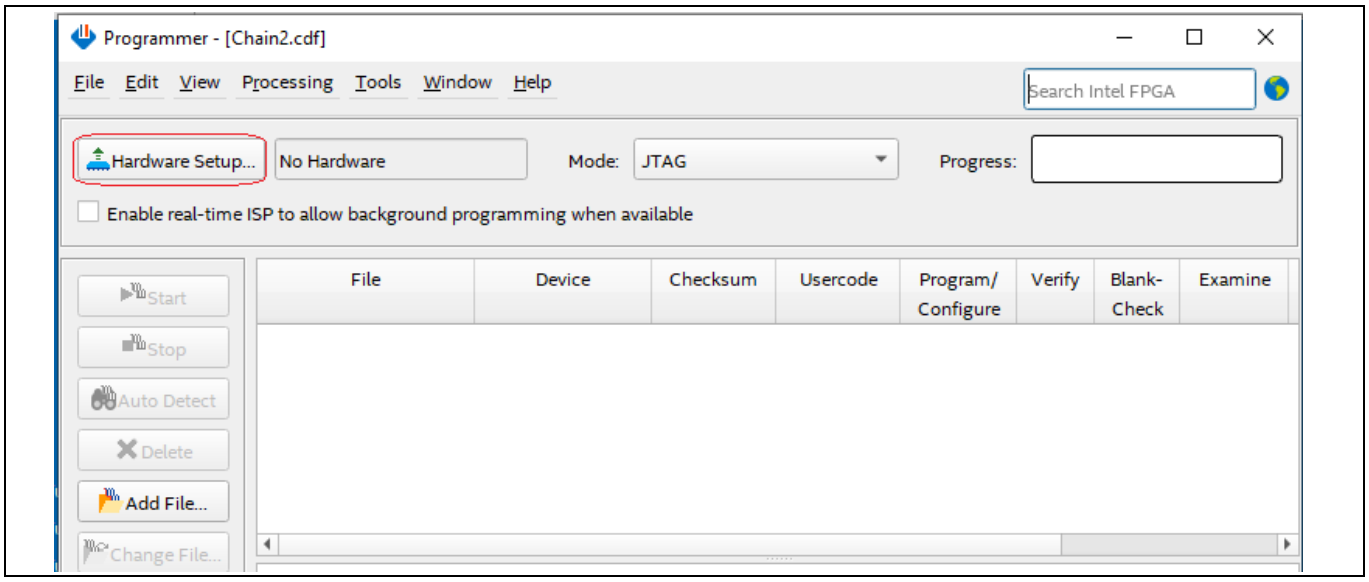
You can now program the generated .jic file into the configuration flash (S25HS512T in this example).

3.4 Program the .jic Configuration Data into the Infineon QSPI Flash Device

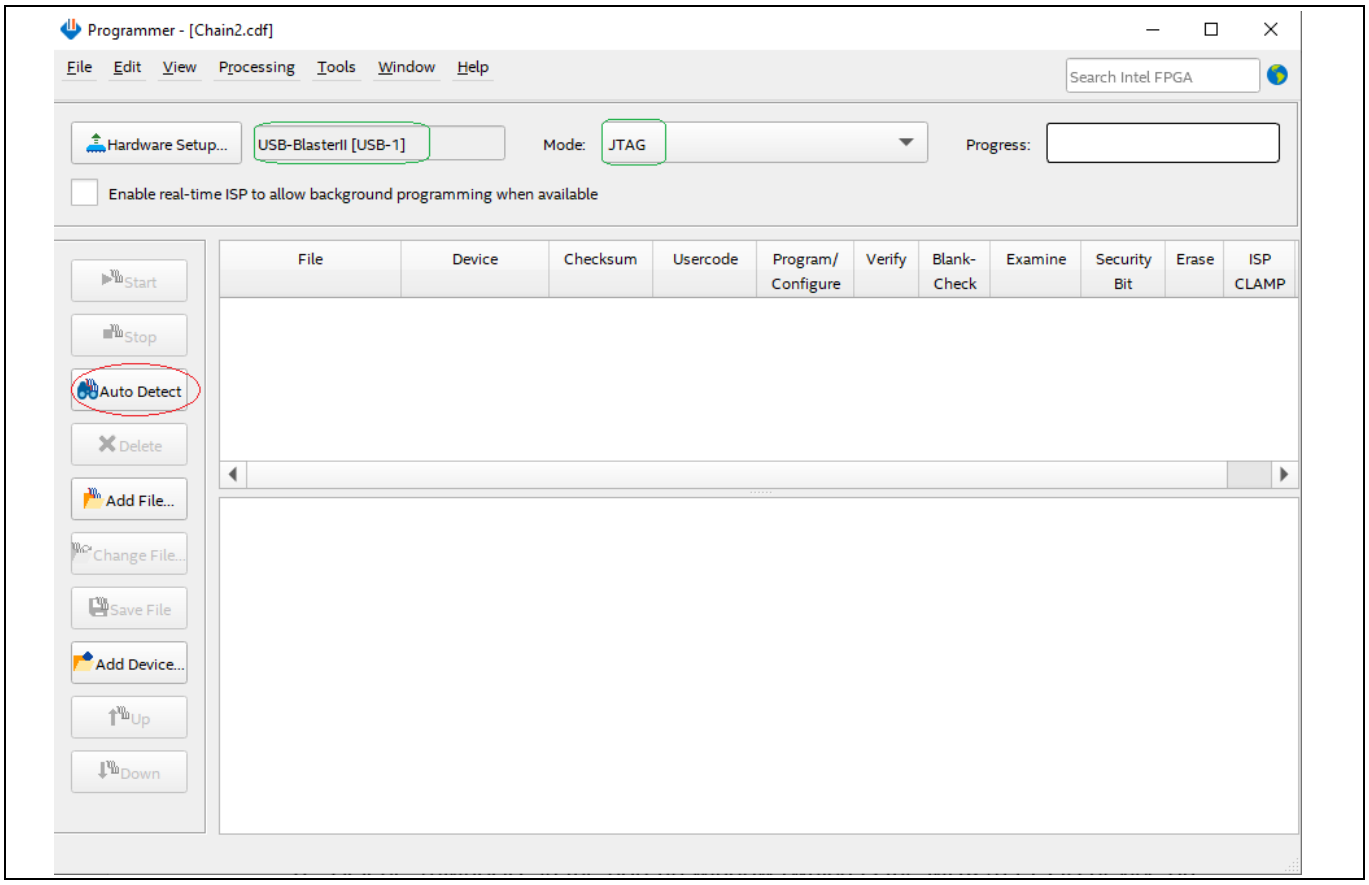
1. Connect Intel FPGA board to PC via Intel FPGA JTAG USB Download cable, and power on the FPGA board.
2. In Quartus Prime Pro, select **Tools** > **Programmer**.

Procedures

3. Click **Hardware Setup…**.



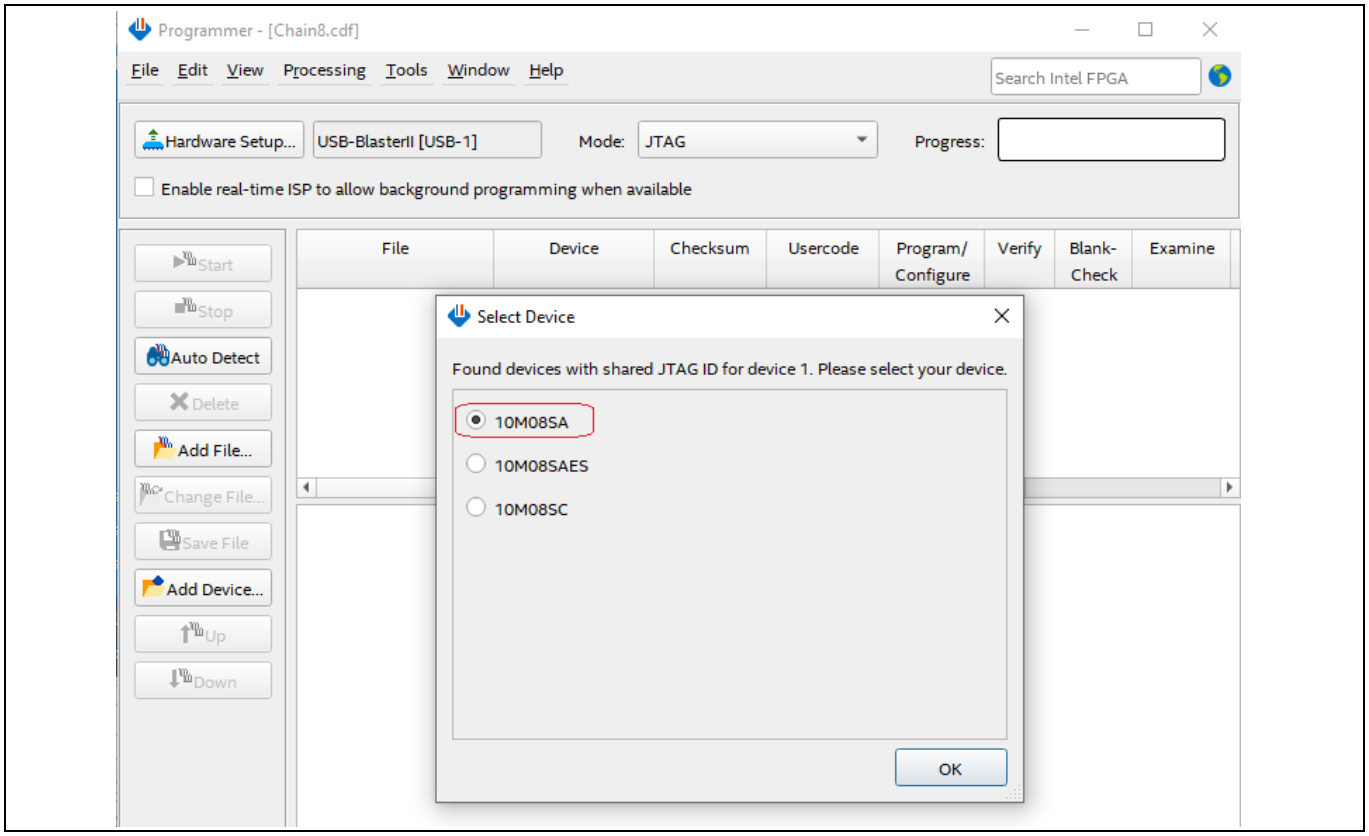
4. Click **USB-Blaster….**



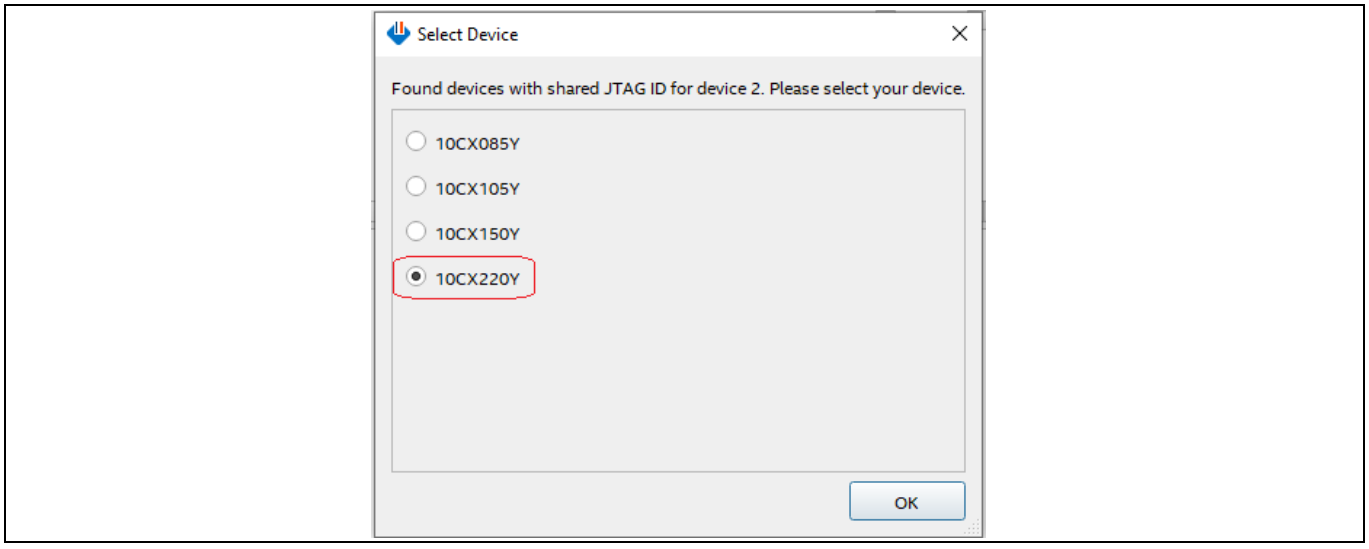
5. Click **Auto Detect**.

Procedures

6. Select **10M08SA** in the pop-up window. This is the MAX10 FPGA device on the Cyclone10 GX dev board on which the procedures were verified.

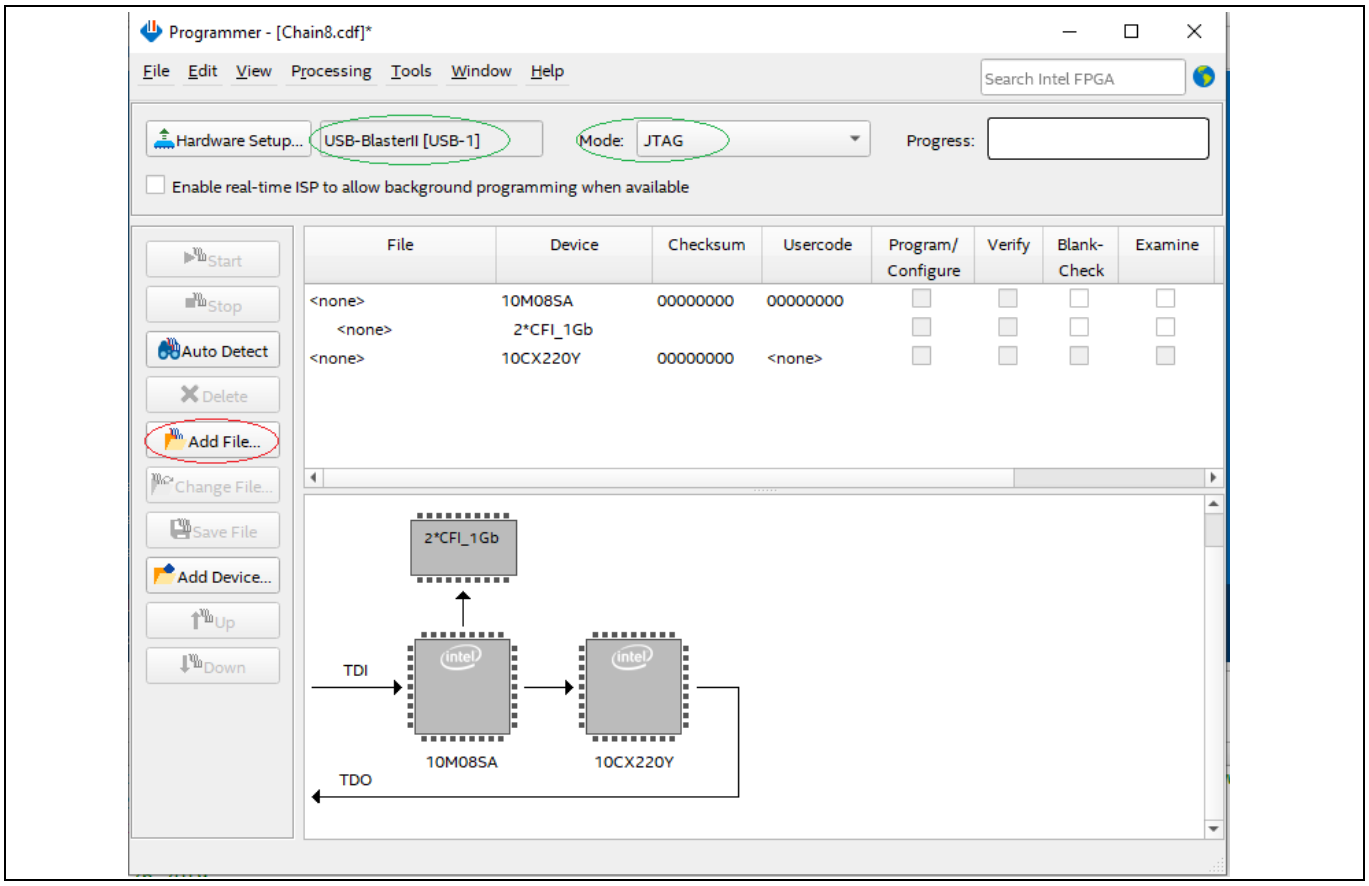


7. Select **10CX220Y** in the pop-up window. This is the Cyclone 10 GX FPGA device on the development board.

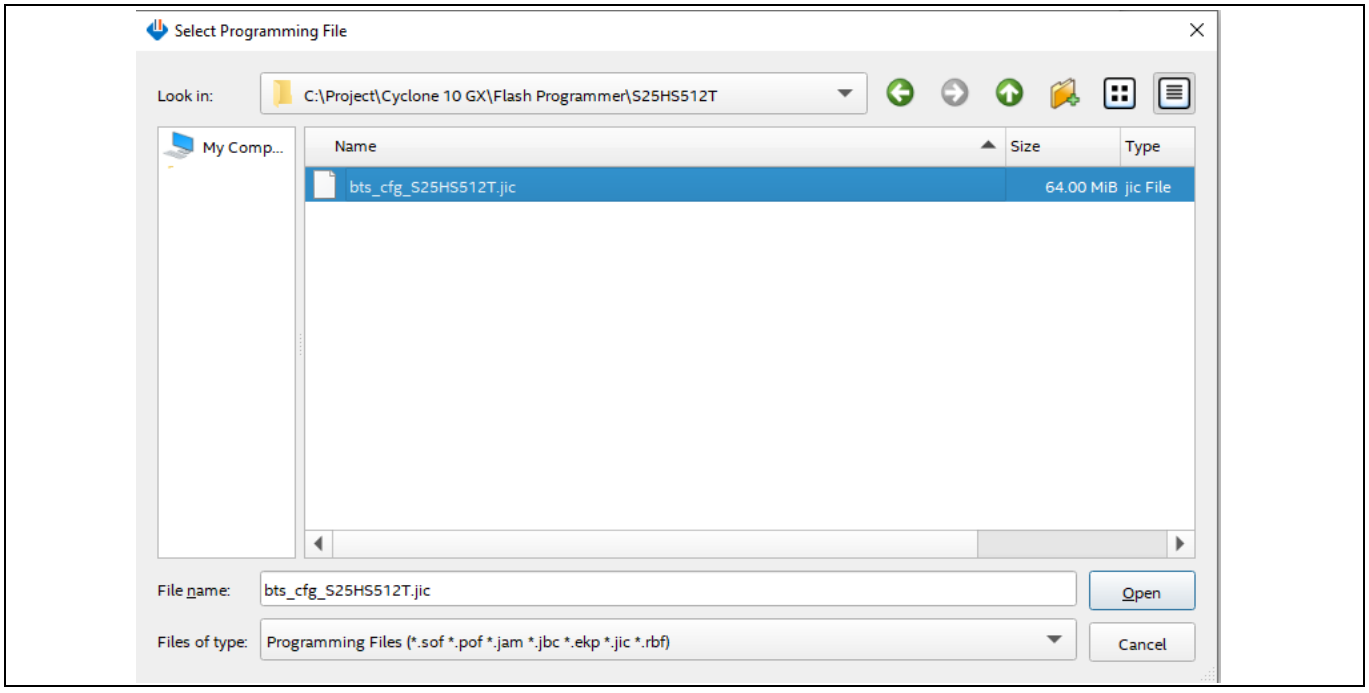


Procedures

8. Click **Add File….**

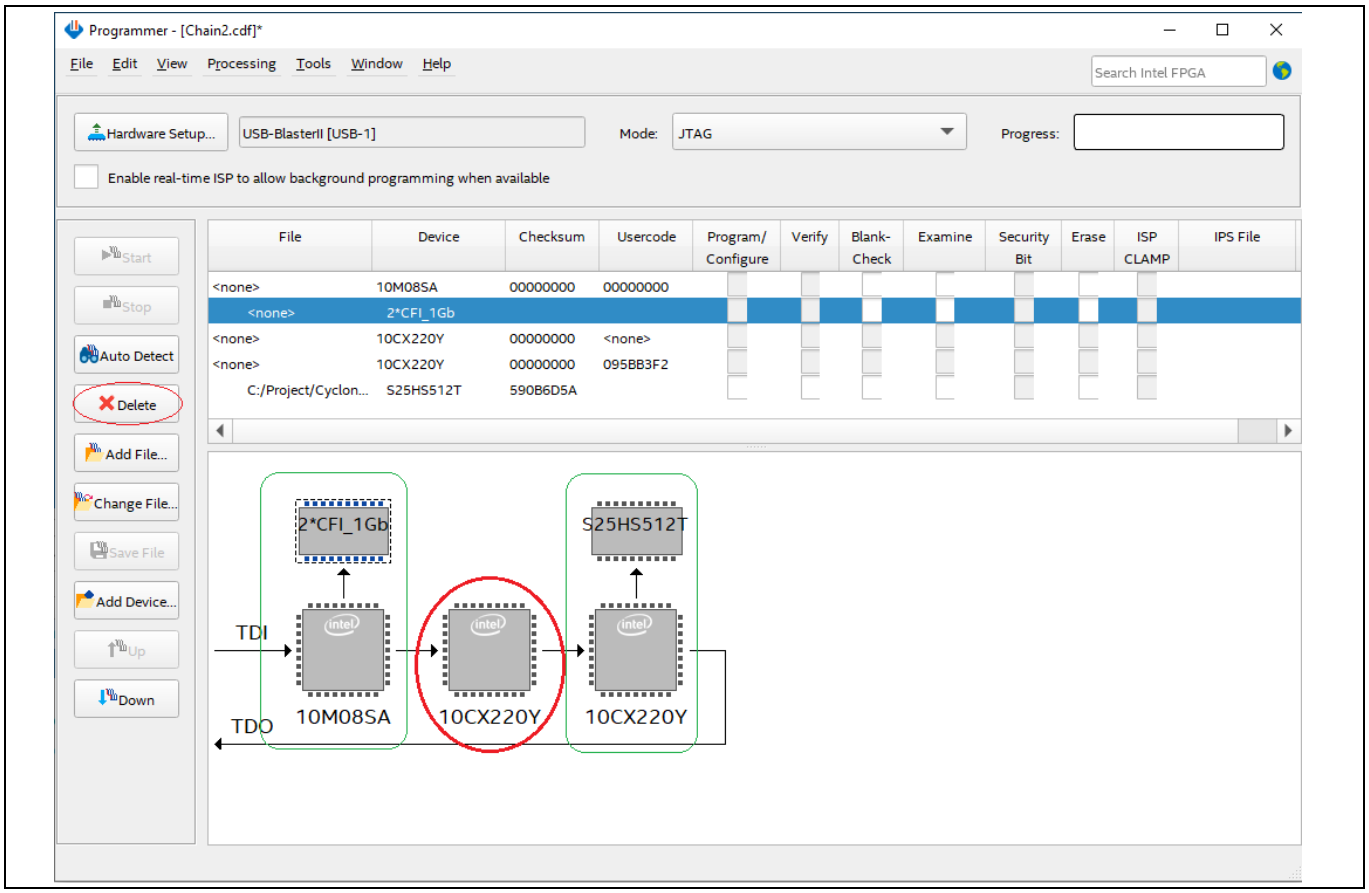


9. Open the .jic file generated in the earlier steps.



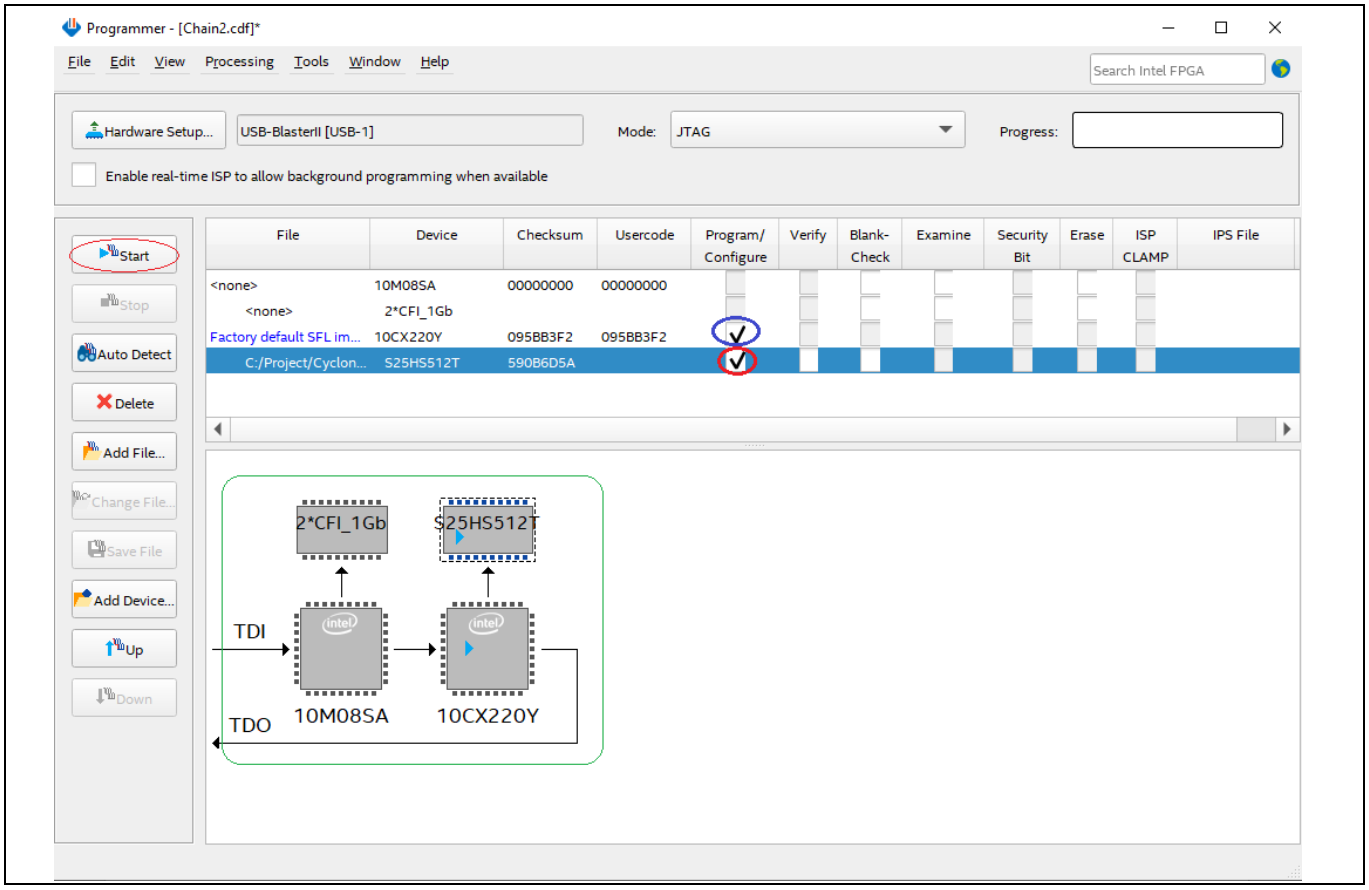
Procedures

10. If an extra device appears after adding the .jic file, select it and then click **Delete**.

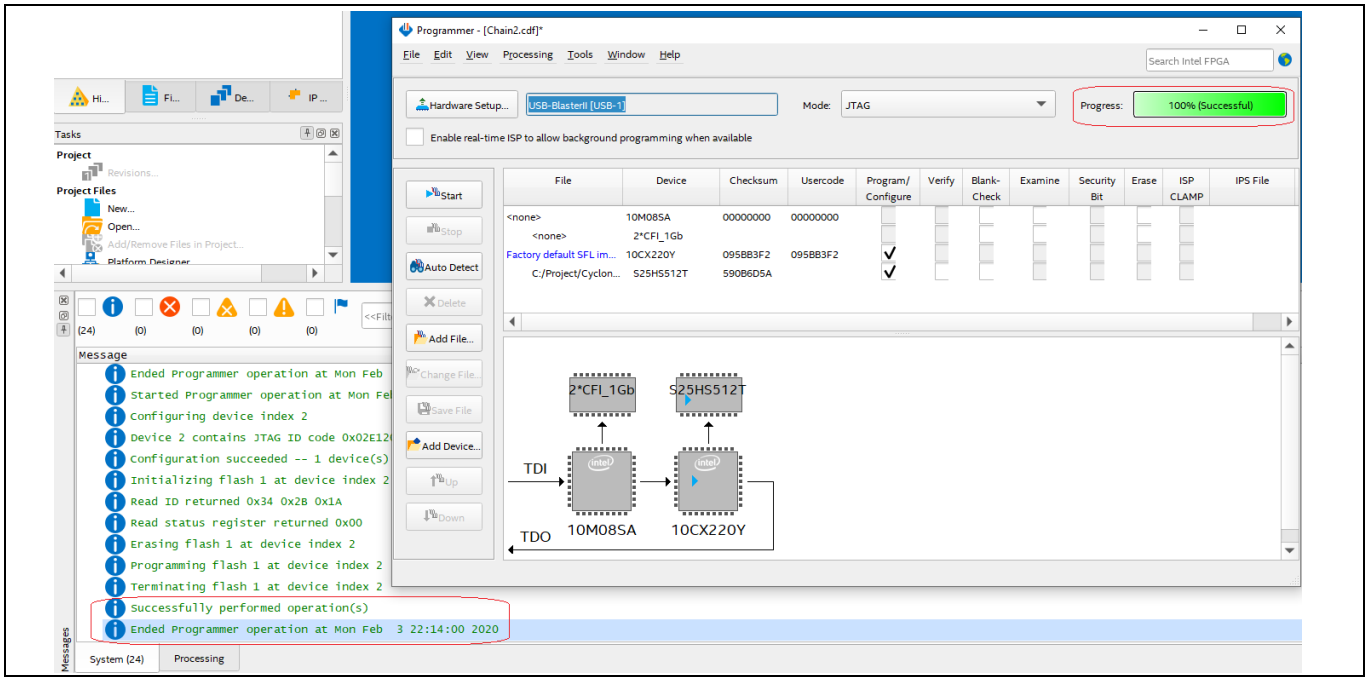


Procedures

11. Enable the **Program/Configure** option (check box in the red circle; the check box in the blue circle will be also enabled automatically).



12. Click **Start**.



13. When the progress bar shows 100% (Successful) and the message shows “Successfully performed operations”, power cycle the target board.

4 Conclusion

This application note describes how to enable Infineon S25HS512T QSPI SEMPER Flash to configure an Intel Cyclone 10 GX FPGA device.

The procedures introduced in this application note should also apply to other Infineon QSPI Flash families and Intel Arria 10 FPGA devices by configuring the flash and FPGA device according to respective datasheet.

References

Intel Cyclone 10 GX FPGA Development Kit User Guide

[1] **https://www.intel.com/content/www/us/en/programmable/documentation/hvu1509010715799.html?wapkw=Intel%20Cyclone%2010%20GX%20FPGA%20Development%20Kit%20User%20Guide**

Generic Flash Programmer User Guide: Intel Quartus Prime Pro Edition

[2] **https://www.intel.com/content/www/us/en/programmable/documentation/pah1554479151020.html?wapkw=Generic%20Flash%20Programmer**

Infineon S25HS-T datasheet

[3] 002-12345: S25HS256T / S25HS512T / S25HS01GT/ S25HL256T / S25HL512T / S25HL01GT, 256-Mb (32-MB), 512-Mb (64-MB), 1-Gb (128-MB) HS-T (1.8-V), HL-T (3.0-V) SEMPER Flash with Quad SPI

Revision history

Document version	Date of release	Description of changes
**	2020-02-26	New Application Note
*A	2021-05-03	Updated to Infineon template

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