AN229411

Error Correction Code (ECC) Management for TCFlash Protection in Traveo Family

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Associated Part Family: Traveo™ Family

This application note describes the Error Correct Code (ECC) mechanism used to protect the contents of TCFlash of Traveo family. ECC protection of external memories and other internal memories is possible, but its implementation is not within the scope of this application note.

1 Introduction

The automotive qualified Traveo family of microcontrollers offer a high-performance core – an Arm® Cortex®-R5 with an Advanced Memory Architecture. The Traveo Main Flash memory is accessible via two main interfaces for read, write, or both accesses: AXI interface for instruction fetch and data load bandwidth and ATCM interface to ensure a high-speed, low latency, and deterministic access for time critical code and data. In addition, to multi-port memory architecture, TCFlash supports ECC which differs according to the user interface.

Note that this application note is complementary to Traveo family hardware manual platform part.

2 Error Detection and Correction Techniques

Data stored in flash memories might get corrupted due to flash stress or over long lifetime. This creates a necessity for the system to verify the correctness of the data before or while executing the software. The error detection techniques help the system to check the integrity of the data in the memory:

- **Parity** - This technique requires additional bits to be added corresponding to the data. Parity only detects single bit failures in a memory. This is a simpler well-known error detection technique.
- **ECC** – This technique adds ECC bits along with the original data, which helps in detecting and correcting errors. The ECC scheme used in Traveo devices can detect up to 2-bit failures and correct single bit failures.

2.1 ECC Overview

ECC protection is one of the highly recommended measures of memory protection in highly reliable and safety-relevant systems.

There are several conventional algorithms used for ECC protection: single-error-correcting (SEC) Hamming code, single-error-correcting-double-error-detecting (SEC-DED) modified Hamming, and SEC-DED Hsiao code. Most of these algorithms are based on the principle of extending information bits with check bits in a way that the bit error is identified and corrected in case of one-bit error or detected in case of two errors.

Note: For the typical retention time and life cycle of the Flash memory, see the device datasheet. There is a minimum number of check bits needed for SEC-DED protection. Table 1 shows the relation between data width and the number of check bits.

Table 1. Number of Error Check Bits Used for SEC-DED

Data Width	Number of Check Bits
16	6
32	7
64	8
128	9

3 TCFlash ECC Handling in Traveo

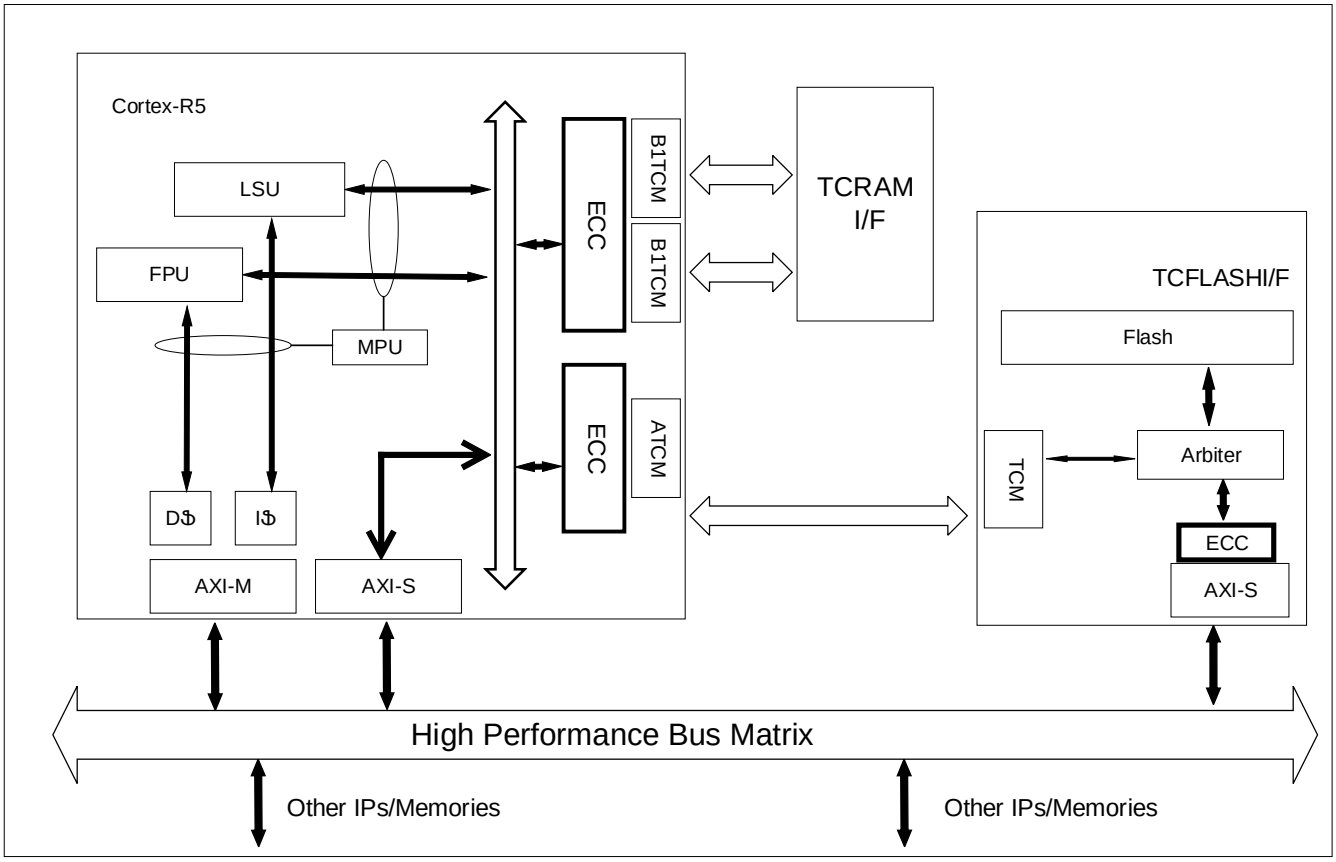
TCFlash is a flash memory used mainly to store programs. In user mode, Traveo device will be mapped to two regions:

- TCM region: TCFLASH is treated as an L1 memory in Arm architecture.
- AXI region: TCFLASH treated as an L2 memory in Arm architecture.

3.1 Block Diagram

Figure 1 shows that Flash in Traveo is accessible via two independent interfaces, and ECC is handled based on these interfaces.

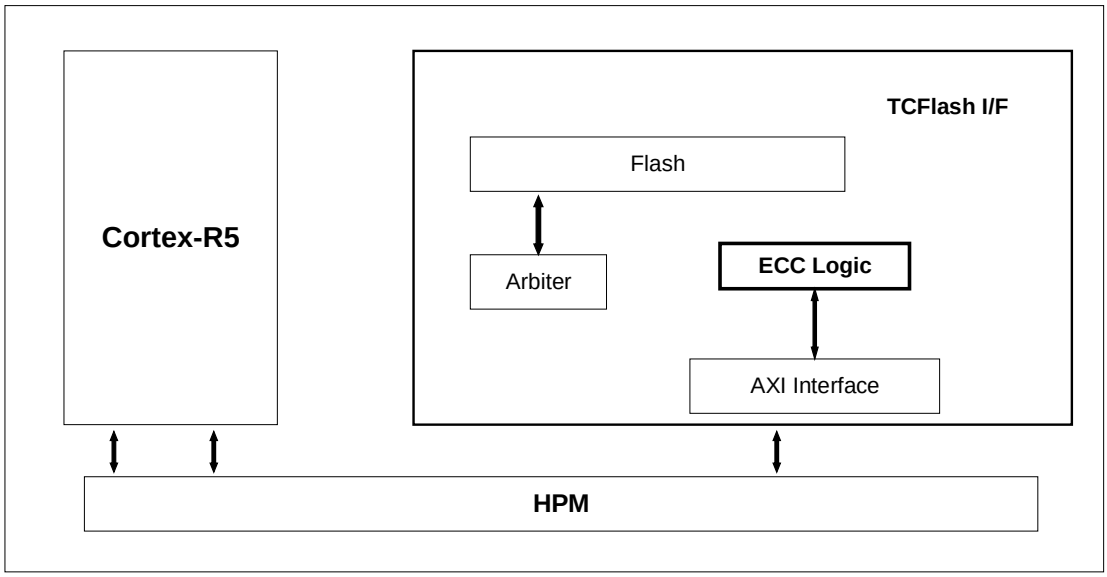
Figure 1. TCFLASH Interfaces Block Diagram



3.2 TCFlash Connected to AXI: Single Bit Error Handling

If TCFlash is accessed through the AXI interface, ECC will be handled by the logic in the TCFlash interface, which supports single-bit error correction and double-bit error detection (SEC-DED).

Figure 2. TCFLASH/AXI Simplified Block Diagram



The ECC logic used in TCFlash performs ECC generation during write access and syndrome check during read access similar to 64-bit ECC in the Arm Cortex-R5F core

Based on the value of the calculated syndrome, either of the following decision is made:

- No error is detected
- Single-bit error is detected
- Double-bit-or-more error is detected

The single-bit errors can be detected and corrected. If the result is double-bit-or-more error, error correction cannot be performed.

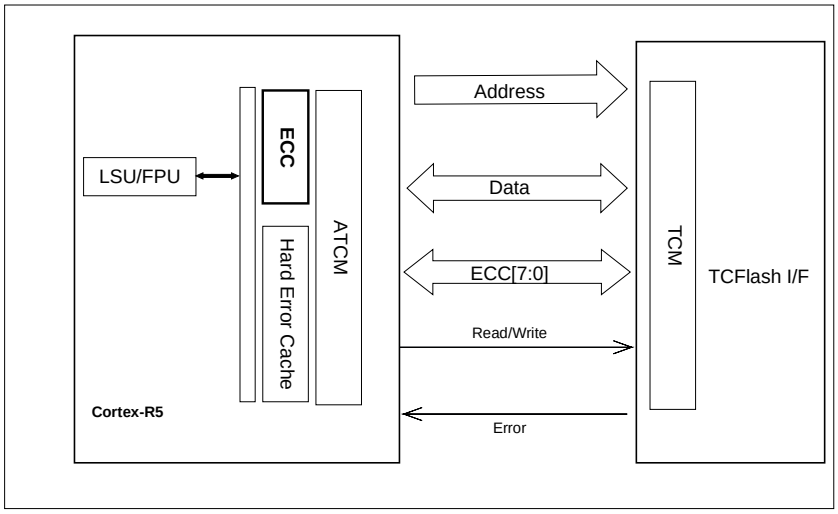
See Traveo Family Hardware Manual Platform Part for further details on the ECC Generation and Check.

3.3 TCFlash Connected to ATCM

The Traveo family offers an additional interface, TCM interface, to access TCFlash memory.

The advantage of accessing TCFlash through the TCM interface is that TCFlash is treated as an L1 memory in Arm architecture. Therefore, non-cacheable and low-latency access is possible. Hence, the deterministic behavior of TCM access.

Figure 3. Simplified Block Diagram ATCM/TCM Interface



When accessing TCFlash through the TCM interface, the ECC mechanism is handled by the Arm Cortex-R5. It is assumed that you are aware of the Cortex-R5 configuration option related to ATCM and ECC:

You can enable the TCM external errors (ACTRL.ATCMECEN) and TCM ECC check (ACTRL.ATCMPCEN) separately by setting the appropriate bits in the Cortex-R5 Auxiliary Control Register.

You can enable the TCM ECC correction by setting the appropriate (SACTRL.ATCMECC) bit in the Cortex-R5 Secondary Auxiliary Control Register:

- If the SACTRL.ATCMECC bit is disabled, a Data/Prefetch Abort exception will be generated for single bit errors.
- If the SACTRL.ATCMECC bit is enabled, the correct-and-retry scheme will cause a Data Abort exception because Flash is connected to ATCM port and will respond with an error on the write attempt.

In Arm architecture, when a correctable ECC error is detected on a TCM read made by instruction-side or data-side, the processor generates the correct data and tries to write it back to the TCM (“correct-and-retry” scheme). Since writing to Flash memory is in general not possible, an error is triggered, and the CPU enters a Data Abort exception.

This behavior or feature on the TCM port protocol is a good indicator during development, test, and qualification to detect different error conditions listed in External TCM Port Signals.

3.4 External TCM Port Signals

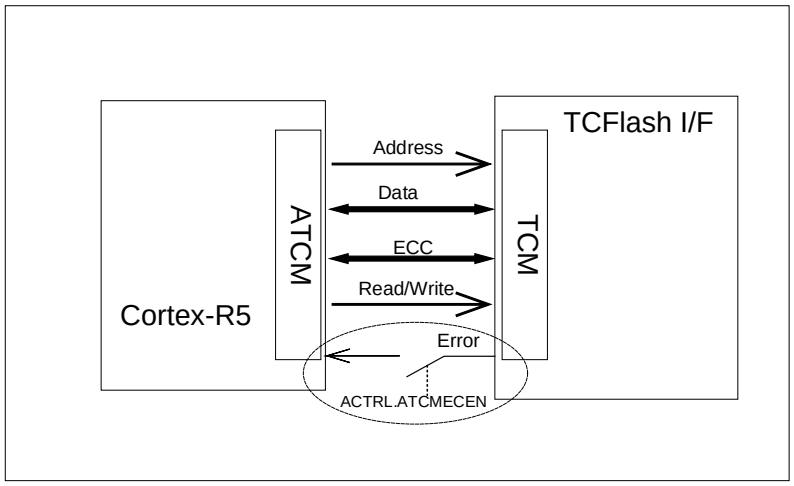
The TCM port includes signals that can be used to signal an error on a TCM transaction. If enabled, this causes the processor to take the appropriate type of abort for instruction and data accesses or to generate a SLVERR response to an AXI-slave transaction.

The TCM External Error signal is used by the TCFlash I/F to signal different error conditions to the CPU:

- Any write access to ATCM area: This occurs due to the “correct-and-retry” scheme.
- Access to an illegal /reserved address: Reserved areas exist because TCM address space = 2^n, but flash-size (for example, 64 KB + 4 MB) ≠ 2^n.
- Access during program/erase algorithm execution.

To get the intended behavior, single bit error correction and double bit error detection. when accessing through the TCM interface, disable the TCM external error by writing 0 to the ATCMECEN bit in the Cortex-R5 ACTLR register.

Figure 4. Disabling TCM External Error



Note that if the TCM external error is disabled:

- Data abort exception caused by corrected data write-back is prevented.
- Cortex-R5 will work with the corrected data.
- Cortex-R5 will no longer be notified of the error conditions.

4 Summary

Memory cells are more prone to bit failures under flash stress or over long lifetime. While the probability of single-bit error is relatively high and needs the countermeasure ECC to avoid data loss, double-bit errors within a word (data width) are very rare and will hardly been seen during the lifetime of a vehicle. Nevertheless, double-bit errors are detected by ECC and erroneous code execution is prevented.

5 Related Documents

- Cortex®-R5 and Cortex-R5F Technical Reference Manual
- Technical Reference Manuals
  - S6J3110 Series Hardware Manual (Doc.No.002-10667)
  - S6J3120 Series Hardware Manual (Doc.No.002-04855)
  - S6J3200 Series Hardware Manual (Doc.No.002-04852)
  - S6J32E/F/G Series Hardware Manual (Doc.No.002-12500)
  - Traveo Family Hardware Manual Platform Part for S6J3200 Series (Doc.No.002-04854)
  - S6J3310/20/30/40/50 Series Hardware Manual (Doc.No.002-10185)
  - Traveo Family Hardware Manual Platform Part for S6J3310/3320/3330/3340/3350 Series (Doc.No.002-07884)
  - S6J3400 Series Hardware Manual (Doc.No.002-09919)
- Series Datasheet
  - S6J311E/D/C/B Series Datasheet (Doc. No.002-05681)
  - S6J311A/9/8 Series Datasheet (Doc. No.002-04632)
  - S6J3120 Series Datasheet (Doc.No.002-04863)
  - S6J3200 Series Datasheet (Doc.No.002-05682)
  - S6J32E/F/G Series Datasheet (Doc.No.002-10689)
  - S6J3310/20/30/40 Series Datasheet (Doc.No.002-10635)
  - S6J3350 Series Datasheet (Doc.No.002-10634)
  - S6J3400 Series Datasheet (Doc.No.001-97829)

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