

Migration from Micron MT28E/MT28F to Infineon S29GL-S NOR Flash Family

About this document

Scope and purpose

This application note provides guidelines for migrating from Micron MT28E/MT28F to Infineon S29GL-S NOR Flash families.

Intended audience

This application note is for NOR flash customers who intend to migrate the Micron MT28E/MT28F to Infineon S29GL-S NOR Flash families.

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1 Introduction

This application note provides migration guidelines for migrating from Micron MT28E/MT28F to Infineon S29GL-S NOR Flash Families.

The discussions will focus on same-density migrations, specifically the cases when migrating from MT28E/MT28F to S29GL-S. Considerations regarding migration to and from other densities can be extrapolated from these discussions. This application note is based on the information currently available from datasheets and application notes publicly available from Infineon and Micron. You should also see the latest relevant specifications.

2 Feature Comparison

Table 1 shows a feature comparison summary of the Micron MT28E/MT28F flash memory device to the Infineon S29GL-S MirrorBit™ flash family device.

Table 1 General Feature Comparison

| Products | | MT28E | MT28F | S29GL-S | Migration Issue |
|--|--|--|--------------------------|---|-----------------|
| Process Node | | 45 nm FG | 45 nm FG | 65 nm | No |
| V _{CC} | | 2.7 ~ 3.6 V | 2.7 ~ 3.6 V | 2.7 ~ 3.6 V | No |
| V _{IO} | | 1.65 ~ V _{CC} V | 1.65 ~ V _{CC} V | 1.65 ~ V _{CC} V | No |
| Random Access Time | | 70 ns (128 Mb, 256 Mb) 105 ns (1Gb) | 105 ns | Density: V _{CC} =V _{IO} /Versatile I/O 64 Mbit: 70 ns/80 ns 128 Mbit: 90 ns/100 ns 256 Mbit: 90 ns/100 ns 512 Mbit: 100 ns/110 ns 1 Gbit: 100 ns/110 ns | No |
| Page Access Time | | 20 ns | 20 ns | Density: V _{CC} =V _{IO} /Versatile I/O 64 Mbit: 15 ns/25 ns 128 Mbit: 15 ns/25 ns 256 Mbit: 15 ns/25 ns 512 Mbit: 15 ns/25 ns 1 Gbit: 15 ns/25 ns | No |
| Test Condition (Output Load Capacitance) | | 30 pF | 30 pF | 30 pF | No |
| Buffer Programming | (512 Bytes) | 2.0 MB/s | 2.0 MB/s | 1.5 MB/s | Maybe |
| | (256 Bytes) | N/A | N/A | 625 KB/s | Maybe |
| Sector Erase | (128 KB) | 640 KB/s | 640 KB/s | 477 KB/s | Maybe |
| | (64 KB) | N/A | N/A | 213 KB/s | Maybe |
| Active Read at 5 MHz, 30 pF | 64 Mbit | N/A | N/A | 30mA | Maybe |
| | 128 Mbit 256 Mbit 512 Mbit 1 Gbit | 26 mA | 26 mA | 60 mA | Maybe |
| Program/Erase Current Consumption | 64 Mbit | N/A | N/A | 60 mA | Maybe |
| | 128 Mbit 256 Mbit 512 Mbit 1 Gbit | 35 mA | 35 mA | 100 mA | Maybe |

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Feature Comparison

| Products | | MT28E | MT28F | S29GL-S | Migration Issue |
|------------------------------|----------|------------|------------|--------------|-----------------|
| Standby Current Consumption | | 65 μ A | 75 μ A | 100 μ A | No |
| Density | | | | | |
| 64 Mbit | | No | No | Yes | Yes |
| 128 Mbit | | Yes | No | Yes | No |
| 256 Mbit | | Yes | No | Yes | No |
| 512 Mbit | | Yes | Yes | Yes | No |
| 1024 Mbit | | Yes | Yes | Yes | No |
| 2048 Mbit | | No | Yes | Yes | Maybe |
| Sector Architecture | | | | | |
| Parameter Block (8 KB) | 64 Mbit | N/A | N/A | Yes | Maybe |
| | 128 Mbit | No | No | No | No |
| | 256 Mbit | | | | |
| | 512 Mbit | | | | |
| | 1 Gbit | | | | |
| Uniform (128 KB/ 64 KB) | | Yes | Yes | Yes | No |
| Access | | | | | |
| x8 Data Bus Width | | Yes | No | Yes | Maybe |
| x16 Data Bus Width | | Yes | Yes | Yes | No |
| Synchronous | | No | No | No | Maybe |
| Asynchronous | | Yes | Yes | Yes | No |
| Read Page Mode | | Yes | Yes | Yes | No |
| Read Page Size | 64 Mbit | N/A | N/A | 16 bytes | Maybe |
| | 128 Mbit | 32 bytes | 32 bytes | 32 bytes | No |
| | 256 Mbit | | | | |
| | 512 Mbit | | | | |
| | 1 Gbit | | | | |
| Write Buffer Size | 64 Mbit | N/A | N/A | 256 bytes | Maybe |
| | 128 Mbit | 1024 bytes | 1024 bytes | 512 bytes | Maybe |
| | 256 Mbit | | | | |
| | 512 Mbit | | | | |
| | 1 Gbit | | | | |
| Security | | | | | |
| Individual Sector Protection | | Yes | Yes | Yes | No |
| Secure Silicon OTP Area | 64 Mbit | N/A | N/A | 256-Byte | No |
| | 128 Mbit | 256-Byte | 256-Byte | 2 x 512-Byte | |
| | 256 Mbit | | | | |
| | 512 Mbit | | | | |
| | 1 Gbit | | | | |
| Other | | | | | |

Migration from Micron MT28E/MT28F to Infineon S29GL-S NOR Flash Family



Feature Comparison

| Products | | MT28E | MT28F | S29GL-S | Migration Issue |
|---------------------------------------|----------|-------|-------|---------|-----------------|
| 12V Accelerated Programming | 64 Mbit | N/A | N/A | Yes | N/A |
| | 128 Mbit | Yes | Yes | No | Yes |
| | 256 Mbit | | | | |
| | 512 Mbit | | | | |
| | 1 Gbit | | | | |
| Unlock Bypass Command | 64 Mbit | N/A | N/A | Yes | Yes |
| | 128 Mbit | Yes | Yes | No | |
| | 256 Mbit | | | | |
| | 512 Mbit | | | | |
| | 1 Gbit | | | | |
| Multi-Sector Erase | | No | No | No | No |
| Blank Check | | Yes | Yes | Yes | No |
| Suspend/Resume | | Yes | Yes | Yes | No |
| Device ID | | Yes | Yes | Yes | No |
| Autoselect Access | | Yes | Yes | Yes | No |
| CFI | | Yes | Yes | Yes | No |
| Status via Data Polling | | Yes | Yes | Yes | No |
| Status via Status Register | | No | Yes | Yes | Yes |
| Packaging and Ordering Options | | | | | |
| 48-pin TSOP | | No | No | Yes | N/A |
| 56-pin TSOP | | Yes | Yes | Yes | No |
| 64-ball FAA BGA 10 x 13 mm | | No | No | No | No |
| 64-ball LAA BGA 11 x 13 mm | | Yes | Yes | Yes | No |
| 64-ball LAE BGA 9 x 9 mm | | No | No | Yes | No |
| 56-ball VBU BGA 9 x 7 mm | | Yes | Yes | Yes | No |

Note:

1. Migration issue means software changes or timing setting adjustment that may need to be made. It does not mean that migration is not possible.

2.1 Density

MT28E/MT28F family is available in 128-, 256-, 512-, 1024-, and 2048-Mbit densities. S29GL-S family is available in monolithic 64-, 128-, 256-, 512- and 1024-Mbit densities and 2048-Mbit dual die stack.

2.2 Sector Architecture

S29GL064S has 64-KB uniform sectors and 8-KB boot sectors. Higher density S29GL-S devices and MT28E/MT28F families have 128-KB uniform sectors. No software modifications are required to operate block erase when migrating to a higher-density device; however, modifications might be required if migration is to a lower-density device with boot sectors.

2.3 Data Bus Width

S29GL-S supports x8 and x16 data bus width. No software and hardware modifications are required to operate x8 or x16 data bus width.

2.4 Read Page Size

S29GL064S has a 16-bytes read page buffer, whereas higher-density S29GL-S and MT28E/MT28F have a 32-bytes read page buffer. No software modifications are required to operate with 32-bytes maximum page transfers supported by S29GL-S.

2.5 Write Buffer Size

MT28E/MT28F has a 1024-bytes write buffer while S29GL-S has either a 256-bytes or 512-bytes write buffer. Modifications are required if software was structured to use a 1024-bytes write buffer architecture.

2.6 Synchronous Mode

MT28E/MT28F and S29GL-S devices do not support synchronous mode operation.

2.7 Asynchronous Mode

All the devices support asynchronous mode. S29GL-S supports asynchronous single and page read modes. No software modifications are required to continue the use of an asynchronous mode supported by MT28E.

2.8 Secure Silicon OTP Area

The Secure Silicon Region (SSR) provides an extra flash memory area that can be programmed once and permanently protected from further changes i.e., it is a One Time Program (OTP) area. The SSR is 256 bytes or 1024 bytes in length depending upon the density of the device. In higher-density S29GL-S, it consists of 512 bytes for Factory Locked Secure Silicon Region and 512 bytes for Customer Locked Secure Silicon Region.

The sector address supplied during the Secure Silicon Entry command selects the Flash Memory Array sector that is overlaid by the Secure Silicon Region address map.

The SSR is overlaid starting at location 0 in the selected sector. Use of the Sector 0 address is recommended for future compatibility. While the SSR Address Space Overlay (ASO) is entered, content of all other sectors is undefined. Locations above the maximum defined address of the SSR ASO to the maximum address of the selected sector have undefined data.

2.9 Sector Protection

MT28E/MT28F supports Volatile/Nonvolatile Protection through block locking that has a method different from the S29GL-S. S29GL-S supports Advanced Sector Protection (ASP) program and erase protection via password, non-volatile and volatile control. Details of ASP program and erase protection implementations can be found in S29GL-S datasheets.

2.10 Program Erase Suspend and Resume

MT28E/MT28F supports program erase suspend and resume in the same way as S29GL-S.

2.11 Data Polling

MT28E/MT28F and S29GL-S support data polling. These are referred to as DQ bits as they appear on the data bus during a read access while an embedded algorithm is in progress. DQ bits 15 to 8, DQ4, and DQ0 are reserved and provide undefined data. Status monitoring software must mask the reserved bits and treat them as don't care.

Note that data polling may not be supported on future smaller-process MirrorBit GL flash families. Status Register reads will be required to determine the status of embedded program and erase operations if data polling is not supported.

2.12 Accelerated Programming

MT28E/MT28F and S29GL064S support accelerated programming. However, higher-density S29GL-S parts do not support accelerated programming. See the S29GL-S datasheet.

3 Package Comparison

There are different pinouts and ballouts between MT28E/MT28F and S29GL-S regarding TSOP and BGA, as shown in [Figure 1](#) through [Figure 10](#).

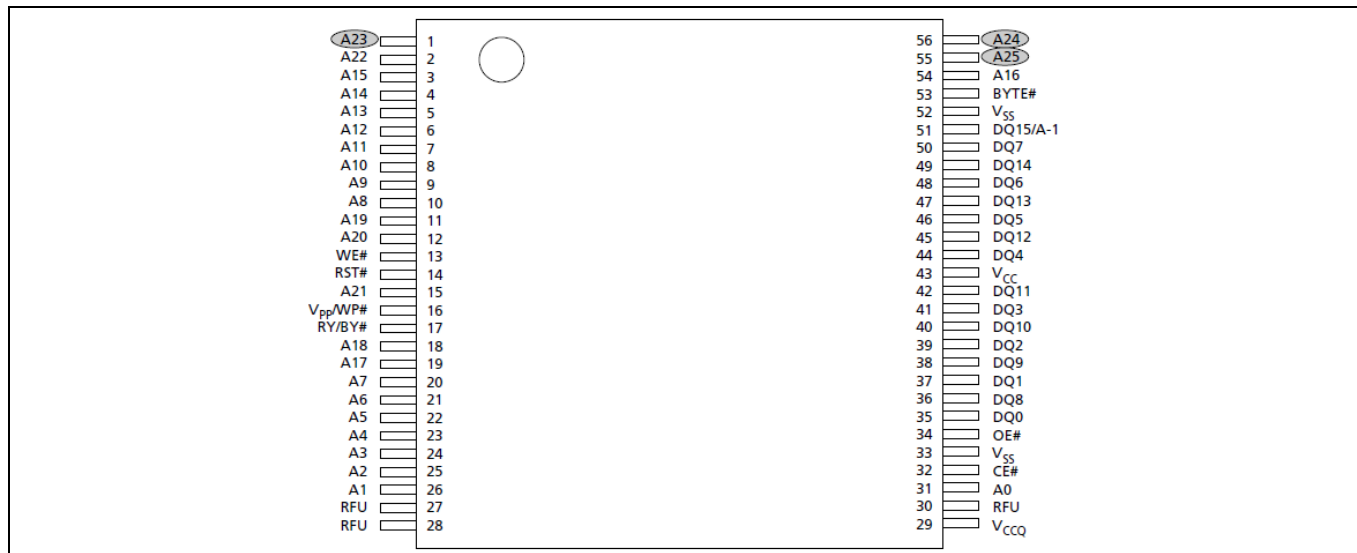


Figure 1 MT28E 56-Lead TSOP

Note:

1. A1 is the least significant address bit in x8 mode.
2. A23 is valid for 256 Mb and above; otherwise, it is RFU.
3. A24 is valid for 512 Mb and above; otherwise, it is RFU.
4. A25 is valid for 1 Gb and above; otherwise, it is RFU.

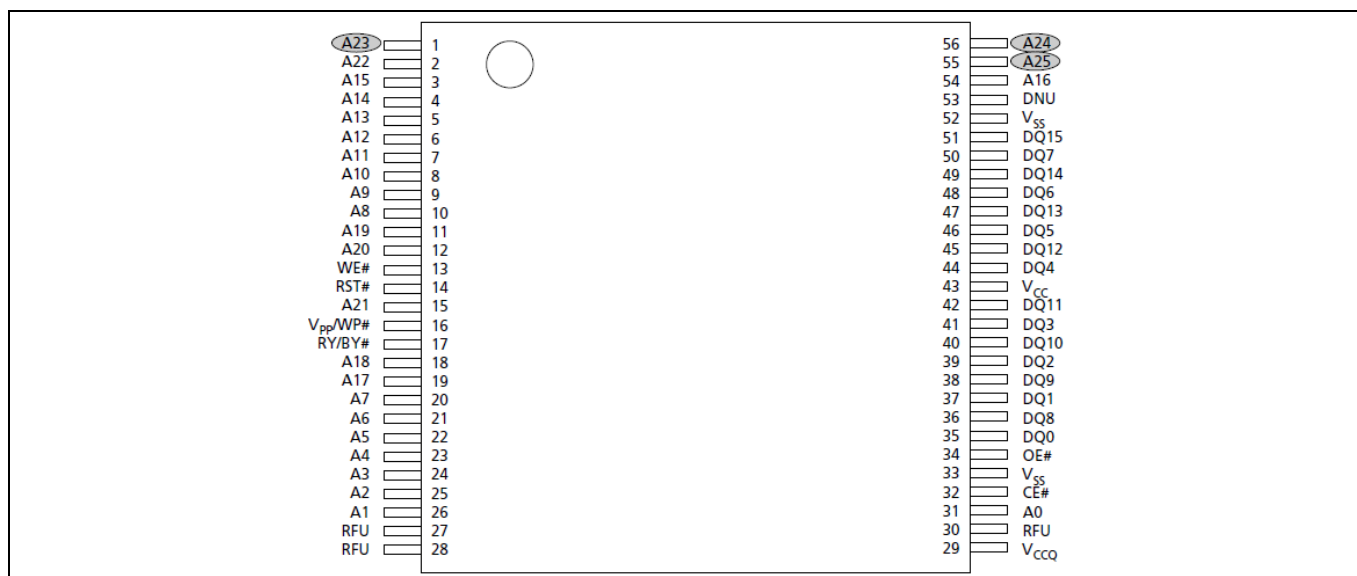


Figure 2 MT28F 56-Lead TSOP

Migration from Micron MT28E/MT28F to Infineon S29GL-S NOR Flash Family



Package Comparison

Note:

1. A23 is valid for 256 Mb and above; otherwise, it is RFU.
2. A24 is valid for 512 Mb and above; otherwise, it is RFU.
3. A25 is valid for 1 Gb and above; otherwise, it is RFU.

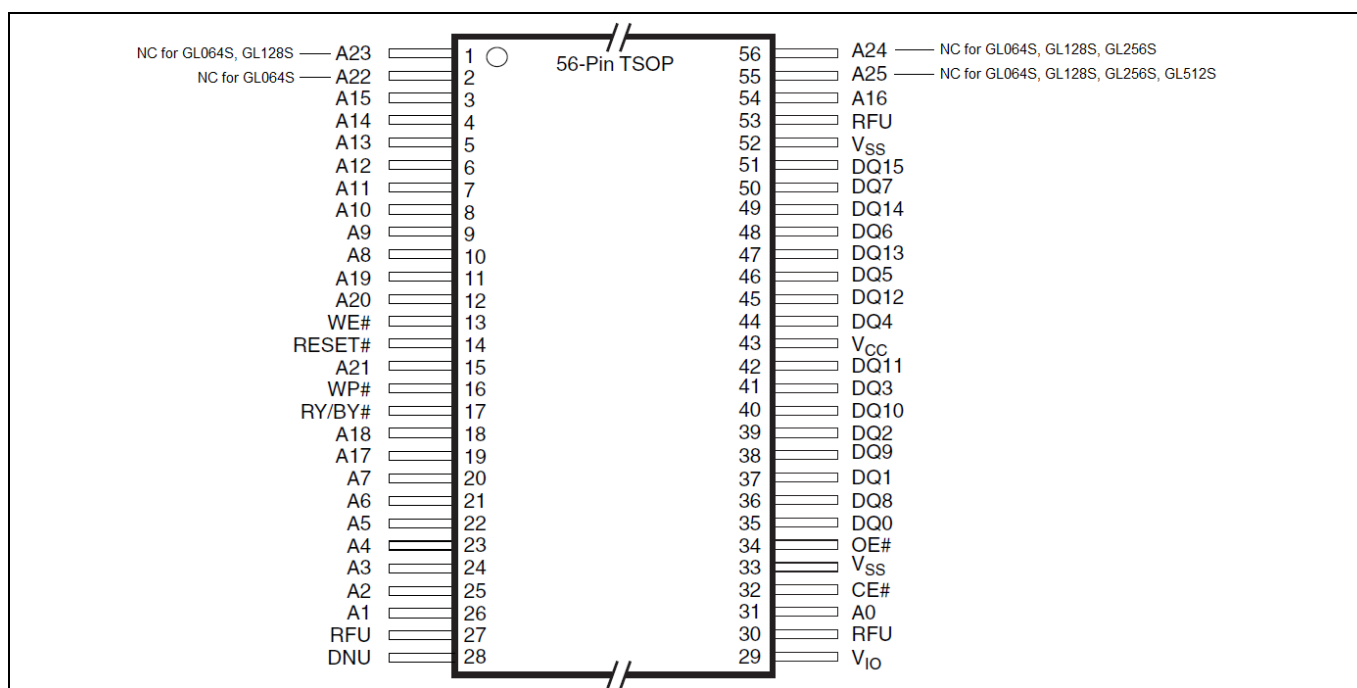


Figure 3 S29GL-S 56-Lead TSOP

Note:

1. Pin 27, 28, and 30 are Reserved for Future Use (RFU).

Package Comparison

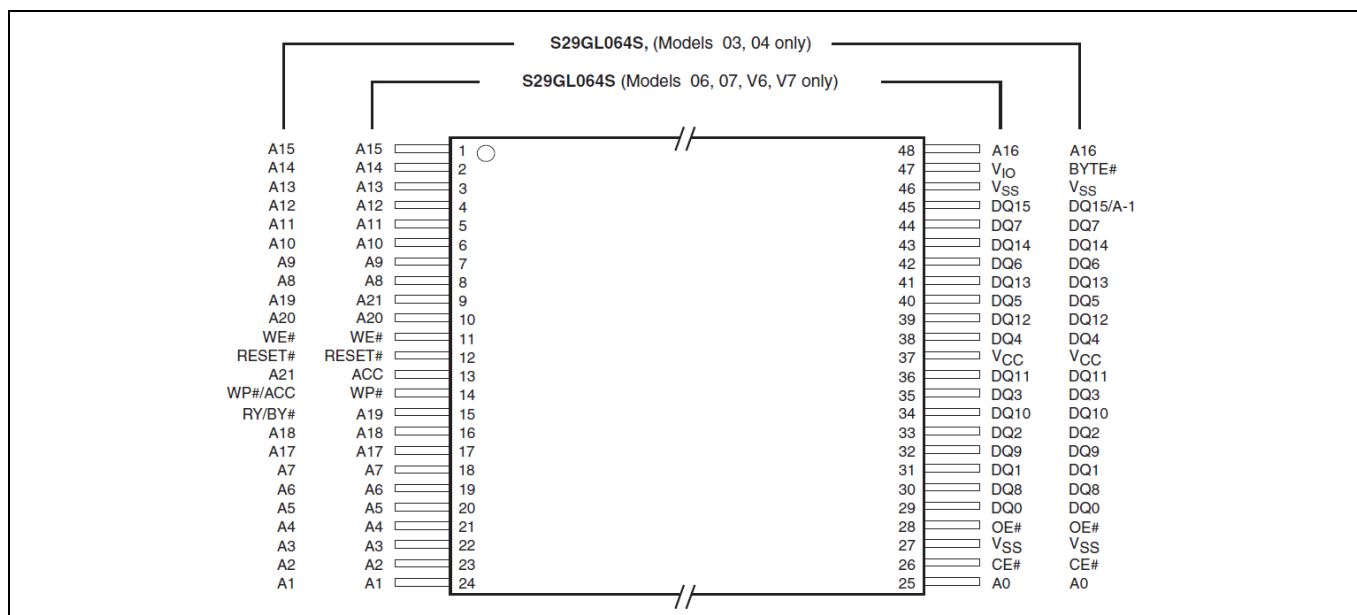


Figure 4 S29GL064S 48-Lead TSOP

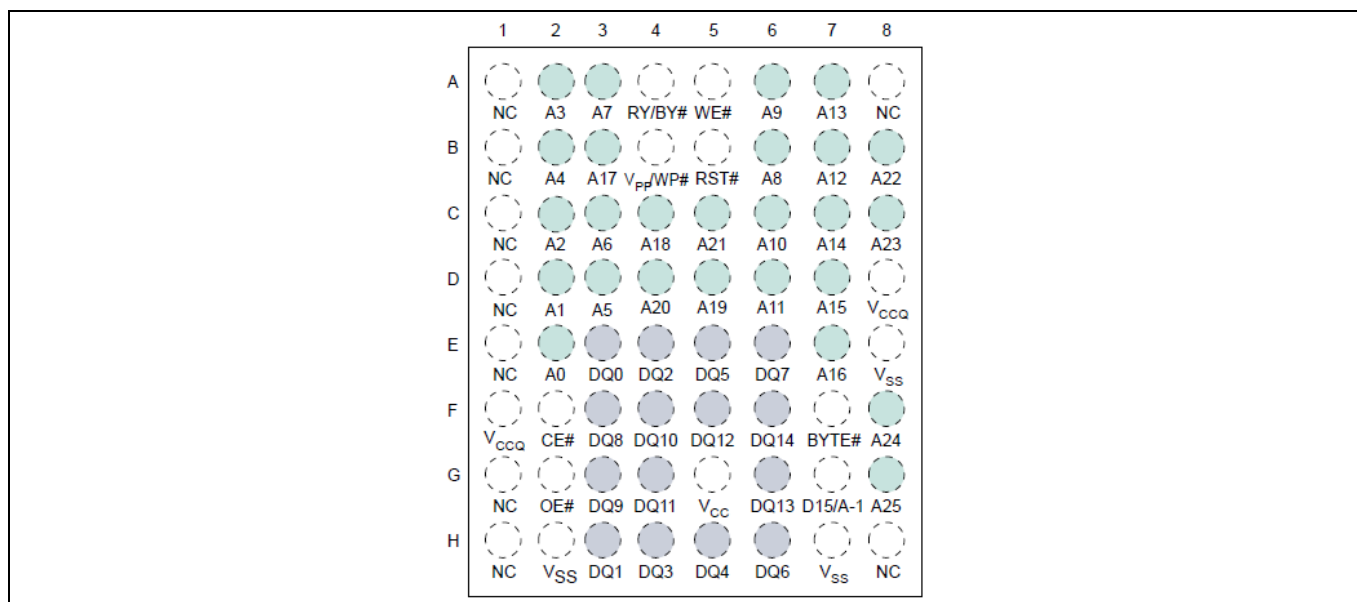


Figure 5 MT28E 64-ball Fortified BGA

Note:

1. A1 is the least significant address bit in x8 mode.
2. A23 is valid for 256 Mb and above; otherwise, it is RFU.
3. A24 is valid for 512 Mb and above; otherwise, it is RFU.
4. A25 is valid for 1 Gb and above; otherwise, it is RFU.

Package Comparison

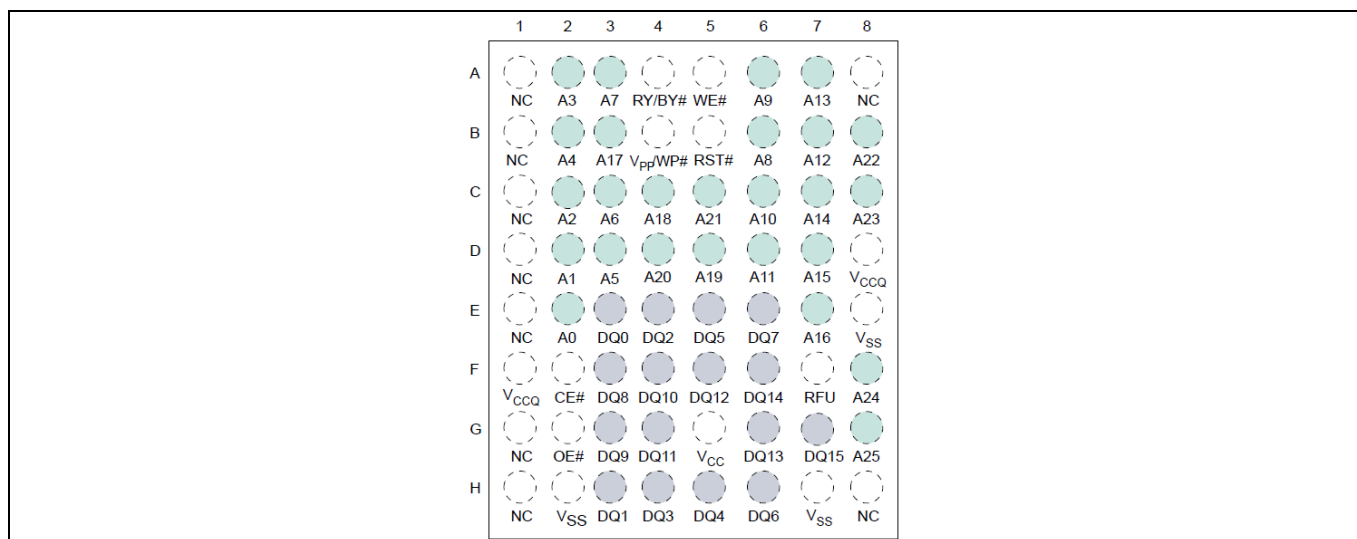


Figure 6 MT28F 64-ball Fortified BGA

Note:

1. A23 is valid for 256 Mb and above; otherwise, it is RFU.
2. A24 is valid for 512 Mb and above; otherwise, it is RFU.
3. A25 is valid for 1 Gb and above; otherwise, it is RFU.

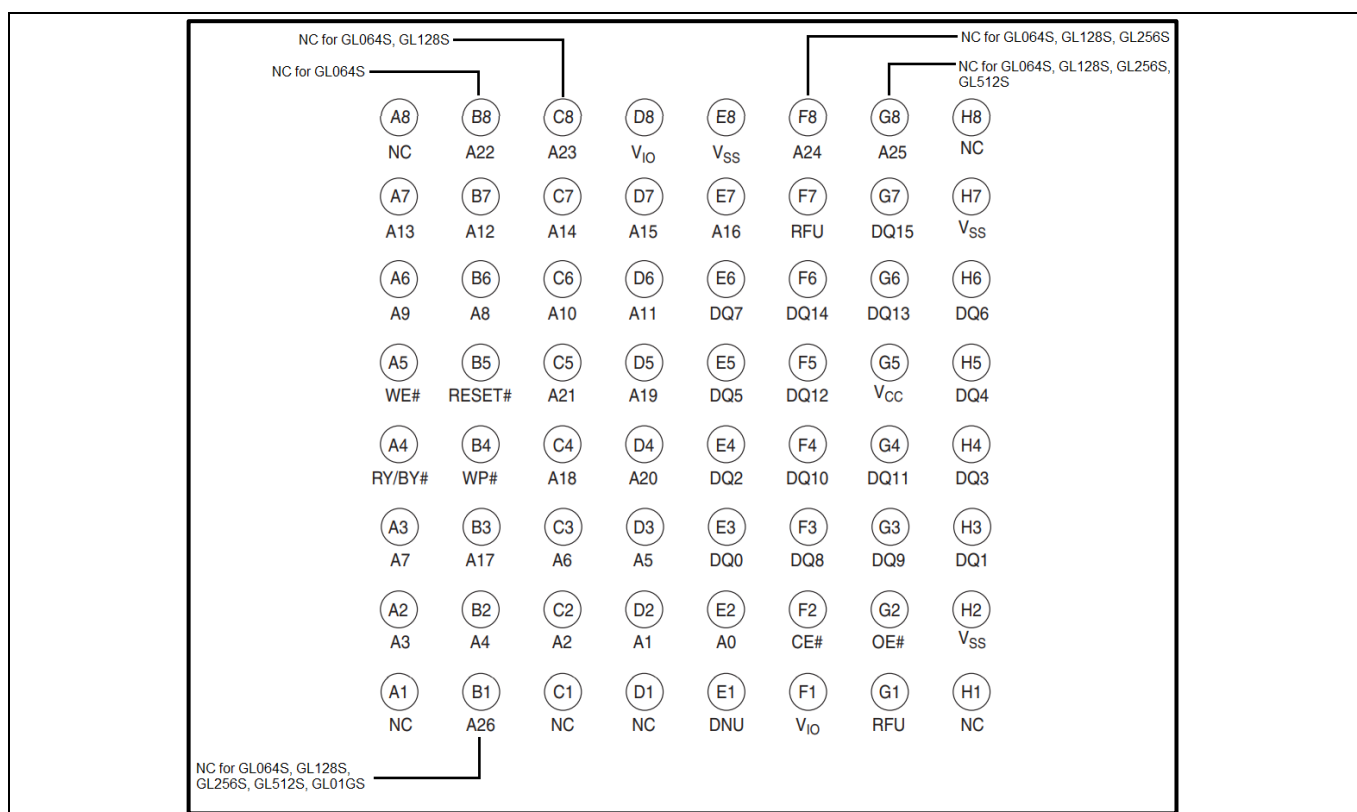


Figure 7 S29GL-S 64-Ball Fortified BGA

Migration from Micron MT28E/MT28F to Infineon S29GL-S NOR Flash Family



Package Comparison

Note:

1. Balls A1, A8, C1, D1, H1 and H8 No Connect (NC).
2. Balls F7 and G1 Reserved for Future Use (RFU).
3. Ball E1, Do Not Use (DNU).

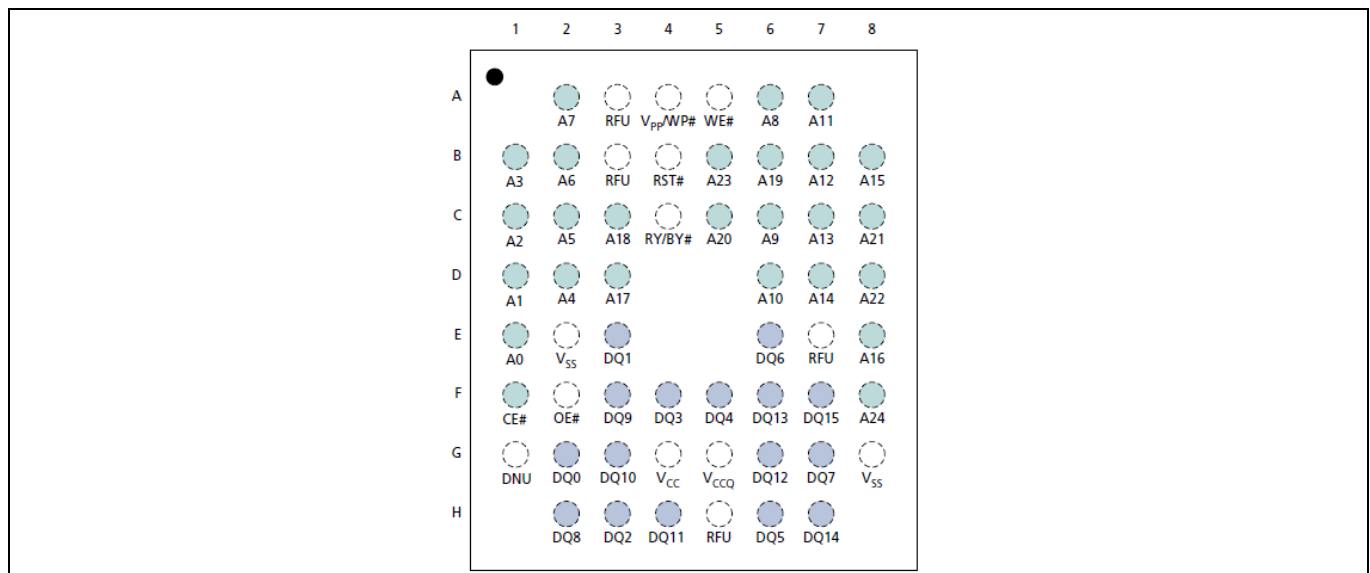


Figure 8 MT28E 56-ball Fortified BGA

Note:

1. A1 is the least significant address bit in x8 mode.
2. A23 is valid for 256 Mb and above; otherwise, it is RFU.
3. A24 is valid for 512 Mb and above; otherwise, it is RFU.
4. A25 is valid for 1 Gb and above; otherwise, it is RFU.

Package Comparison

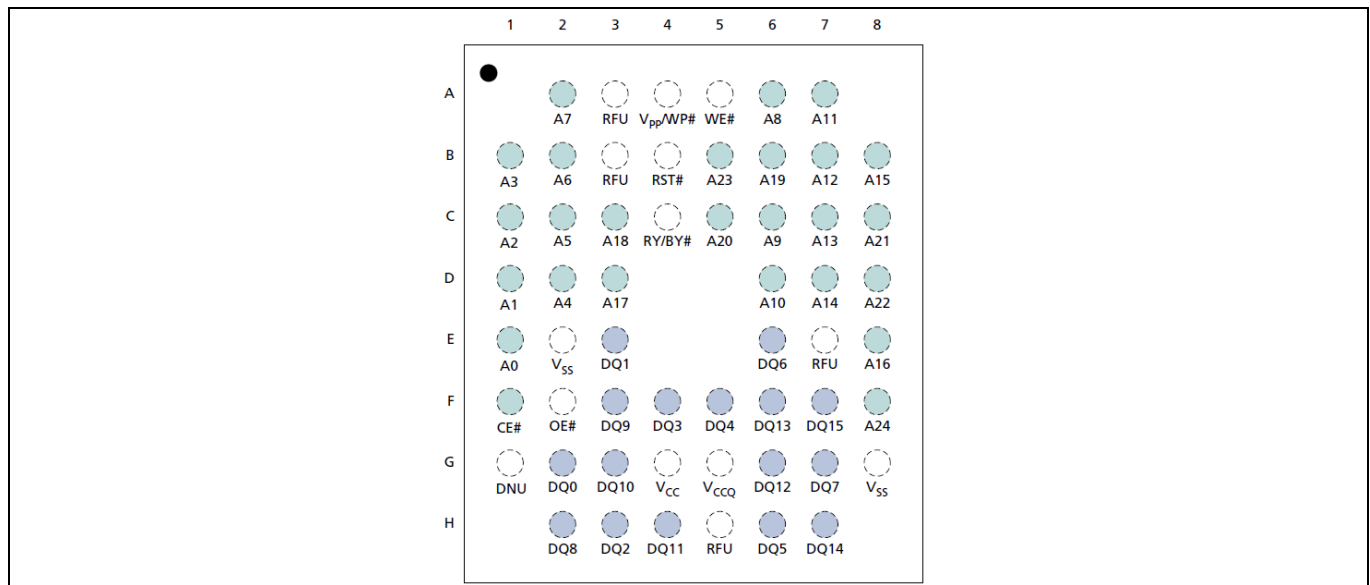


Figure 9 MT28F 56-ball Fortified BGA

Note:

1. A23 is valid for 256 Mb and above; otherwise, it is RFU.
2. A24 is valid for 512 Mb and above; otherwise, it is RFU.

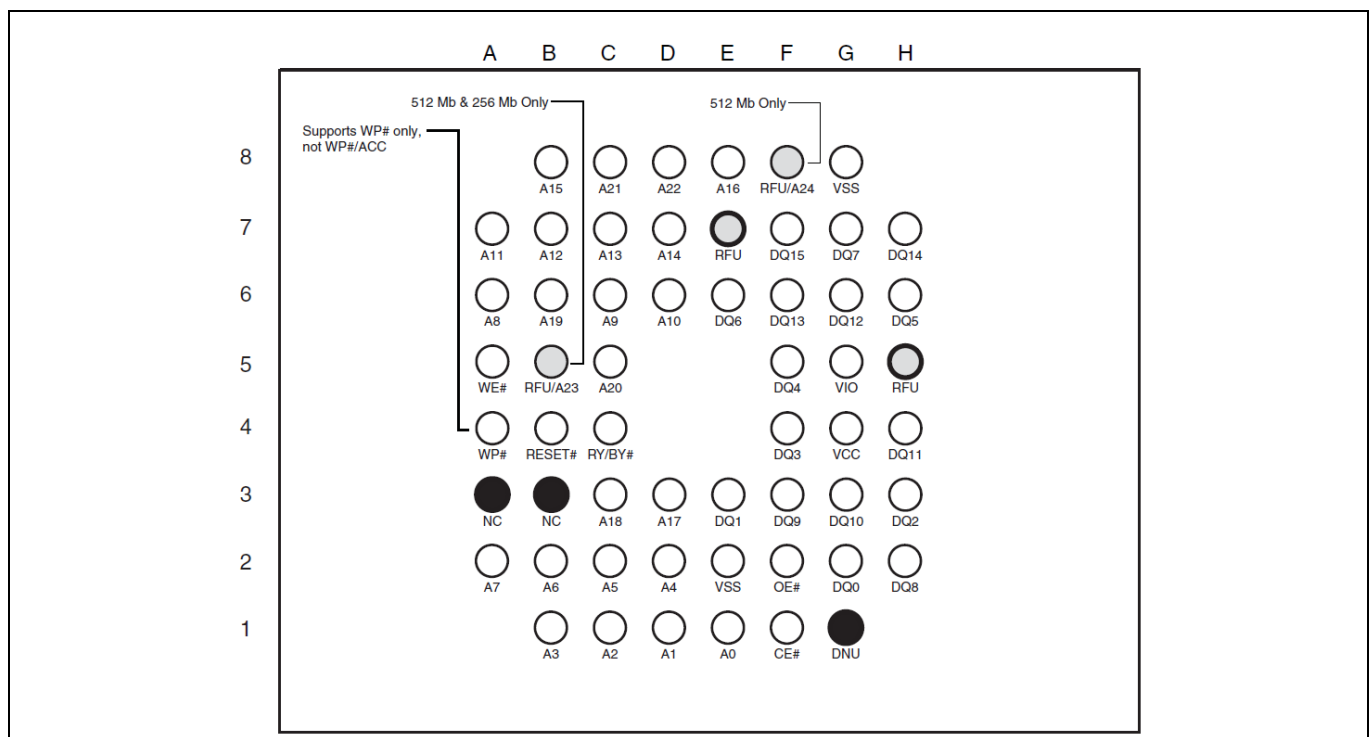


Figure 10 S29GL-S 56-Ball Fortified BGA

Migration from Micron MT28E/MT28F to Infineon S29GL-S NOR Flash Family



Package Comparison

Note:

1. Balls G1 is DNU.
2. Ball E7, F8 and H5 are RFU.
3. Ball A3 and B3 are NC.

4 Signal Comparison

Table 2 shows a signal comparison summary of Infineon S29GL-S to MT28E/MT28F.

Table 2 Signal Comparison

| MT28E/MT28F | | S29GL-S | |
|----------------------|--|----------------------|---|
| Symbol | Description | Symbol | Description |
| RESET# | Hardware Reset | RESET# | Hardware Reset |
| CE# | Chip Enable | CE# | Chip Enable |
| OE# | Output Enable | OE# | Output Enable |
| WE# | Write Enable | WE# | Write Enable |
| A _{MAX} -A0 | Address inputs. A26-A0 for 2048 Mbit A25-A0 for 1024 Mbit A24-A0 for 512 Mbit A23-A0 for 256 Mbit A22-A0 for 128 Mbit | A _{MAX} -A0 | Address inputs: A26-A0 S70GL02GS A25-A0 for S29GL01GS A24-A0 for S29GL512S A23-A0 for S29GL256S A22-A0 for S29GL128S A21-A0 for S29GL064S |
| DQ15-DQ0 | Data inputs and outputs | DQ15-DQ0 | Data inputs and outputs |
| V _{PP} /WP# | V _{PP} /Write Protect | WP# | Write Protect |
| BYTE# | Selects data bus width | BYTE# | Selects data bus width |
| RY/BY# | Ready/Busy | RY/BY# | Ready/Busy |
| V _{CC} | Supply voltage | V _{CC} | Core power supply |
| V _{CCQ} | I/O supply voltage | V _{IO} | Versatile I/O power supply |
| V _{SS} | Ground | V _{SS} | Power supplies ground |
| NC | Not Connected internally | NC | Not Connected internally |
| RFU | Reserved for Future Use | RFU | Reserved for Future Use |
| DNU | Do Not Use | DNU | Do Not Use |

5 Command Set Comparison

MT28E/MT28F and S29GL-S device commands vary from one to seven bus cycles, as shown in [Table 3](#) and [Table 4](#).

Table 3 Table. MT28E/MT28F Command Set (x16)

| Command and Code/Subcode | Cycles | Address and Data Cycles | | | | | | | | | | | | Notes |
|---------------------------------------|--------|-------------------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|----|---------|
| | | 1 st | | 2 nd | | 3 rd | | 4 th | | 5 th | | 6 th | | |
| | | A | D | A | D | A | D | A | D | A | D | A | D | |
| Read and Autoselect Operations | | | | | | | | | | | | | | |
| Read/Reset | 1 | X | F0 | | | | | | | | | | | 2 |
| | 3 | 555 | AA | 2AA | 55 | X | F0 | | | | | | | |
| Read CFI | 1 | 555 | 98 | | | | | | | | | | | |
| Exit Read CFI | 1 | X | F0 | | | | | | | | | | | |
| Autoselect | 4 | 555 | AA | 2AA | 55 | 555 | 90 | *3 | *3 | | | | | 4, 5 |
| Exit Autoselect | 1 | X | F0 | | | | | | | | | | | |
| Bypass Operations | | | | | | | | | | | | | | |
| Unlock Bypass | 3 | 555 | AA | 2AA | 55 | 555 | 20 | | | | | | | |
| Unlock Bypass Reset | 2 | X | 90 | X | 00 | | | | | | | | | |
| Program Operations | | | | | | | | | | | | | | |
| Program | 4 | 555 | AA | 2AA | 55 | 555 | A0 | PA | PD | | | | | |
| Unlock Bypass Program | 2 | X | A0 | PA | PD | | | | | | | | | 6 |
| Write to Buffer Program | 5 | 555 | AA | 2AA | 55 | BAd | 25 | BAd | N | PA | PD | | | 7, 8, 9 |
| Unlock Bypass Write to Buffer Program | 3 | BAd | 25 | BAd | N | PA | PD | | | | | | | 6 |
| Write to Buffer Program Confirm | 1 | BAd | 29 | | | | | | | | | | | 7 |
| Program Suspend | 1 | X | B0 | | | | | | | | | | | |
| Program Resume | 1 | X | 30 | | | | | | | | | | | |
| Erase Operations | | | | | | | | | | | | | | |
| Chip Erase | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | 555 | 10 | |
| Unlock Bypass Chip Erase | 2 | X | 80 | X | 10 | | | | | | | | | 6 |
| Block Erase | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | BAd | 30 | 10 |
| Unlock Bypass Block Erase | 2 | X | 80 | BAd | 30 | | | | | | | | | 6 |
| Erase Suspend | 1 | X | B0 | | | | | | | | | | | |

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Command Set Comparison

| Command and Code/Subcode | Cycles | Address and Data Cycles | | | | | | | | | | | | Notes |
|------------------------------|--------|-------------------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|----|-------|
| | | 1 st | | 2 nd | | 3 rd | | 4 th | | 5 th | | 6 th | | |
| | | A | D | A | D | A | D | A | D | A | D | A | D | |
| Erase Resume | 1 | X | 30 | | | | | | | | | | | |
| Blank Check Operations | | | | | | | | | | | | | | |
| Blank Check Setup | 6 | 555 | AA | 2AA | 55 | BAd | EB | BAd | 76 | BAd | 00 | BAd | 00 | |
| Blank Check Confirm and Read | 1 | BAd + 00 | 29 | | | | | | | | | | | |

Note:

1. A = Address; D = Data; X = Don't Care; BAd = Any address in the block; N = Number of bytes (x8) or words (x16) to be programmed; PA = Program Address; PD = Program Data; Gray shading = Not applicable. All values in the table are hexadecimal. Some commands require both a command code and subcode.
2. A full three-cycle Reset command sequence must be used to reset the device in the event of a Buffered Program Abort error (DQ1 = 1).
3. These cells represent read cycles (versus write cycles for the others).
4. Autoselect enables the device to read the Device ID, block protection status, and extended memory block protection indicator.
5. Autoselect addresses and data are specified in [Table 5](#).
6. For any Unlock Bypass Erase/Program command, the first two Unlock cycles are unnecessary.
7. BAd must be the same as the address loaded during the Write-to-Buffer Program 3rd and 4th cycles.
8. Write-to-Buffer Program operation: maximum cycles = 261 (x8) and 517 (x16). Unlock Bypass Write-to-Buffer Program operation: maximum cycles = 259 (x8), 515 (x16). Write-to-Buffer Program operation: N + 1 = bytes (x8) or words (x16) to be programmed; maximum buffer size = 256 bytes (x8) and 512 words (x16).
9. For x8, A[*MAX*:7] address pins should remain unchanged while A[6:0] and A-1 pins are used to select a byte within the N + 1 byte page. For x16, A[*MAX*:9] address pins should remain unchanged while A[8:0] pins are used to select a word within the N+1 word page.
10. Block Erase address cycles can extend beyond six address-data cycles, depending on the number of blocks to erase.

Table 4 S29GL-S Major Command Set (x16)

| Command Sequence ^{*1} | Cycles | Address and Data Cycles | | | | | | | | | | | |
|-----------------------------------|--------|-------------------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|----|
| | | 1 st | | 2 nd | | 3 rd | | 4 th | | 5 th | | 6 th | |
| | | A | D | A | D | A | D | A | D | A | D | A | D |
| Read ^{*6} | 1 | RA | RD | | | | | | | | | | |
| Reset/ASO Exit ^{*7, *17} | 1 | XXX | F0 | | | | | | | | | | |
| Status Register Read | 2 | 555 | 70 | XXX | RD | | | | | | | | |
| Status Register Clear | 1 | 555 | 71 | | | | | | | | | | |
| Word Program | 4 | 555 | AA | 2AA | 55 | 555 | A0 | PA | PD | | | | |
| Write to Buffer | 6 | 555 | AA | 2AA | 55 | SA | 25 | SA | WC | WBL | PD | WBL | PD |
| Program Buffer to Flash | 1 | SA | 29 | | | | | | | | | | |

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Command Set Comparison

| Command Sequence ^{*1} | Cycles | Address and Data Cycles | | | | | | | | | | | |
|--|--------|-------------------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|----|
| | | 1 st | | 2 nd | | 3 rd | | 4 th | | 5 th | | 6 th | |
| | | A | D | A | D | A | D | A | D | A | D | A | D |
| Write-to-Buffer-Abort Reset ^{*13} | 3 | 555 | AA | 2AA | 55 | 555 | F0 | | | | | | |
| Chip Erase | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | 555 | 10 |
| Sector Erase | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | SA | 30 |
| Erase Suspend/Program Suspend Legacy Method ^{*11} | 1 | XXX | B0 | | | | | | | | | | |
| Erase Suspend Enhanced Method | 1 | XXX | B0 | | | | | | | | | | |
| Erase Resume/Program Resume Legacy Method ^{*12} | 1 | XXX | 30 | | | | | | | | | | |
| Erase Resume Enhanced Method | 1 | XXX | 30 | | | | | | | | | | |
| Program Suspend Enhanced Method | 1 | XXX | 51 | | | | | | | | | | |
| Program Resume Enhanced Method | 1 | XXX | 50 | | | | | | | | | | |
| Blank Check | 1 | (SA) 55 | 33 | | | | | | | | | | |

Unlock Bypass

| | | | | | | | | | | | | | |
|--|---|-----|----|-----|----|-----|----|-----|----|--|--|--|--|
| Enter | 3 | 555 | AA | 2AA | 55 | 555 | 20 | | | | | | |
| Program ^{*9} | 2 | XXX | A0 | PA | PD | | | | | | | | |
| Write-to-Buffer ^{*9} | 4 | SA | 25 | SA | WC | WBL | PD | WBL | PD | | | | |
| Program Buffer to Flash (Confirm) | 1 | SA | 29 | | | | | | | | | | |
| Write-to-Buffer-Abort Reset ^{*13} | 3 | 555 | AA | 2AA | 55 | 555 | F0 | | | | | | |
| Sector Erase ^{*9} | 2 | XXX | 80 | SA | 30 | | | | | | | | |
| Chip Erase ^{*9} | 2 | XXX | 80 | XXX | 10 | | | | | | | | |
| Command Set Exit ^{*10} | 2 | XXX | 90 | XXX | 00 | | | | | | | | |

ID-CFI (Autoselect) ASO

| | | | | | | | | | | | | | |
|-----------------------------------|---|------------|----|-----|----|-------------|----|--|--|--|--|--|--|
| ID (Autoselect) Entry | 3 | 555 | AA | 2AA | 55 | (SA) 555 | 90 | | | | | | |
| CFI Enter ^{*8} | 1 | (SA) 55 | 98 | | | | | | | | | | |
| ID-CFI Read | 1 | RA | RD | | | | | | | | | | |
| Reset/ASO Exit ^{*7, *18} | 1 | XXX | F0 | | | | | | | | | | |

Command Set Comparison

Legend:

X = Don't care.

RA = Address of the memory to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed.

PD = Data to be programmed at location PA.

SA = Address of the sector selected. Address bits Amax-A16 uniquely select any sector.

WBL = Write Buffer Location. The address must be within the same Line.

WC = Word Count is the number of write buffer locations to load minus 1.

PWAx = PPB Password address for Word 0 = 00h, Word 1 = 01h, Word 2 = 02h, and Word 3 = 03h. SSR3 Password address for Word 0 = 10h, Word 1 = 11h, Word 2 = 12h, and Word 3 = 13h.

PWDx = Password data Word 0, Word 1, Word 2, and Word 3.

Gray vs. White Box = Read vs. Write Operation.

Note:

1. See *Interface Status* for description of bus operations in the S29GL-S datasheet.
2. All values are in hexadecimal.
3. Except for the following, all bus cycles are write cycles: read cycle during Read, ID/CFI Read (Manufacturing ID / Device ID), Indicator Bits, Secure Silicon Region Read, SSR Lock Read, and 2nd cycle of Status Register Read.
4. Data bits DQ15-DQ8 are don't care in command sequences, except for RD, PD, WC and PWD.
5. Address bits Amax-A11 are don't care for unlock and command cycles, unless SA or PA required. (Amax is the highest address pin.).
6. No unlock or command cycles required when reading array data.
7. The Reset command is required to return to reading the array data when the device is in the ASO mode, or if DQ5 goes HIGH (while the device is providing the status data).
8. The command is valid when the device is ready to read array data.
9. The Unlock-Bypass command is required prior to the Unlock-Bypass-Program and the Unlock-Bypass-Write to buffer commands.
10. The Unlock-Bypass-Reset command is required to return to reading the array data when the device is in the Unlock-Bypass mode.
11. The system can read and program/program suspend in non-erasing sectors, or enter the ID-CFI ASO, when in the Erase Suspend mode. The Erase Suspend command is valid only during a Sector Erase operation.
12. The Erase Resume/Program Resume command is valid only during Erase Suspend/Program Suspend modes.
13. Issue this command sequence to return to Read State after detecting device is in a Write-to-Buffer-Abort state. **IMPORTANT:** The full command sequence is required if resetting out of ABORT.
14. The Exit command returns the device to reading the array.
15. The password portion can be entered or read in any order if the entire 64-bit password is entered or read. Addresses are 10h-13h if the SSR3 is being accessed.
16. For PWDx, only one portion of the password can be programmed per each A0 command. Portions of the password must be programmed in sequential order (PWD0 - PWD3).

Command Set Comparison

17. *All Lock Register bits are one-time programmable. The program state = 0 and the erase state = 1. Also, both the Persistent Protection Mode Lock Bit and the Password Protection Mode Lock Bit cannot be programmed at the same time; the Lock Register Bits Program operation halts and returns the device to Read State if you attempt this. Lock Register Bits that are reserved for future use are undefined.*
18. *If any of the Entry commands was issued, an Exit command must be issued to reset the device into Read State.*
19. *Protected State = 00h, Unprotected State = 01h. The sector address for DYB set, DYB clear, or PPB Program command may be any location within the sector - the lower order bits of the sector address are don't care.*

6 Device ID Comparison

This section provides a comparison between Micron MT28E/MT28F and Infineon S29GL-S flash memory Device ID.

Table 5 Device ID Comparison

| | | | Infineon | Micron | |
|-----------------|--------|---------------|-----------|----------------|----------------|
| | | Address (x16) | S29GL02S | | MT28F 2 Gbit |
| Manufacturer ID | | (Base)+00h | 0001h | | 0089h |
| Device ID | Word 1 | (Base)+01h | 227Eh | | 227Eh |
| | Word 2 | (Base)+0Eh | 2248h | | 2248h |
| | Word 3 | (Base)+0Fh | 2201h | | 2201h |
| | | | Infineon | Micron | |
| | | Address (x16) | S29GL01GS | MT28E 1 Gbit | MT28F 1 Gbit |
| Manufacturer ID | | (Base)+00h | 0001h | 0089h | 0089h |
| Device ID | Word 1 | (Base)+01h | 227Eh | 227Eh | 227Eh |
| | Word 2 | (Base)+0Eh | 2228h | 2228h | 2228h |
| | Word 3 | (Base)+0Fh | 2201h | 2201h | 2201h |
| | | | Infineon | Micron | |
| | | Address (x16) | S29GL512S | MT28E 512 Mbit | MT28F 512 Mbit |
| Manufacturer ID | | (Base)+00h | 0001h | 0089h | 0089h |
| Device ID | Word 1 | (Base)+01h | 227Eh | 227Eh | 227Eh |
| | Word 2 | (Base)+0Eh | 2223h | 2223h | 2223h |
| | Word 3 | (Base)+0Fh | 2201h | 2201h | 2201h |
| | | | Infineon | Micron | |
| | | Address (x16) | S29GL256S | MT28E 256 Mbit | |
| Manufacturer ID | | (Base)+00h | 0001h | 0089h | |
| Device ID | Word 1 | (Base)+01h | 227Eh | 227Eh | |
| | Word 2 | (Base)+0Eh | 2222h | 2222h | |
| | Word 3 | (Base)+0Fh | 2201h | 2201h | |
| | | | Infineon | Micron | |
| | | Address (x16) | S29GL128S | MT28E 128 Mbit | |
| Manufacturer ID | | (Base)+00h | 0001h | 0089h | |
| Device ID | Word 1 | (Base)+01h | 227Eh | 227Eh | |
| | Word 2 | (Base)+0Eh | 2221h | 2221h | |
| | Word 3 | (Base)+0Fh | 2201h | 2201h | |

Migration from Micron MT28E/MT28F to Infineon S29GL-S NOR Flash Family



Device ID Comparison

| | | | | Infineon | Micron | |
|-----------------|--------|---------------|--------------|---|--------|--|
| | | Address (x16) | Address (x8) | S29GL064S | | |
| Manufacturer ID | | (Base)+00h | (Base)+00h | 0001h | | |
| Device ID | Word 1 | (Base)+01h | (Base)+02h | 227Eh | | |
| | Word 2 | (Base)+0Eh | (Base)+1Ch | 220Ch (Model Number 01, 02, V1, V2) 2210h (Model Number 03, 04) 2213h (Model Number 06, 07, V6, V7) | | |
| | Word 3 | (Base)+0Fh | (Base)+1Eh | 2201h (Model Number 01, 02, V1, V2) 2200h (Model Number 04, bottom boot) 2201h (Model Number 03, top boot) 2201h (Model Number 06, 07, V6, V7) | | |

7 Status Register Comparison

MT28F supports Status Register reads as an alternative method to data polling to determine the embedded operation status. The Status Register feature is also supported on S29GL-S family. The 16-bit Status Register is accessed via a two-cycle sequence consisting of a Read Status Register Command write cycle followed immediately by a read cycle to the same targeted sector address. Using the Status Register is advantageous because, unlike legacy data polling, software does not need to track active address regions or compare sequential polling read values to determine embedded algorithm status; one Status Register access provides all the information necessary to determine the flash state. A Clear Status Register command is available to reset the last completed embedded operation portion of the Status Register.

Status Register usage is optional. If required, software can be modified to take advantage of this feature by querying the Lower Software Bits at offset 000Ch in Autoselect mode. If Bit 0 is set, the Status Register functionality is supported. Details of the Status Register implementation are provided in the S29GL-S datasheet. MT28E does not support the Status Register functionality.

The Status Register contains bits related to the results – success or failure – of the most recently completed Embedded Algorithms (EA) and bits related to the current state of any EA in process:

- Erase Status (Bit 5)
- Program Status (Bit 4)
- Write Buffer Abort (Bit 3)
- Sector Locked Status (Bit 1)
- RFU (Bit 0)

Current State of EA in Process:

- Device Busy (Bit 7)
- Erase Suspended (Bit 6)
- Program Suspended (Bit 2)

The Current State bits indicate whether an EA is in process, suspended, or completed. The upper eight bits (Bits 15:8) are reserved. These have undefined HIGH or LOW value that can change from one status read to another. These bits should be treated as don't care and ignored by any software reading status. The Soft Reset Command will clear bits [5, 4, 1, 0] to '0' of the status register if Status Register Bit 3 = 0. This will not affect the Current State bits. The Clear Status Register Command will clear the results related bits of the status register to '0' but will not affect the Current State bits.

Table 6 MT28E/MT28F Data Polling Register

| Bit | Name | Settings | Description | Note |
|-----|------------------|------------------------------------|--|---------|
| DQ7 | Data Polling Bit | 0 or 1, depending on operations | Monitors whether the program/erase has successfully completed its operation, or has responded to an Erase Suspend operation. | 2, 4 |
| DQ6 | Toggle Bit | Toggles: 0 to 1; 1 to 0; and so on | Monitors whether the program, erase, or blank check has successfully completed its operations, or has responded to an Erase Suspend operation. During a Program/Erase/Blank Check operation, DQ6 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from any address. | 3, 4, 5 |
| DQ5 | Error Bit | 0 = Success 1 = Failure | Identifies errors detected by the program/erase. DQ5 is set when a Program, Block Erase, or Chip Erase | 4, 6 |

Migration from Micron MT28E/MT28F to Infineon S29GL-S NOR Flash Family



Status Register Comparison

| Bit | Name | Settings | Description | Note |
|-----|----------------------------|--|--|------|
| | | | operation fails to write the correct data to the memory, or when a Blank Check or CRC operation fails. | |
| DQ3 | Erase Timer Bit | 0 = Erase not in progress 1 = Erase in progress | Identifies the start of program/erase operation during a Block Erase command. Before the program/erase controller starts, this bit set to 0, and additional blocks to be erased can be written to the command interface. | 4 |
| DQ2 | Alternative Toggle Bit | Toggles: 0 to 1; 1 to 0; and so on | During Chip Erase, Block Erase, and Erase Suspend operations, DQ2 toggles from 0 to 1, 1 to 0, and so on, with each successive Read operation from addresses within the blocks being erased. | 3, 4 |
| DQ1 | Buffered Program Abort Bit | 1 = Abort | Indicates a Buffer Program, EFI Blank Check, or CRC operation abort. The Buffered Program Abort and Reset command must be issued to return the device to read mode. | |

Note:

1. The data polling register can be read during Program, Erase, or Erase Suspend operations; the Read operation outputs data on DQ[7:0].
2. For a Program operation in progress, DQ7 outputs the complement of the bit being programmed. For a Read operation from the address previously programmed successfully, DQ7 outputs existing DQ7 data. For a Read operation from addresses with blocks to be erased while an Erase Suspend operation is in progress, DQ7 outputs 0; upon successful completion of the Erase Suspend operation, DQ7 outputs 1. For an Erase operation in progress, DQ7 outputs 0; upon Erase operation's successful completion, DQ7 outputs 1. During a Buffer Program operation, the data polling bit is valid only for the last word being programmed in the write buffer.
3. After successful completion of a Program, Erase, or Blank Check operation, the device returns to read mode.
4. During Erase Suspend mode, Read operations to addresses within blocks not being erased output memory array data as if in Read mode. A protected block is treated in the same way as a block not being erased.
5. During erase suspend mode, DQ6 toggles when addressing a cell within a block being erased. The toggling stops when the program/erase has suspended the Erase operation.
6. When DQ5 is set to '1', a Read/Reset (F0h) command must be issued before any subsequent command.

Table 7 S29GL-S Status Register

| Bit # | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----------|------------------|----------------------------|----------------------|------------------------|-------------------------------|------------------------------|------------------------|----------|
| Bit Description | Reserved | Device Ready Bit | Erase Suspend Status Bit | Erase Status Bit | Program Status Bit | Write Buffer Abort Status Bit | Program Suspend Status Bit | Sector Lock Status Bit | Reserved |
| Bit Name | | DRB | ESSB | ESB | PSB | WBASB | PSSB | SLSB | |
| Reset Status | X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Busy Status | Invalid | 0 | Invalid | Invalid | Invalid | Invalid | Invalid | Invalid | Invalid |
| Ready Status | X | 1 | 0 = No erase in suspension | 0 = Erase successful | 0 = Program successful | 0 = Program | 0 = No program in suspension | 0 = Sector not locked | X |

Migration from Micron MT28E/MT28F to Infineon S29GL-S NOR Flash Family



Status Register Comparison

| Bit # | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|------|---|-------------------------|----------------|------------------|---|---------------------------|---|---|
| | | | 1 = Erase in suspension | 1 = Erase fail | 1 = Program fail | not aborted 1 = Program aborted during Write to Buffer command | 1 = Program in suspension | during operation 1 = Sector locked error | |

Note:

1. Bits 15 through 8 and 0 are RFU and may display as '0' or '1'. These bits should be ignored (masked) when checking the status.
2. Bit 7 is '1' when there is no Embedded Algorithm in progress in the device.
3. Bits 6 through '1' are valid only if Bit 7 is '1'.
4. All bits are put in their reset status by a cold reset or warm reset.
5. Bits 5, 4, 3, and 1 are cleared by the Clear Status Register command or Reset command.
6. Upon issuing the Erase Suspend Command, you must continue to read the Status Register until DRB becomes '1'.
7. ESSB is cleared by the Erase Resume Command.
8. ESB reflects the success or failure of the most recent erase operation.
9. PSB reflects the success or failure of the most recent program operation.
10. During Erase Suspend, programming to the suspended sector or a sector in the queue, will be ignored and no error is reported.
11. Upon issuing the Program Suspend command, you must continue to read the Status Register until DRB becomes '1'.
12. PSSB is cleared by the Program Resume command.
13. SLSB indicates that a program or erase operation failed because the sector was locked.
14. SLSB reflects the status of the most recent program or erase operation.

8 DC Specifications

S29GL-S and MT28E have primarily compatible specifications. Differences in DC characteristics between the devices are highlighted in [Table 8](#). The potential impact of any parameter specification differences should be evaluated and validated. Refer to the respective Micron MT28E and Infineon S29GL-S datasheets to verify the latest specifications.

Table 8 DC Specifications (-40°C to +85°C)

| | | Infineon | | | Micron | | | | | |
|--|----------|----------|------------------------|-----------------------|--------|-------|---------------------|-------|-------|---------------------|
| | | S29GL-S | | | MT28E | | | MT28F | | |
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| Input Load Current | 64 Mbit | | | $\pm 2.0 \mu\text{A}$ | | | N/A | | | N/A |
| | 128 Mbit | | +0.02 μA | $\pm 1.0 \mu\text{A}$ | | | $\pm 1 \mu\text{A}$ | | | |
| | 256 Mbit | | | | | | | | | |
| | 512 Mbit | | | | | | | | | $\pm 1 \mu\text{A}$ |
| | 1 Gbit | | | | | | | | | |
| | 2 Gbit | | +0.04 μA | $\pm 2.0 \mu\text{A}$ | | | N/A | | | |
| Output Leakage Current | 64 Mbit | | +0.02 μA | $\pm 1.0 \mu\text{A}$ | | | N/A | | | N/A |
| | 128 Mbit | | +0.02 μA | $\pm 1.0 \mu\text{A}$ | | | $\pm 1 \mu\text{A}$ | | | |
| | 256 Mbit | | | | | | | | | |
| | 512 Mbit | | | | | | | | | $\pm 1 \mu\text{A}$ |
| | 1 Gbit | | | | | | | | | |
| | 2 Gbit | | $\pm 0.04 \mu\text{A}$ | $\pm 2.0 \mu\text{A}$ | | | N/A | | | |
| V _{CC} Active Read Current (5 MHz) | 64 Mbit | | 25 mA | 30 mA | | N/A | N/A | | N/A | N/A |
| | 128 Mbit | | 55 mA | 60 mA | | 26 mA | 31 mA | | | |
| | 256 Mbit | | | | | | | | | |
| | 512 Mbit | | | | | | | 26 mA | 31 mA | |
| | 1 Gbit | | | | | | | | | |
| | 2 Gbit | | | | | N/A | N/A | | | |
| V _{CC} Intra-Page Read Current | 64 Mbit | | 7.5 mA | 20 mA | | N/A | N/A | | N/A | N/A |
| | 128 Mbit | | 9 mA | 25 mA | | 12 mA | 16 mA | | | |
| | 256 Mbit | | | | | | | | | |
| | 512 Mbit | | | | | | | 12 mA | 16 mA | |
| | 1 Gbit | | | | | | | | | |
| | 2 Gbit | | | | | N/A | N/A | | | |
| V _{CC} Active Erase/Program Current | 64 Mbit | | 50 mA | 60 mA | | N/A | N/A | | N/A | N/A |
| | 128 Mbit | | 45 mA | 100 mA | | 35 mA | 50 mA | | | |
| | 256 Mbit | | | | | | | | | |
| | 512 Mbit | | | | | | | 35 mA | 50 mA | |
| | 1 Gbit | | | | | | | | | |
| | 2 Gbit | | | | | N/A | N/A | | | |
| | 64 Mbit | | 40 μA | 100 μA | | N/A | N/A | | N/A | N/A |

Migration from Micron MT28E/MT28F to Infineon S29GL-S NOR Flash Family



DC Specifications

| | | Infineon | | | Micron | | | | | |
|---|----------|------------------------|--------|------------------------|------------------------|-------|------------------------|------------------------|--------|---|
| | | S29GL-S | | | MT28E | | | MT28F | | |
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| V _{CC} Standby Current | 128 Mbit | | 70 µA | (–40 °C to +85 °C) | | 50 µA | 120 µA | | | |
| | 256 Mbit | | | | | 65 µA | 135 µA | | | |
| | 512 Mbit | | | | | 70 µA | 200 µA | | | |
| | 1 Gbit | | | | | 75 µA | 230 µA | | | |
| | 2 Gbit | | 140 µA | 200 µA | | N/A | N/A | | 150 µA | 460 µA |
| V _{CC} Reset Current | 64 Mbit | | 10 mA | 20 mA | | | | | | |
| | 128 Mbit | | | | | | | | | |
| | 256 Mbit | | | | | | | | | |
| | 512 Mbit | | | | | | | | | |
| | 1 Gbit | | | | | | | | | |
| | 2 Gbit | | 20 mA | 40 mA | | | | | | |
| Automatic Sleep Mode | 64 Mbit | | 3 mA | 6 mA | | | | | | |
| | 128 Mbit | | | | | | | | | |
| | 256 Mbit | | | | | | | | | |
| | 512 Mbit | | | | | | | | | |
| | 1 Gbit | | | | | | | | | |
| | 2 Gbit | | 6 mA | 12 mA | | | | | | |
| V _{CC} current during power up | 64 Mbit | | 53 mA | 80 mA | | | | | | |
| | 128 Mbit | | | | | | | | | |
| | 256 Mbit | | | | | | | | | |
| | 512 Mbit | | | | | | | | | |
| | 1 Gbit | | | | | | | | | |
| | 2 Gbit | | 106 mA | 160 mA | | | | | | |
| Input LOW Voltage | | –0.5 V | | $0.3 \times V_{IO} V$ | –0.5 V | | 0.8 V | –0.5 V | | 0.8 V (512 Mb, 01 Gb) $0.3 \times V_{IO} V$ (2 Gb) |
| Input HIGH Voltage | | $0.7 \times V_{IO} V$ | | $V_{IO} + 0.4 V$ | $0.7 \times V_{IO} V$ | | $V_{IO} + 0.4 V$ | $0.7 \times V_{IO} V$ | | $V_{IO} + 0.4 V$ |
| Output LOW Voltage | | | | $0.15 \times V_{IO} V$ | | | $0.15 \times V_{IO} V$ | | | $0.15 \times V_{IO} V$ |
| Output HIGH Voltage | | $0.85 \times V_{IO} V$ | | | $0.85 \times V_{IO} V$ | | | $0.85 \times V_{IO} V$ | | |

DC Specifications

Note:

1. *Apart from the Max V_{CC} Standby Current, all other DC Characteristics remain same for (–40 °C to +105 °C) temperature grade devices.*

9 Program or Erase Suspend / Resume

There are specification differences at Program or Erase Suspend / Resume specifications between Micron and Infineon flash memory devices.

Table 9 Program or Erase Suspend / Resume Specification

| | | | Infineon | | Micron | |
|-----------------|----------|--|-------------|--------------|-------------|------------|
| | | | S29GL-S | | MT28E/MT28F | |
| | | | Typ | Max | Typ | Max |
| Erase | 64 Mbit | Erase suspend latency | | 30 μ s | | 20 μ s |
| | 128 Mbit | | | 40 μ s | | |
| | 256 Mbit | | | | | |
| | 512 Mbit | | | | | |
| | 1 Gbit | | | | | |
| | 2 Gbit | | | | | |
| Erase Suspend | | Erase resume to next erase suspend | 100 μ s | | 100 μ s | |
| Program | 64 Mbit | Program suspend latency | | 23.5 μ s | | 15 μ s |
| | 128 Mbit | | | 40 μ s | | |
| | 256 Mbit | | | | | |
| | 512 Mbit | | | | | |
| | 1 Gbit | | | | | |
| | 2 Gbit | | | | | |
| Program Suspend | | Program resume to next program suspend | 100 μ s | | | |

10 Power Up Timing

This section provides a comparison of power up timing of Micron and Infineon flash memory devices.

Table 10 Power Up Timing Specification

| | | Infineon | Micron |
|---|----------|-------------|--------------|
| | | S29GL-S | MT28E/MT28F |
| | | Min | Min |
| V _{CC} setup time to first access | 64 Mbit | 50 μs | 300.05 μs |
| | 128 Mbit | 300 μs | |
| | 256 Mbit | | |
| | 512 Mbit | | |
| | 1 Gbit | | |
| | 2 Gbit | | |
| V _{IO} setup time to first access | 64 Mbit | 50 μs | 50 ns |
| | 128 Mbit | 300 μs | |
| | 256 Mbit | | |
| | 512 Mbit | | |
| | 1 Gbit | | |
| | 2 Gbit | | |
| RESET# LOW to CE# LOW during embedded operation | 64 Mbit | 50 μs (Min) | 150 ns (Min) |
| | 128 Mbit | 35 μs (Min) | |
| | 256 Mbit | | |
| | 512 Mbit | | |
| | 1 Gbit | | |
| | 2 Gbit | | |
| RESET# pulse width during embedded operation | | 200 ns | 100 ns |
| Time between RESET# HIGH and CE# HIGH | | 50 ns | 50 ns |

References

- [1] Micron Parallel NOR Flash Automotive Memory MT28E datasheet
- [2] Micron Parallel NOR Flash Automotive Memory MT28F datasheet

Migration from Micron MT28E/MT28F to Infineon S29GL-S NOR Flash Family



Revision history

Revision history

| Document version | Date of release | Description of changes |
|------------------|-----------------|------------------------------|
| ** | 2020-01-08 | Initial release |
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