DLP Optimized Read Performance for Quad SPI Flash FL-S, FS-S, and FL-L Families

About this document

Scope and purpose

This application note highlights the use of the Data Learning Pattern (DLP) feature that can optimize DDR read performance for the Quad SPI Flash FL-S, FS-S, and Fl-L families.

Intended audience

This is intended for customers using the DDR high performance read with the Quad SPI flash memory devices from Infineon.

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1 Introduction

Quad SPI Flash families of products are built on an advanced 65-nm MirrorBit™ (FL-S, FS-S) and Floating Gate (FL-L) process technologies.

SPI interfaces have progressed from a single-bit, SDR, unidirectional input and output (x1) interface to SDR/DDR four-bit, bidirectional (x4) Quad interface. The Quad SPI Flash 66 MB/s (SDR@133 MHz) and 80 MB/s (DDR@80 MHz) high clock rates the traditional method using t_V (max) as the strobe point within data window does not work; however, using the DLP feature, an optimal capture point within the data window can be achieved without the addition of a data strobe pin.

This application note highlights the SEMPER Flash SDR and DDR Quad I/O access protocol and how the use of the DLP feature can optimize performance. The transactions and protocols that support DLP are:

- SDR QUAD Output Read (1S-1S-4S)
- SDR QUAD IO Read (1S-4S-4S)
- DDR QUAD IO Read (1S-4D-4D)
- SDR QPI Read (4S-4S-4S)
- DDR QPI Read (4S-4D-4D)

2 Quad SPI Flash

The Quad I/O SPI interface retains backward compatibility to support legacy x1 and x2 peripheral products, see **Figure 1**.

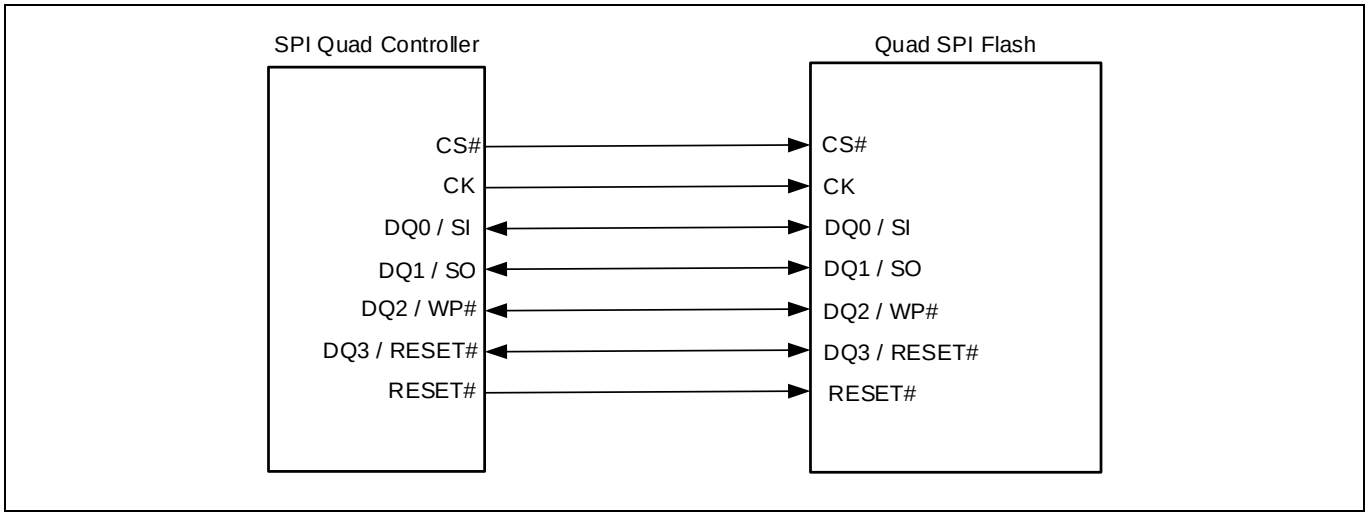

Figure 1 High-level Quad I/O Master/Slave Interface

See the product-specific datasheets listed in **References** to determine the connection and functionalities available for a device.

3 Data Valid Window

Today, high-speed embedded systems have more complex OS and application requirements, which typically result in increased read bandwidth requirements to provide acceptable performance at a neutral or lower cost point. Quad I/O SPI-based flash is becoming a pseudo- industry standard and its key features are its low pin count serial interface and bandwidths. The Quad SPI Flash families offer read access capability offering excellent tradeoffs in reducing interface pin count and best in class read bandwidth. The application of the DLP feature to identify the optimal capture point for the data enabled high-speed Quad SPI-based read performance

The following sections highlight how to evaluate the data valid window for traditional and high frequency SDR and DDR to guarantee the host system has a data window wide enough to capture data.

3.1 Double Data Rate (DDR) Quad Reads

3.1.1 Traditional Evaluating Data Valid Window

The DDR Quad reads timing mode and outputs a new data value upon each edge of CK. After a period known as the clock-to-data-out time (t_V), data becomes valid and remains valid until shortly after the next CK edge (see **Figure 2**). The traditional method host typically uses this CK edge to capture the data being output by the SPI flash. The hold time (t_{HO}) defines the duration the data remains valid after a CK edge.

At low frequency DDR operation, if the duration when data becomes valid (t_V) is less than half the clock period (P_{CK}), the size of t_{DV} is P_{CK} divided by 2, then t_V is subtracted; hold time (t_{HO}) is added after the next clock edge: $t_{DV} = P_{CK} / 2 - t_V + t_{HO}$.

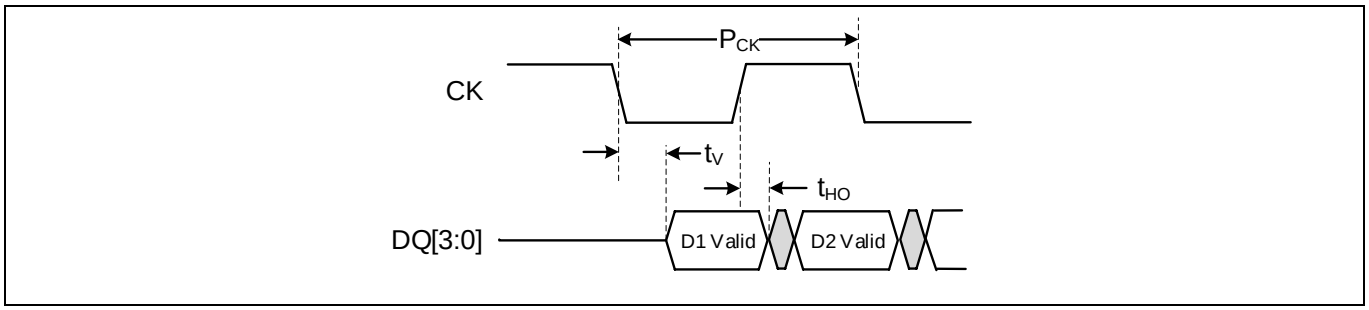

Figure 2 t_{DV} DDR Timing (Traditional)

Example of legacy DDR data valid window:

- P_{CK} = 15 ns (66 MHz)
- t_V [max] = 6.5 ns
- t_{HO} [min] = 1.5 ns
- $t_{DV} = P_{CK} / 2 - t_V + t_{HO}$: 15 ns / 2 - 6.5 ns + 1.5 ns = 2.5 ns

If it is assumed that t_V and t_{HO} timings are fixed, then the data valid window compresses as the CK frequency increases, which limits CK frequency to ~66 MHz.

3.1.2 High Frequency Evaluating Data Valid Window

At high frequency DDR, t_V and t_{HO} timing track each other; a device with a longer t_V has a longer t_{HO} and a device with a short t_V has a shorter t_{HO}. The data valid window timing varies with respect to the next clock edge and t_V. Utilizing this information that t_V and t_{HO} track one another, you can define the size of the data valid window (t_{DV}).

Data Valid Window

At high frequency DDR operation, t_V maybe close to or larger than the half clock period (1/2 P_{CK}). Under this condition, it is still possible to have large enough data window, and by using the DLP feature an optimal strobe point can be found within the data window. At high frequency, the minimum data valid window (t_{DV}) and t_V minimum (t_V_min) can be calculated as follows:

$t_{DV} = t_{CL\_MIN}$[1] - t_{OTT}[2] - t_{IO_SKEW}[3]

$t_{V\_min} = t_{HO} + t_{IO\_SKEW} + t_{OTT}$

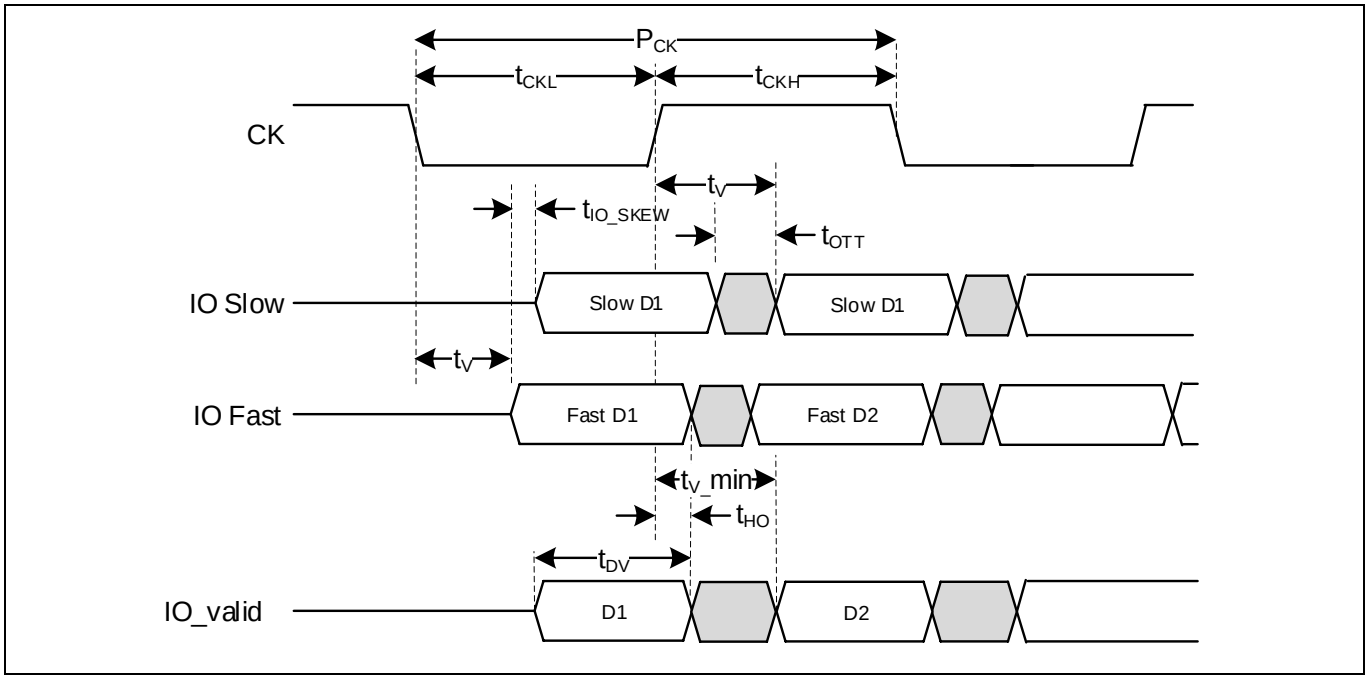

Figure 3 t_{DV} DDR Timing (High Frequency)

Example of DDR data valid window at high frequency:

- 80 MHz clock frequency = 12.5 ns clock period DDR operations and duty cycle of 45% or higher
  - t_{CL_MIN} = 0.45 x P_{CK} = 0.45 x 12.5 ns = 5.625 ns
- For this example, t_{OTT} is the rise time from 0 to 1. The rise time is calculated by using the RC time constant with Bus impedance of 45 ohm and capacitance of 22 pf, with rise time timing reference of 75% of V_{CC}. The rise time is 1.39[4] times the RC time constant (Tau)[5]. For instance, rise time = 1.4 x 0.99 ns = 1.39 ns.
  - t_{OTT} = rise time = 1.39 ns.

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1 t_{CK_MIN} is the minimum of CK low time (t_{CKL}) or CK high time (t_{CKH}) time.

2 t_{OTT} is the maximum Output Transition Time from one valid data value to the next valid data value on each IO. t_{OTT} is dependent on system level considerations including:

- Memory device output impedance (drive strength).
- System-level parasitic on the IOs (primarily bus capacitance).
- Host memory controller input VIH and VIL levels at which 0 to 1 and 1 to 0 transitions are recognized.
- t_{OTT} is not a specification tested by Infineon, it is system dependent and must be derived by the system designer based on the above considerations.

3 t_{IO_SKEW} is the maximum difference (delta) between the minimum and maximum t_V (output valid) across all IO signals.

4 Multiplier of Tau time for voltage to rise to 75% of V_{CC}.

5 Tau = R (Output Impedance) x C (Load Capacitance).

Data Valid Window

- Data Valid Window
  - $t_{DV} = t_{CLH} - t_{IO\_SKEW} - t_{OTT} = 5.625\ ns - 600\ ps - 1.39\ ns = 3.635\ ns$
- t_V Minimum
  - $t_{V\_min} = t_{HO}\,[min] + t_{IO\_SKEW} + t_{OTT} = 1\ ns + 600\ ps + 1.39\ ns = 2.99\ ns$

4 Read Transactions — Data Learning Pattern

In a high frequency implementation, t_V time can be greater than a clock period (SDR) or a half clock period (DDR), which means a specific CK edge cannot be used by the master to reliably capture the data coming from the flash. The master must skew the data-capture point with respect to each CK edge to reliably capture data.

The read transactions that support DLP are shown in **Figure 4** through **Figure 8**. These transactions add an 8-bit DLP that is output by the **SEMPER** Flash on the four dummy clock cycles before outputting target data. DLP provides a known data sequence on each data signal, so that the host controller can determine the optimal capture timing to use when receiving the read data. The dummy cycles that carry the DLP occur during the idle period in the read transaction, while the target data is retrieved from the memory array; it can be accomplished without impacting performance. DLP presents the same timing, phase delay, and skew characteristics that exist during the output of the target data. The clock to data output delay t_V will be the same for DLP and the target data on each individual data signal.

Data phase delay and skew arise from issues related to either the memory device or the system environment. Memory device timing variations are caused by process, voltage, temperature, and output-to-output skew. System-level variations are introduced by PCB parasitic, trace-length mismatches, and bus capacitive loading. The timing characteristics of the known data learning pattern will allow the host controller to compensate for both the device and system-level timing phase and skew offsets when valid data is present on the bus.

The following are some of the key points:

- DLP output by the device for each supported read transaction
- Oversampled by host using DLP identifies the optimal data capture point
- Data read from device
  - Calibration upon every read transaction
  - Provides compensation for process, voltage, temperature
- Enables 80 MBps Data Rate

The read transactions using DLP are processed as follows:

1. The command operation code is transferred to be compatible with all other legacy SPI instructions.
2. Target address is transferred.
3. Mode bits are loaded, if needed.
4. Read latency (dummy) cycles are issued while target data is extracted from the array.
5. DLP is output by Flash during the last eight dummy cycles for SDR and four dummy cycles for DDR.
6. Target data is output by the Flash device.

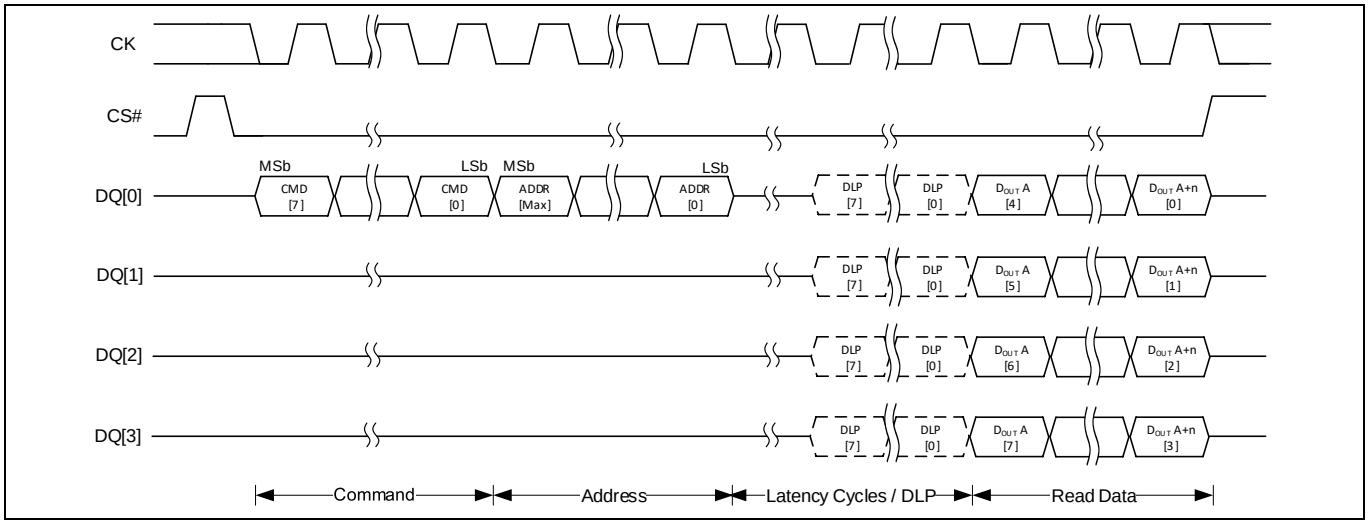

Figure 4 SDR QUAD Output Read (4QOR) Command (1S-1S-4S)

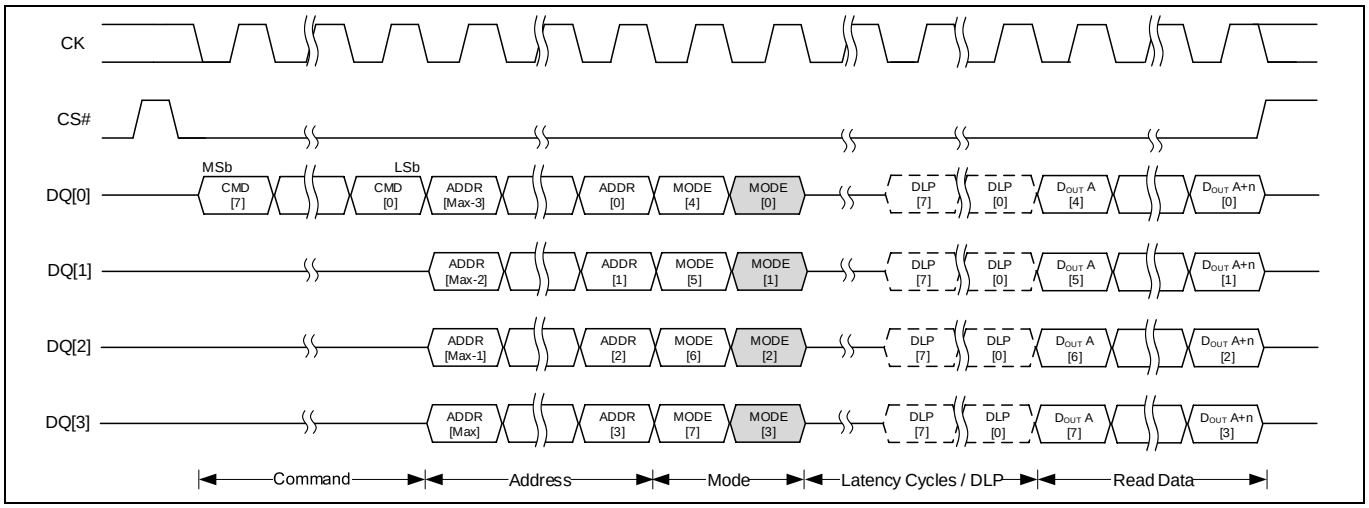

Figure 5 SDR QUAD IO Read (QIOR) Command (1S-4S-4S)

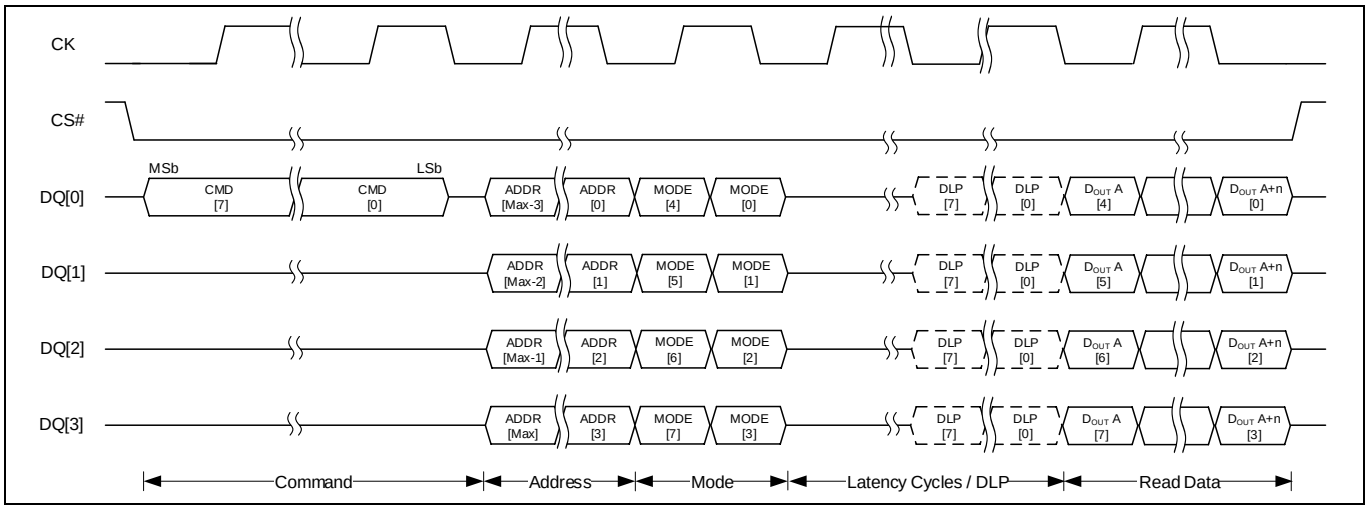

Figure 6 DDR QUAD IO Read (DDRQIOR) Command (1S-4D-4D)

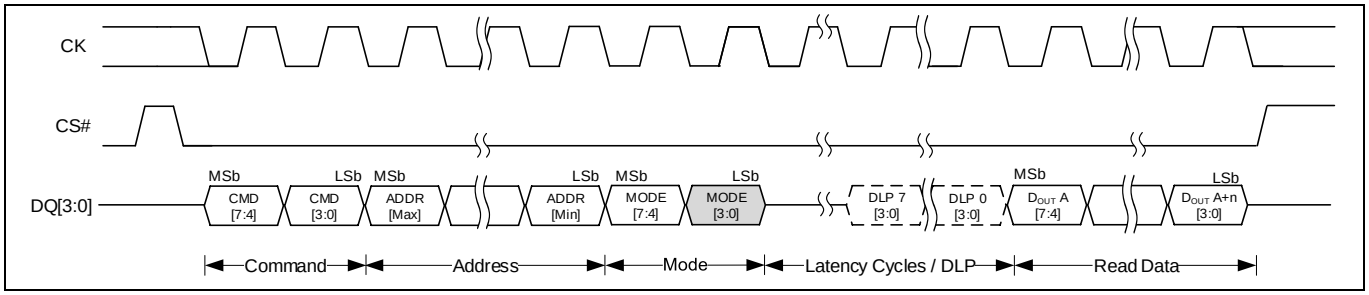

Figure 7 SDR QPI Read (QIOR) Command (4S-4S-4S)

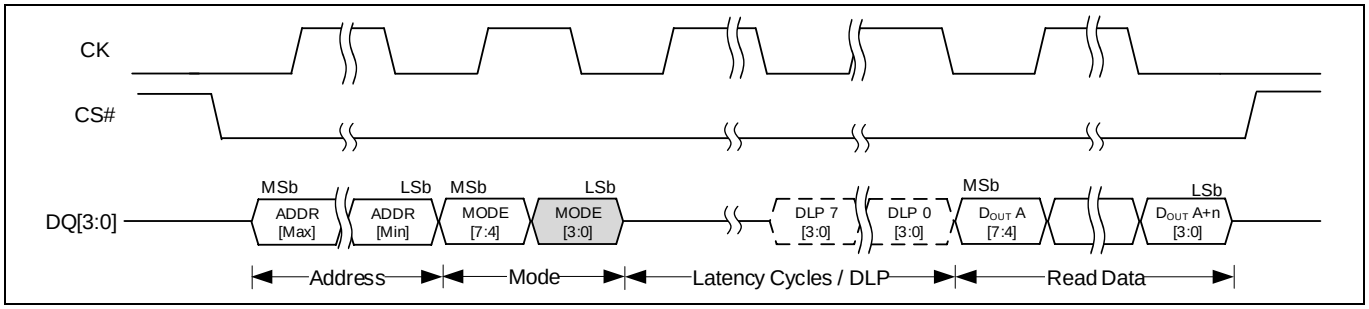

Figure 8 DDR QPI Read (DDRQIOR) Transaction (4S-4D-4D)

5 Data Learning Pattern Storage and Definition

The nonvolatile data learning register (NVDLR) and the volatile data learning register (VDLR) are used to define the sequence of DLP values (8 bits on each of the four I/Os) that are used during a read transaction to train the host controller (see **Figure 9**). The NVDLR register can be programmed with a customer-specific DLP value. During power-up or reset, the value in the NVDLR register is loaded into the VDLP register. The sequence of values used as DLP is defined in the VDLP register during read transactions. VDLP can be read and written directly by the host system. When VDLP is 00h, DLP will not be output during read operations, thus providing an option to turn OFF DLP. See the datasheets mentioned in **References** for details on reading and writing these registers.

The choice of an appropriate DLP is up to the system developer but the pattern should be chosen to maximize skews dependent on the bit-stream sequence. The most significant pattern-dependent skewing is bounded by transitions from states that have been stable for extended periods and states that have existed for shorter periods of time; for example, at higher frequencies, the HIGH to LOW transition of a signal behaves slightly different when the bit stream is xx110 than when the bit stream is xx010. The HIGH reached in the xx110 pattern is usually a higher voltage than the HIGH reached with the xx010 pattern. The higher starting voltage will mean that it will take slightly longer to reach a valid LOW state during a High to Low transition. The xx110 HIGH to LOW transition demonstrates a ‘strong 1,’ while the xx010 transition demonstrates a ‘weak 1.’

The DLP pattern should be chosen to include at least one instance of: weak 0, strong 0, weak 1, and strong 1

One pattern fulfilling these requirements is 34h (00110100b). The edges in the 34h pattern step through the following transitions: Strong 0 → Strong 1 → Weak 0 → Weak 1.

Any data learning pattern that includes these four transition types should maximize pattern-dependent skew characteristics.

6 Host Capture Strategy

The overall data-capture strategy for the host memory controller is to use the DLP input as a test sequence to characterize system response and determine t_V and t_{DV}. Once the data eye has been identified during the DLP portion of the read sequence, the controller selects the optimal data-capture point to maximize the timing margin for the read data.

A common way to create the master data-capture logic is via series of skewed data-capture points that span the data-valid window. **Figure 9** shows the implementation for a single DQ might consist of five channels with a fixed sampling delay between each of the channels. The five delayed strobes (A through E) could be generated with a delay-locked loop (DLL) or using an oversampling clock that is in turn generated using an internally available higher frequency clock. The host controller samples the target DQ while the DLP is being output. The phase-delayed strobes (A-E) are triggered by the clock edges when the DLP is output.

The following are some of the key points:

- Data oversampled
- Samples from ‘taps’ B, C, and D always successfully capture the DLP
- In this case, Tap C provides the greatest margin
- Use Tap C to capture data for the remainder of this read transaction
- Recalibration can be performed prior to every read transaction, and it provides more robust/reliable operation across operating conditions

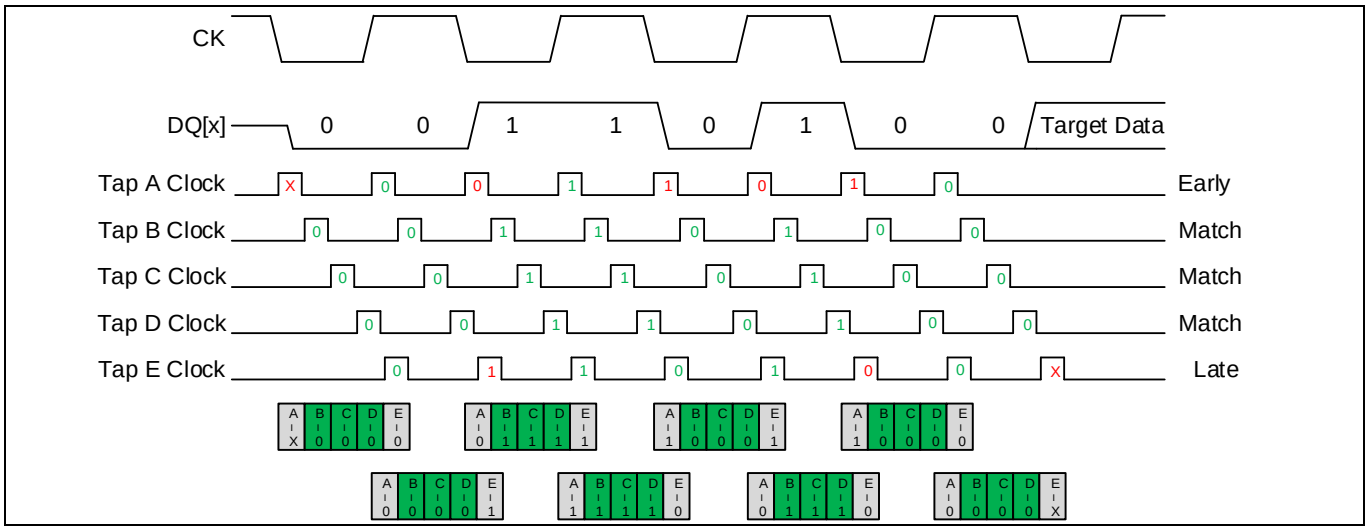

Figure 9 Host Capture Strategy DDR

7 Conclusion

As embedded applications continue to demand higher performance, the legacy SPI interface and protocols must continue to accommodate higher read speeds. The DLP approach enables Flash with Quad SPI to have higher data rate. This new feature provides the embedded designers another attractive nonvolatile memory solution to maximize read data throughput while minimizing pin count, PCB complexity, package size, and cost. These principles and feature improvements apply across many market applications whether it is industrial, automotive, or consumer; DLP-enabled Flash provides another enhanced solution to improve system design and performance, all for a reasonable cost.

References

S25FL-S

[1] **001-98284: S25FL512S, 512 Mb (64 MB), 3.0 V SPI Flash Memory**

[2] **002-00124: S25FL256L 256 Mbit (32 Mbyte) 3.0 V FL-L Flash Memory**

[3] **001-98295: S70FL01GS 1 Gbit (128 Mbyte) 3.0V SPI Flash**

[4] **002-00466: S79FL01GS, 1 Gbit (128 Mbyte) Dual-Quad MirrorBit™ Flash NVM CMOS 3.0V Core SPI with Multi-I/O**

S25FS-S

[5] **002-03631: S25FS064S, 64 Mbit (8 Mbyte), 1.8-V FS-S Flash**

[6] **002-00368: S25FS128S/S25FS256S, 1.8 V, Serial Peripheral Interface with Multi-I/O, MirrorBit™ Non-Volatile Flash**

[7] **002-00488: S25FS512S, 512 Mb, 1.8 V Serial Peripheral Interface with Multi-I/O Flash**

[8] **002-03833: S70FS01GS, 1-Gb (128 MB), 1.8 V FS-S Flash**

[9] **002-25385: S79FS01GS, 1 Gbit, 1.8 V Dual-Quad Serial Peripheral Interface with Multi-I/O Flash**

S25FL-L

[10] **002-00124: S25FL256L, S25FL128L, 256 Mbit (32 Mbyte), 128 Mbit (16 Mbyte) 3.0 V FL-L Flash Memory**

[11] **002-12878: S25FL064L, 64-Mbit (8-Mbyte) 3.0 V FL-L SPI Flash Memory**

Revision history

Document version	Date of release	Description of changes
**	2019-12-10	New Application Note
*A	2021-05-04	Updated to Infineon format

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Edition 2021-05-04
Published by
Infineon Technologies AG
81726 Munich, Germany

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Document reference
002-29091 Rev. *A

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