Migrating from S27KL0641/S27KS0641 to S27KL0642/S27KS0642

About this document

Scope and purpose

This application note discusses the key differences that need to be considered when migrating from S27KL0641/S27KS0641 to S27KL0642/S27KS0642. This application note explains how S27KL0642/S27KS0642 is a replacement for S27KL0641/S27KS0641.

Intended audience

This document is primarily intended for anyone who wants to migrate from S27KL0641/S27KS0641 to S27KL0642/S27KS0642.

Associated part family

S27KL0641/S27KS0641, S27KL0642/S27KS0642

Table of contents

1 Introduction

S27KL0642/S27KS0642, a 64-Mbit HYPERRAM™, is a replacement device for S27KL0641/S27KS0641. For all designs, S27KL0642/S27KS0642 can be considered as a superset of S27KL0641/S27KS0641. The two devices are pin-to-pin compatible and identical in terms of package composition and dimensions and read/write functionality. This application note discusses the key differences between the two devices that need to be considered when migrating from S27KL0641/S27KS0641 to S27KL0642/S27KS0642.

2 Drop-in replacement or not?

From a hardware point of view, no PCB modification required. From a software point of view, the key difference between the two devices are configuration register 1 and device ID. See **Critical considerations** for more details.

S27KL0642/S27KS0642 adds many features like deep power down capability, lower standby current, and higher speed capability. **Table 1** shows the compatibility chart of S27KL0641/S27KS0641 and S27KL0642/S27KS0642. For a detailed comparison, see **Table 4**.

Table 1 Compatibility chart

S27KL0641/S27KS0641 feature or spec	S27KL0642/S27KS0642 compatible?
Package	Yes
Pinout	Yes
Temperature range	Yes
Operating voltage	Yes
Operating current	Yes
Standby current	Yes
Read/write function	Yes
Timing/frequency	Yes
Default ID and CR settings	No

3 Ordering part numbers

Table 2 lists the recommended S27KL0642/S27KS0642 ordering part numbers (OPN) that correspond to S27KL0641/S27KS0641 ordering part numbers.

Table 2 Recommended ordering part numbers for migration

S27KL0641/S27KS0641		S27KL0642/S27KS0642		Comments
OPN	**Status**	**OPN**	**Status**	
S27KS0641	Not recommended for new designs	S27KS0642	In production	No hardware change required. Both devices are pin compatible.
S27KL0641	Not recommended for new designs	S27KL0642	In production	No hardware change required. Both devices are pin compatible.

4 Detailed comparison of S27KL0641 and S27KL0642

Table 3 Detailed comparison table

	S27KL0641	S27KL0642	Comments
Pinout/package outline	24-ball FBGA	24-ball FBGA	Identical
Temperature range	–40 °C to +85 °C	–40 °C to +85 °C	Identical
Operating voltage range	2.7 V to 3.6 V	2.7 V to 3.6 V	Identical
DC characteristics	**Table 8** shows the detailed comparison of DC parameters		
AC characteristics	**Table 10** shows the detailed comparison of AC characteristics		
Standby current (ICC4I)	200 µA @ 85 °C	250 µA @ 85 °C	S27KL0642 has a higher standby current
Deep power down current	20 µA	12 µA	S27KL0642 has a lower deep power down current
Hybrid sleep current	–	230 µA	New feature/spec in this device. Not supported in the previous generation device.
CS# HIGH to enter hybrid sleep (t_{HSIN})	–	3 µs	New feature/spec in this device. Not supported in the previous generation device
Differential clock	Not applicable at V_{CC} = 3 V	Applicable for all operating voltage ranges	CK# of S27KL0642 can be left floating if not used
Die manufacture information	-	36-byte die manufacture information available	This information can be read as a register with an address offset of 0x1800. New feature/spec in this device. Not supported in the previous generation device.
Clock frequency (Max)	100 MHz	200 MHz	Higher speed offered in S27KL0642. For timing comparison, see **Table 11**.
Default latency	6 clock cycles	7 clock cycles	Critical difference. See **Latency cycles**.
Configuration register 1	Used to configure distributed refresh interval	Added additional options	See **Table 7**
V_{DD} minimum and RESET# HIGH to first access (t_{VCS})	150 µs / V	150 µs / V	Identical
Power down period for part to initialize correctly (t_{PD})	50	50	Identical
V_{DD} required to ensure initialization (V_{RST})	0.8	0.7	S27KL0642 offers a lower $V_{RST.}$
V_{DD} lock-out below which require initialization (V_{LKO})	2.7	2.4	S27KL0642 offers a lower $V_{LKO.}$

Detailed comparison of S27KL0641 and S27KL0642

	S27KL0641	S27KL0642	Comments
V_{DD} power-down ramp rate (t_{VF})	50 µs / V	50 µs / V	Identical
Reset pulse width (t_{RP})	200 ns	200 ns	Identical
Time between RESET# HIGH and CS# LOW (t_{RH})	200 ns	200 ns	Identical
Time between RESET# LOW to CS# LOW (t_{RPH})	400 ns	400 ns	Identical
Device ID0	0x0C81	0x0C81	Identical
Device ID1	0x0000	0x0001	Critical difference. See **Device ID**.

5 Detailed comparison of S27KS0641 and S27KS0642

Table 4 Detailed comparison table

	S27KS0641	S27KS0642	Comments
Pinout/package outline	24-ball FBGA	24-ball FBGA	Identical
Temperature range	–40 °C to +85 °C	–40 °C to +85 °C	Identical
Operating voltage range	1.7 V to 1.95 V	1.7 V to 2.0 V	S27KS0642 offers wide operating range.
DC characteristics	**Table 9** shows the detailed comparison of DC parameters.		
AC characteristics	**Table 11** shows the detailed comparison of AC characteristics.		
Standby current	200 µA @ 85 °C	220 µA @ 85 °C	S27KS0642 has a higher standby current.
Deep power down current	10 µA	10 µA	Identical
Hybrid sleep current	–	200 µA	New feature/spec in this device. Not supported in the previous generation device.
Differential clock (CK#)	Differential clock is required	Differential clock is optional	CK# of S27KL0642 can be left floating if not used.
CS# HIGH to enter hybrid sleep (t_{HSIN})	–	3 µs	New feature/spec in this device. Not supported in the previous generation device.
Die manufacture information	–	36 bytes die manufacture information available	This information can be read as a register with an address offset of 0x1800. New feature/spec in this device. Not supported by the earlier generation device.
Clock frequency (Max)	166 MHz	200 MHz	Higher speed offered in S27KS0642. For timing comparison, see **Table 11**.
Default latency	6 clock cycles	7 clock cycles	Critical difference. See **Latency cycles**.
Configuration register 1	Used to configure distributed refresh interval	Added additional options	See **Table 7**
V_{DD} minimum and RESET# HIGH to first access (t_{VCS})	150 µs / V	150 µs / V	Identical
Power down period for part to initialize correctly (t_{PD})	50	50	Identical
V_{DD} required to ensure initialization (V_{RST})	0.8	0.7	S27KS0642 offers a lower V_{RST}.
V_{DD} lock-out below which require initialization (V_{LKO})	1.7	1.5	S27KS0642 offers a lower V_{LKO}.

Detailed comparison of S27KS0641 and S27KS0642

	S27KS0641	S27KS0642	Comments
V_{DD} power-down ramp rate (t_{VF})	50 µs / V	50 µs / V	Identical
Reset pulse width (t_{RP})	200 ns	200 ns	Identical
Time between RESET# HIGH and CS# LOW (t_{RH})	200 ns	200 ns	Identical
Time between RESET# LOW to CS# LOW (t_{RPH})	400 ns	400 ns	Identical
Device ID0	0x0C81	0x0C81	Identical
Device ID1	0x0000	0x0001	Critical difference. See **Device ID**.

6 Critical considerations

You must consider all parameter differences mentioned in **Table 3** and **Table 4** during the migration to S27KL0642/S27KS0642. This section discusses the critical differences between S27KL0641/S27KS0641 and S27KL0642/S27KS0642. System designers should also review the datasheet when migrating to the new part.

6.1 Device ID (ID0 and ID1)

S27KL0641/S27KS0641 and S27KL0642/S27KS0642 incorporate a two, double-word (4-byte), read-only device ID to identify the product uniquely. Device ID allows the host to determine the manufacturer, product density, and product type. **Table 5** gives the Device IDs of S27KL0641/S27KS0641 and S27KL0642/S27KS0642, where the difference is highlighted in bold.

Table 5 Device ID

	S27KL0641/S27KS06421	S27KL0642/S27KS0642
Device ID 0	0x0C81	0x0C81
Device ID 1	0x0000	0x00**01**

6.2 Latency cycles

Configuration register 0 (CR0) is used to set latency cycles. S27KL0641/S27KS0641 has a latency setting of six clocks by default, while S27KL0642/S27KS0642 has a latency setting of seven clocks by default. Migrating to S27KL0642/S27KS0642 requires a firmware update to take care of the additional one clock cycle, if using the default latency settings.

Table 6 Comparing CR0

CR1 bit	S27KL0641/S27KS0641	S27KL0642/S27KS0642	Comments
[7:4]	0001b (default)	0010b (default)	Default value is different

6.3 Configuration register 1

In S27KL0641/S27KS0641, configuration register 1 (CR1) is used to define the distributed refresh interval for this HYPERRAM™ device. A few additional features were added in S27KL0642/S27KS0642. they are configurable through CR1 of S27KL0642/S27KS0642. **Table 7** compares CR1 of S27KL0641/S27KS0641 and S27KL0642/S27KS0642.

Table 7 Comparing CR1

CR1 bit	S27KL0641/S27KS0641	S27KL0642/S27KS0642	Comments
[15:8]	0x00 (default)	0xFF (default)	Not used, but the default value is different
[7]	0 (default)	1 (default)	
[6]	0 (default)	Master clock type: 1 = single ended (default) 0 = differential	Default value in S27KX0641 configures S27KX0642 in differential clock mode. However, even if the differential clock in S27KX0642 is enabled, toggling of CK# is optional. Make sure CK# input remains static (either HIGH or LOW), but not floating to prevent it from picking unnecessary noise.

Critical considerations

CR1 bit	S27KL0641/S27KS0641	S27KL0642/S27KS0642	Comments
[5]	0 (default)	Hybrid sleep: 0 = normal operation (default) 1 = enter hybrid sleep	In S27KX0642, use this bit to enter into Hybrid Sleep. Retain the default if the feature is not used.
[4:2]	000b (default)	Partial array refresh: 000b = Full array (default)	In S27KX0642, you can use these bits to restrict the refresh operation to a portion of the memory
[1:0]	Distributed refresh interval 10b – 4 µs (default) 11b – 1.5 times default 00b – 2 times default 01b – 4 times default	Distributed refresh interval 10b – 1 µs (only applicable for industrial plus (105 °C) devices) 11b – Reserved 00b – Reserved 01b – 4 µs	For S27KX0642, CR[1:0] are read-only bits determined and configured by the device internally based on its refresh interval variation across the Process, Voltage, Temperature (PVT) corners. You can probe these two bits prior to every HYPERRAM™ access (write or read) to determine whether refresh interval should be 10b (1 µs) or 01b (4 µs) for the current cycle and set the t_{CSM} for the host controller accordingly. Alternatively, if the host controller does not want to access CR1 prior to every memory access, it can set t_{CSM} to 4 µs (fixed), as per datasheet recommendations at 85 °C.

6.4 DC characteristics (S27KL0641 and S27KL0642)

Table 8 compares the DC parameters of S27KL0641 with S27KL0642. S27KL0642 has some higher DC characteristic values; you should take these differences in DC characteristics into consideration at the system level for a proper migration.

Table 8 Comparing DC Characteristics

Parameter	Description	Test condition	S27KL0641		S27KL0642		Unit
			Typ	Max	Typ	Max	
I_{LI4}	Input leakage current 3.3 V device reset signal low only	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max		+20		+15	µA
I_{CC1}	V_{CC} active read current	CS# = V_{IL}, V_{CC} = 3.6 V	20	35	15	30	mA
I_{CC2}	V_{CC} active write current	CS# = V_{IL}, V_{CC} = 3.6 V	15	35	15	30	mA
I_{CC4I}	V_{CC} standby current	CS# = V_{IL}, V_{CC} = 3.6 V	135	200	90	250	µA
I_{CC5}	Reset current	CS# = V_{IH}, RESET# = V_{IL}, V_{CC} = V_{CC} max		20		1	mA
I_{CC6I}	Active clock stop current	CS# = V_{IH}, RESET# = V_{IL}, V_{CC} = V_{CC} max	5.3	8	5	8	mA
I_{CC7}	Vcc current during power up	CS# = V_{IH}, V_{CC} = V_{CC} max, V_{CC} = V_{CCQ} = 3.6V	-	35		35	mA
I_{DPD}	Deep power down current	CS# = V_{IH}, V_{CC} = V_{CC} max, V_{CC} = V_{CCQ} = 3.6 V		20		12	µA

Critical considerations

Parameter	Description	Test condition	S27KL0641		S27KL0642		Unit
			Typ	Max	Typ	Max	
I_{HS}	Hybrid sleep current	CS# = V_{IH}, VCC = V_{CC} max, V_{CC} = V_{CCQ} = 2.0 V		-	35	230	µA

6.5 DC characteristics (S27KS0641 and S27KS0642)

Table 9 compares the DC parameters of S27KS0641 with S27KS0642. S27KS0642 has some higher DC characteristic values; you should take these differences in the DC characteristics into consideration at system level for a proper migration.

Table 9 Comparing DC characteristics

Parameter	Description	Test condition	S27KS0641		S27KS0642		Unit
			Typ	Max	Typ	Max	
I_{LI4}	Input leakage current 1.8 V device reset signal low only	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} max		+20		+15	µA
I_{CC1}	V_{CC} active read current	CS# = V_{IL}, @200 MHz, V_{CC} = 2.0 V	20	60	15	25	mA
I_{CC2}	V_{CC} active write current	CS# = V_{IL}, @200 MHz, V_{CC} = 2.0 V	15	60	15	25	mA
I_{CC4I}	V_{CC} standby current	CS# = V_{IL}, @200 MHz, V_{CC} = 2.0 V	135	200	80	220	µA
I_{CC5}	Reset current	CS# = V_{IH}, RESET# = V_{IL}, V_{CC} = V_{CC} max		20		1	mA
I_{CC6I}	Active clock stop current	CS# = V_{IH}, RESET# = V_{IL}, V_{CC} = V_{CC} max	5.3	8	5	8	mA
I_{CC7}	Vcc current during power up	CS# = V_{IH}, V_{CC} = V_{CC} max, V_{CC} = V_{CCQ} = 2.0V	-	35		35	mA
I_{DPD}	Deep power down current	CS# = V_{IH}, V_{CC} = V_{CC} max, V_{CC} = V_{CCQ} = 2.0 V		10		10	µA
I_{HS}	Hybrid sleep current	CS# = V_{IH}, V_{CC} = V_{CC} max, V_{CC} = V_{CCQ} = 2.0V		-	25	200	µA

6.6 AC characteristics (S27KL0641 and S27KL0642)

Table 10 compares the AC parameters of S27KL0641 with S27KL0642. Migrating to S27KL0642 requires no timing adjustment at system level due to its improved AC characteristics values.

Table 10 Comparing timing parameters

Parameter	Symbol	S27KL0641 (100 MHz)		S27KL0642 (166 MHz)		S27KL0642 (200 MHz)		Unit
		Min	Max	Min	Max	Min	Max	
Chip select HIGH between transactions	t_{CSHI}	10		6	-	6	-	ns
HYPERRAM™ read-write recovery time	t_{RWR}	40		36	-	35	-	ns
Chip select setup to next CK rising edge	t_{CSS}	3		3	-	3	-	ns
Data strobe valid	t_{DSV}		12	-	12	-	6.5	ns
Input setup	t_{IS}	1		0.6	-	0.5	-	ns

Critical considerations

Parameter	Symbol	S27KL0641 (100 MHz)		S27KL0642 (166 MHz)		S27KL0642 (200 MHz)		Unit
		Min	Max	Min	Max	Min	Max	
Input Hold	t_{IH}	1		0.6	-	0.5	-	ns
HYPERRAM™ read initial access time	t_{ACC}	40		36	-	35	-	ns
Clock to DQs Low Z	t_{DQLZ}	0		0	-	0	-	ns
CK transition to DQ valid (64 Mb)	t_{CKD}		7	-	7	-	6.5	ns
CK transition to DQ invalid (64 Mb)	t_{CKDI}		5.2	-	5.6	-	5.7	ns
Data valid (t_{DV} min = the lessor of: t_{CKHP} min - t_{CKD} max + t_{CKDI} max) or t_{CKHP} min - t_{CKD} min + t_{CKDI} min)	t_{DV}	2.7		1.3	-	1.45	-	ns
CK transition to RWDS valid (64 Mb)	t_{CKDS}	1	7	1	7	1	6.5	ns
RWDS transition to DQ valid	t_{DSS}		0.8	-	0.8	-	0.4	ns
RWDS transition to DQ invalid	t_{DSH}		0.8	-	0.8	-	0.8	ns
Chip select hold after CK falling edge	t_{CSH}	0		0	-	0	-	ns
Chip select inactive to RWDS High-Z	t_{DSZ}		7	-	7	-	6.5	ns
Chip select inactive to DQ High-Z	t_{OZ}		7	-	7	-	6.5	ns
HYPERRAM™ chip select maximum low time (85 °C)	t_{CSM}		4	-	4	-	4	µs
Refresh time	t_{RFH}	40		36	-	35	-	ns
HYPERBUS™ CK transition to RWDS LOW @CA phase @read (64 Mb)	t_{CKDSR}			1	7	1	7	ns

6.7 AC characteristics (S27KS0641 and S27KS0642)

Table 11 compares the AC parameters of S27KS0641 with S27KS0642. Migrating to S27KS0642 requires no timing adjustment at system level due to its improved AC characteristics values except t_{CSS} timing parameter. You must modify the system-level timing to meet the t_{CCS} timing requirement.

Table 11 Comparing timing parameters

Parameter	Symbol	S27KS0641 (166 MHz)		S27KS0642 (200 MHz)		Unit
		Min	Max	Min	Max	
Chip select HIGH between transactions	t_{CSHI}	6		6	-	ns
HYPERRAM™ read-write recovery time	t_{RWR}	36		35	-	ns
Chip select setup to next CK rising edge	t_{CSS}	3		4	-	ns
Data strobe valid	t_{DSV}		12	-	5	ns
Input setup	t_{IS}	0.6		0.5	-	ns
Input hold	t_{IH}	0.6		0.5	-	ns
HYPERRAM™ read initial access time	t_{ACC}	36		35	-	ns
Clock to DQs low Z	t_{DQLZ}	0		0	-	ns
CK transition to DQ valid (64 Mb)	t_{CKD}		5.5	-	5	ns

Critical considerations

Parameter	Symbol	S27KS0641 (166 MHz)		S27KS0642 (200 MHz)		Unit
		Min	Max	Min	Max	
CK transition to DQ invalid (64 Mb)	t_{CKDI}		4.6	-	4.2	ns
Data valid (t_{DV} min = the lessor of: t_{CKHP} min - t_{CKD} max + t_{CKDI} max) or t_{CKHP} min - t_{CKD} min + t_{CKDI} min)	t_{DV}	1.7		1.45	-	ns
CK transition to RWDS valid (64 Mb)	t_{CKDS}	1	5.5	1	5	ns
RWDS transition to DQ valid	t_{DSS}		0.45	-	0.4	ns
RWDS transition to DQ invalid	t_{DSH}		0.45	-	0.4	ns
Chip select hold after CK falling edge	t_{CSH}	0		0	-	ns
Chip select inactive to RWDS High-Z	t_{DSZ}		6	-	5	ns
Chip select inactive to DQ High-Z	t_{OZ}		6	-	5	ns
HYPERRAM™ chip select maximum low time (85 °C)	t_{CSM}		4	-	4	µs
Refresh time	t_{RFH}	36		35	-	ns
HYPERBUS™ CK transition to RWDS low @CA phase @read (64 Mb)	t_{CKDSR}			1	5.5	ns

References

[1] **S27KL0641/S27KS0641, 3.0 V/1.8 V, 64 Mb (8 MB)/128 Mb (16 MB), HYPERRAM™ self-refresh DRAM**

[2] **S27KL0642/S27KS0642, 3.0 V/1.8 V, 64 Mb (8 MB), HYPERRAM™ self-refresh DRAM**

[3] **HYPERBUS™ specification low signal count, high performance DDR bus**

Revision history

Document version	Date of release	Description of changes
**	2019-07-11	New application note
*A	2020-01-08	Added default ID and CR settings in **Table 1**. Updated die manufacturer information and hybrid sleep values in **Table 3** and **Table 4**. Updated in **Table 3** and **Table 4**. Updated **Table 7**. Added 200 MHz values in **Table 10**.
*B	2021-09-21	Migrated to Infineon template.

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