SPI Flash Migration from Micron M25P128 to Infineon S25FL128L

About this document

Scope and purpose

Since Micron M25P128 SPI flash devices have entered End of Life, Infineon S25FL128L is an excellent replacement with good fit and a long production lifetime. This application note shows the best-fit Infineon part numbers, and summarizes the similarities and differences for engineers who are replacing the M25P128 devices with Infineon S25FL128L devices.

Intended audience

This is intended for flash memory users who intend to migrate from Micron M25P128 to Infineon S25FL128L.

*Note: Please see **References** before reading this application note.*

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1 Ordering Options

At the time of publication of the original version (Rev. **) of this Application Note, the Micron web site shows four End-of-Life (EOL) part numbers for the M25P128, which span two chip packages and two packing methods for shipping; this table shows the best-fit part numbers from the Infineon S25FL-L family:

Index	Part Family	Part Number	Density	Bus Width	Voltage	Package	Pin Count	SDR Speed	Op Temp	Media
1	M25P	M25P128-VME6GB	128Mb	x1	2.7V-3.6V	VFDFPN8	8-pin	54 MHz	-40C to +85C	Tray
2	M25P	M25P128-VME6TGB	128Mb	x1	2.7V-3.6V	VFDFPN8	8-pin	54 MHz	-40C to +85C	Tape & Reel
3	S25FL-L	S25FL256LAGNFI010	256Mb	x4	2.7V-3.6V	WSON 6x8	8-pin	133 MHz	-40C to +85C	Tray
4	S25FL-L	S25FL256LAGNFI013	256Mb	x4	2.7V-3.6V	WSON 6x8	8-pin	133 MHz	-40C to +85C	Tape & Reel
5	M25P	M25P128-VMF6TPB	128Mb	x1	2.7V-3.6V	SO16 Wide	16-pin	54 MHz	-40C to +85C	Tape & Reel
6	M25P	M25P128-VMF6PB	128Mb	x1	2.7V-3.6V	SO16 Wide	16-pin	54 MHz	-40C to +85C	Tube
7	S25FL-L	S25FL128LAGMFI000	128Mb	x4	2.7V-3.6V	SOIC-16	16-pin	133 MHz	-40C to +85C	Tray
8	S25FL-L	S25FL128LAGMFI001	128Mb	x4	2.7V-3.6V	SOIC-16	16-pin	133 MHz	-40C to +85C	Tube
9	S25FL-L	S25FL128LAGMFI003	128Mb	x4	2.7V-3.6V	SOIC-16	16-pin	133 MHz	-40C to +85C	Tape & Reel

The first four part numbers are for the WSON 8-pin package. Note that the Infineon datasheet shows that S25FL128L is available in the WSON 5x6 (WND008) package, while S25FL128L is available in the WSON 6x8 (WNG008) package. The Micron datasheet shows the VFDFPN8 8x6 (MLP8) package for M25P128; this package is compatible with the Infineon WSON 6x8 (WNG008) package, so this migration must use the higher-density Infineon S25FL256S device with the “N” Package Type and the “01” Model Number.

The last five part numbers are for the SOIC-16 package; you have many more migration options if you are starting with this package. As long as you select the “M” Package Type and the “00” Model Number, you have access to all densities, speed grades, and temperature ranges offered by Infineon.

Note that the Infineon S25FL-L family provides multiple upgrade or change opportunities vs. Micron M25P128; see the list below with matchups highlighted in yellow:

Feature	Micron	Infineon Options
Density (Mb)	128	64 128 256
Bus Width	x1	x1 x2 x4
Package	VFDFPN8 SO16 Wide	8-contact WSON SOIC16 5x5 ball BGA 5x4 ball BGA
Single Data Rate (SDR) IO Speed (MHz)	54	108 (64 Mb) 133 (128/256 Mb)
Double Data Rate (DDR) IO Speed (MHz)		54 (64 Mb) 66 (128/256 Mb)
Temperature Rating	Industrial -40°C to +85°C	Industrial -40°C to +85°C Industrial Plus -40°C to +105°C Automotive, AEC-Q100 Grade 3 -40°C to +85°C

Ordering Options

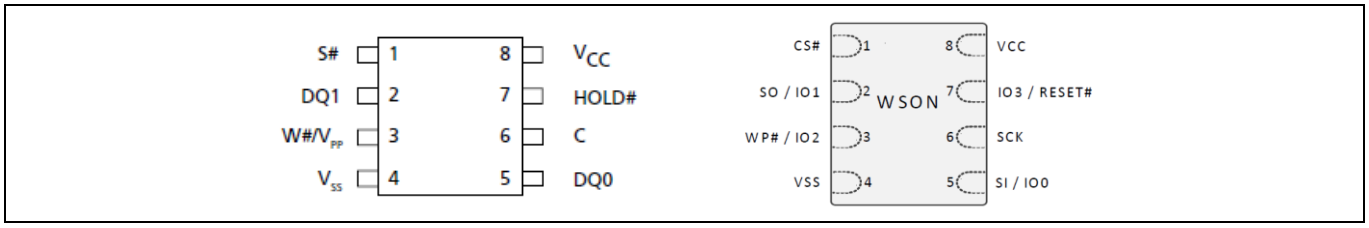
Feature	Micron	Infineon Options
		Automotive, AEC-Q100 Grade 2 -40°C to +105°C Automotive, AEC-Q100 Grade 1 -40°C to +125°C

Note with some exceptions, only the matchups are covered in this application note.

The Micron datasheet mentions that automotive-grade versions of M25P128 are available. However, the publicly available datasheet does not list any automotive properties or ordering options, so those options are out-of-scope for this application note.

2 8-Pin Packages and Pinouts

Here are the pinout arrangements of the Micron VFDFPN8 package, on the left, and the Infineon 8-connector WSON 6x8 package, on the right:



Note the matching pins: #1, #2, #4, #5, #6 and #8. For 8-pin packages, there is no standard way to assign WP# (write protection), HOLD# (pause serial communication), or RESET# (reset pin) in the multiplexed pin positions: #3 & #7.

The following sections presume the Infineon QUAD mode and QPI mode are both disabled; i.e., CR1V[1]=0 and CR2V[3]=0, the factory default configuration.

2.1 Pin #3

Starting with pin #3, note that the V_{pp} function (9-V accelerated program or erase) on the Micron part is not supported in the Infineon part.

- If your application uses the V_{pp} function, the 9-V supply to pin #3 must be disabled or disconnected when the Infineon part is used.
- If your application does not use the V_{pp} function, W# = WP# pin operations are compatible; no board changes are required.

That said, there are some additional special considerations for pin #3 on the Infineon part:

- If WP# is unconnected, there is an internal pull-up that guarantees that the write protect function is disabled on pin #3.
- If WP# is connected, Micron and Infineon devices may respond differently to changes in the WP# pin state, depending upon how the Infineon device is configured.

The Micron register protection state depends on the W# pin state and the SRWD register bit state. The following table shows configurations that define the Micron Software Protected Mode (SPM) and the Hardware Protected Mode (HPM):

W#/WP#	SRWD/SRP0	Mode	Register Operations	Array Operations on BP-Protected Region
1	0	SPM	Yes	No
0	0	SPM	Yes	No
1	1	SPM	Yes	No
0	1	HPM	No	No

In SPM, the nonvolatile SWRD and BP bits can be changed. This means that BP bits can be changed at will by software to update the block protection state. HPM is entered when SWRD=1 *and* W# = LOW; in this mode, SWRD and BP bits cannot be changed, so the protection state is locked. Once W# = HIGH, the device enters SPM, wherein the nonvolatile protection state can be changed.

Infineon parts have the same functionality, but with more optionality (see the Infineon datasheet for details). The analogous Infineon control bits are the SRP0 bit and the BP bits. As long as SEC=0, TBPROT=0 and CMP=0

(factory default), M25P128 BP bit controls have the same effect as BP bit controls in S25FL128S. Even though the Infineon datasheet does not label the modes as in the Micron datasheet, the same state transitions are clearly possible.

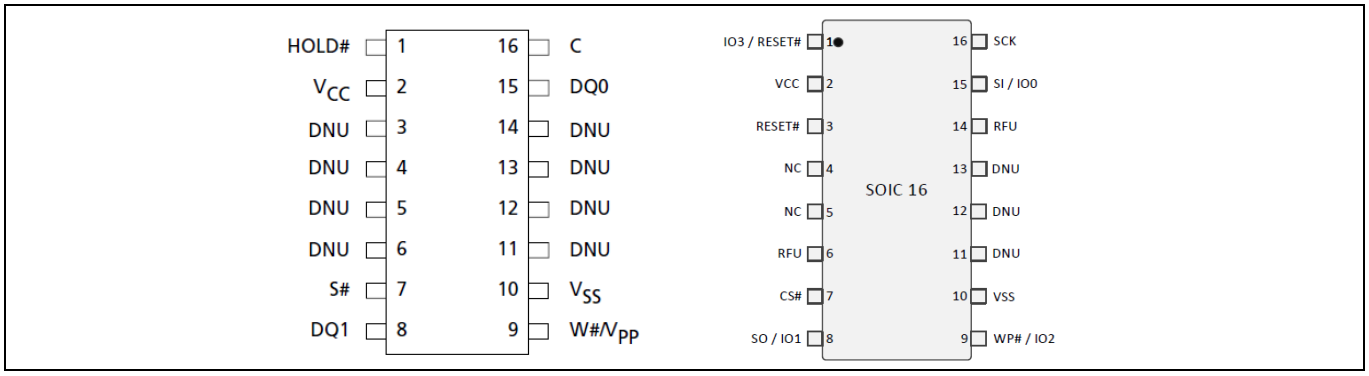
2.2 Pin #7

Given that the Infineon IO3 function on pin #7 is disabled by default, only the Micron HOLD# and the Infineon RESET# functions must be examined for pin #7. These pin functions are not compatible.

If you are using the HOLD# pin function, you know that Micron HOLD# = LOW does not terminate any register write operation, program operation, or erase operation that may be in progress. However, while the Infineon IO3 function on pin #7 is disabled, the Infineon RESET# pin may be activated at any time, and the reset function does terminate register writes, program operations, and erase operations. In this case, the simplest way to manage the incompatibility is to disconnect the Infineon RESET# pin, and let the internal pull-up keep the device out of reset.

3 16-Pin Packages and Pinouts

Here are the pinout arrangements of the Micron SO16W package, on the left, and the Infineon SOIC16 package, on the right.



Note the matching pins: #2, #4, #5, #6, #7, #8, #10, #11, #12, #13, #14, #15 & #16.

As in the last section, we presume the Infineon QUAD mode and QPI mode are both disabled; i.e., CR1V[1]=0 and CR2V[3]=0, the factory default configuration. Now let's examine the differences.

3.1 Pin #1

See the pin #7 discussion in the previous section.

3.2 Pin #3

The Micron pin is "DNU", while the Infineon pin is RESET#. If your application leaves this pin unconnected, the internal pull-up on Infineon pin 3 (RESET#) will ensure that this pin never triggers the reset function.

3.3 Pin #9

See the pin #3 discussion in the previous section.

4 Memory Architecture

The Micron and Infineon device families are both byte-addressable memories; therefore, 128-Mb devices provide identical addressable space for reading.

The programming page sizes are the same – 256 B – so the programming boundaries align for the 128-Mb devices.

However, the erasable units are of different sizes – uniform 256-KB sectors for the Micron device, and uniform 64/32/4-KB erase units for the Infineon device. There is no issue with memory map management for the Micron-to-Infineon migration, because Micron erase units are larger than Infineon erase unit sizes; thus, all erase unit boundaries for the Micron part map to erase unit boundaries for the Infineon part. See the table below for an overview, and refer to the datasheets for more details.

	Micron M25P128	**Infineon S25FL128L**		
Erase Unit Name	Sector	Block	Half-Block	Sector
Erase Unit Size (KB)	256	64	32	4
Erase Unit Count	64	128	246	2048

5 Command Sets

5.1 Addressing Modes

Three-byte addressing is sufficient for up to 128 Mb; the 256-Mb density of the largest Infineon device requires four-byte addressing or a bank addressing method. The Infineon design provides new 4-byte-address commands for this purpose, as well as legacy 3-byte-address commands that can be used in 4-byte mode. A bank addressing method is not provided.

So, if you must migrate the 128-Mb Micron device to a 256-Mb Infineon device, the easiest way to access the entire space is to use the legacy 3-byte-address commands in 4-byte-address mode. Use the ADP bit in the CR2NV[1] register bit location, or the CR2V[1] register bit location, to adjust the address length for legacy commands. If only the low 128 Mb of the 256-Mb device is used, no software changes are required to manage command address arguments. Note, however, that the protection regions on M25P128 will not match with those on S25FL256L.

Thus, if you are migrating to a 128-Mb Infineon device, no software changes are required to manage command address arguments. Also, no register changes are required; the default value of ADP enables 3-byte-addressing.

5.2 Commands and Registers

All Micron commands but one (highlighted yellow) are present in the Infineon devices:

Micron Command	Command Code
Write Enable	06h
Write Disable	04h
Read Identification (1)	9Fh
Read Identification (2)	9Eh
Read Status Register	05h
Write Status Register	01h
Read Data Bytes	03h
Read Data Bytes at Higher Speed	0Bh
Page Program	02h
Sector Erase	D8h
Bulk Erase	C7h

5.3 Read Identification 9Fh

If your software performs a read identification command, ensure that it uses the 9Fh version.

5.4 Read Status Register 05h

The Micron read status register command, 05h, reads the single status register in that device. In the Infineon device, this command reads Status Register 1; specifically, SR1V. Note that all bits in the Micron status register are present in the Infineon Status Register 1; however, the Infineon register also defines additional functions in bit positions 5 and 6. See the Infineon datasheet for details. The Infineon device has many other registers and register read commands; consult the Infineon datasheet for details.

5.5 Write Status Register 01h

The Micron write status register command, 01h, writes one byte to the single status register in that device. In the Infineon device, this command writes one byte each to Status Register 1, Configuration Register 1, Configuration Register 2 and Configuration Register 3. If only one byte of register argument is provided, the Infineon command is nominally equivalent to the Micron command. However, the architecture of the registers is different between the two designs. Namely, the Micron design uses some nonvolatile bits within the register and volatile bits elsewhere; whereas the Infineon design uses a nonvolatile register instance to define the power-on states of the corresponding bits in the volatile register instance. Thus, the single WRR 01h command can be prepared for changing either the volatile or nonvolatile copy of a register by using either the standard write enable command (WREN 06h for nonvolatile register copies) or the volatile write enable command (WRENV 50h for volatile register copies). Thus, the Micron Write Status Register (01h) command is fully compatible with the Infineon 01h command only if it is used to update the nonvolatile instance of Status Register 1.

While it seems like you can get away without changing any software and just manipulate the nonvolatile instance of Status Register 1, updating the nonvolatile registers while the system is not on always-on power, means that the nonvolatile register states are then vulnerable to corruption. The Infineon design provides volatile register instances specifically to avoid corruption of the nonvolatile register copies. So, if your application normally updates nonvolatile registers at runtime, it is a good practice to change this so that your application updates only volatile registers at runtime. The corollary is that nonvolatile registers should be updated only while continuous power is guaranteed – as during production.

5.6 Read 03h

The Micron version of this command is valid up 33 MHz, while the Infineon version is valid up to 50 MHz.

5.7 Fast Read 0Bh

The Micron version of this command is valid up to 54 MHz, while Infineon version is valid up to 108 MHz for the 64-Mb device, and 133 MHz for the 128/256-Mb devices.

	Typ	Max
Micron Read Current @ 50 MHz (mA)		6
Infineon SDR Read Current @ 50 MHz (mA)	15	20
Infineon SDR Read Current @ 108 MHz (mA)	20	25
Infineon SDR Read Current @ 133 MHz (mA)	22	30

5.8 Page Program 02h

Both devices provide the WIP bit for embedded algorithm polling status.

	Typ	Max
Micron 256B Program Time (µs)	500	5000
Infineon 256B Program Time (µs) 64 Mb	450	1350
Infineon 256B Program Time (µs) 128/256 Mb	300	1200
Micron Programming Current (mA)		20
Infineon Programming Current (mA) 64 Mb	17	25
Infineon Programming Current (mA) 128/256 Mb	40	50

5.9 Erase D7h

Both devices provide the WIP bit for embedded algorithm polling status.

	Typ	Max
Micron 256 Kb Sector Erase Time (ms)	1600	3000
Infineon 4x64 Kb Block Erase Time (ms) 64 Mb	1800	4600
Infineon 4x64 Kb Block Erase Time (ms) 128/256 Mb	1080	2900
Micron Erase Current (mA)		20
Infineon Erase Current (mA) 64 Mb	15	25
Infineon Erase Current (mA) 128/256 Mb	25	35

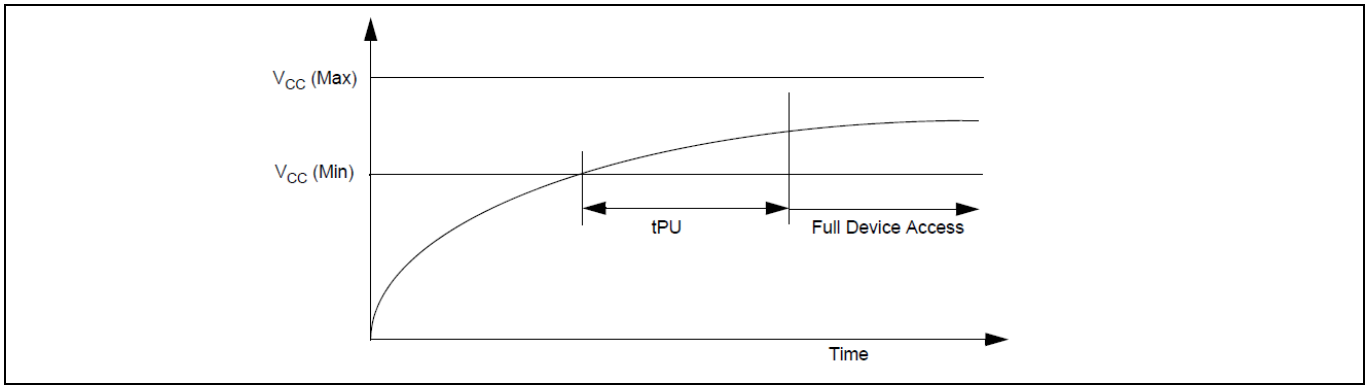
5.10 Bulk Erase C7h

Both devices provide the WIP bit for embedded algorithm polling status.

	Typ	Max
Micron 128 Mb Bulk Erase Time (s)	130	250
Infineon 128 Mb Bulk Erase Time (s)	70	180

6 Power-up, Standby, Deep Power Down

The power-up curves from zero volts, with critical voltages and timings are similar for Micron and Infineon devices. Here is the power-up curve from the Infineon datasheet:

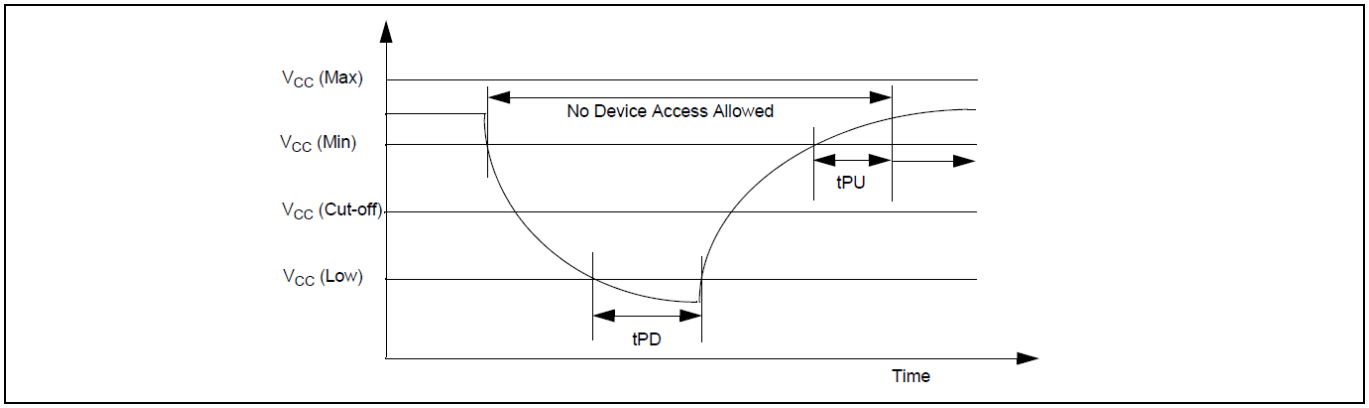


For both devices, the chip must not be selected until enough time has elapsed to allow full device access. This start-up period is around 300-400 µs for both devices. The start-up time periods are measured differently, so they are not directly comparable; see the datasheets for details.

For decaying V_{cc}, both devices have a minimum voltage below which the device terminates embedded operations and stops responding to commands.

	Min	Max
Micron V_{WI} Write Inhibit Voltage (V)	1.5	2.5
Infineon V_{CC}(cut-off) Re-initialization Voltage (V)	2.4	

Both datasheets require reinitialization if the voltage drops below the cutoff voltage. The only available reinitialization is Power-On Reset (POR). The Micron datasheet implies POR involves V_{CC} decay to zero volts (this is not explicitly called out), followed by the specified power-up profile. The Infineon datasheet specifies that POR involves V_{CC} decay to a low, non-zero voltage (V_{CC}(low) = 1.0 V) for a minimum amount of time (t_{PD} = 10 µs), followed by the specified power-up profile. Here is the POR cycle from the Infineon datasheet:



The following table shows power-up, standby, and deep power-down currents. Note that the Micron part does not provide a deep power-down mode. In the Infineon part, this mode is accessed via the Deep Power Down command DPD (B9h), and the Release from Deep Power Down command RES (ABh). See the Infineon datasheet for more details.

Power-up, Standby, Deep Power Down

	Typ	Max
Micron POR Current (mA)		Not specified
Infineon POR Current (mA) 64 Mb	3	5
Infineon POR Current (mA) 128/256 Mb	15	30
Micron Standby Current (µA)		100
Infineon Standby Current (µA) 64 Mb	20	30
Infineon Standby Current (µA) 128/256 Mb	20	35
Infineon Deep Power-Down Current (µA)	2	20

7 Endurance and Data Retention

Endurance and data retention are inversely proportional, so the maximums for each do not occur at the same point. This is clearly shown in the Infineon specification, where the yellow highlights show the comparable values in the Micron specification.

The Infineon specification also lists the minimum program/erase cycle count for the nonvolatile instances of registers. The best practice is to ensure that high write-cycle loads are applied to the volatile register instances.

	Min Endurance (Program/Erase Cycles per Sector)	Min Data Retention (Years)
Micron	100K	20
Infineon	10K 100K	20 2
Infineon Registers	1K	

8 Summary

Migrating from Micron M25P128 to the Infineon S25FL-L family is a straightforward exercise, once the following points are reviewed:

- Both parts provide compatible packages, voltages, densities, temperature ranges, endurance, and data retention.
- The Micron V_{PP} pin function is not available on the Infineon part; board or software modifications may be required to disable the 9-V supply.
- Micron protection modes can be duplicated in the Infineon part.
- The Micron HOLD# pin function is not available in the Infineon part; and the Infineon RESET# pin function provided on the same pin is not compatible. Some board or software adaption may be required.
- All Micron commands, except one, are supported in the Infineon command set; but there is an alternate command that can be used in both devices.
- Sector sizes don’t match, but any erase boundary in the Micron part maps to an erase boundary in the Infineon part; so, no memory map changes are required. Software changes are required to support reprogramming the smaller Infineon flash sectors.
- Addressing modes are compatible (3-byte-addressing), unless you need to migrate to the S25FL256L (4-byte-addressing). In this case, software changes are required to access the upper 128-Mb bank.
- The Infineon device has multiple status registers and configuration registers, vs. the single status register on the Micron part. These differences may require software changes.
- The same Micron single-I/O data transfer speeds are available in the Infineon single-I/O and Single Data Rate (SDR) transfer modes.
- Programming commands and write buffer sizes require no software changes. There are timing differences that may affect software.
- Erase commands require software changes to accommodate the smaller Infineon sector sizes. There are timing differences that may affect software.
- Operating currents are different for the two devices; review the datasheets.
- POR requirements are compatible; any Micron-compatible POR is also compatible with Infineon POR.

References

Note: *Please refer to these datasheets while reading this application note, because only key similarities and differences are highlighted here; full details are in the datasheets.*

[1] **M25P128 Serial Flash Embedded Memory, CCMTD-1718347970-10412 m25p_128.pdf - Rev. A 11/16 EN**.

[2] **S25FL064L 64-Mbit (8-Mbyte) 3.0 V FL-L SPI Flash Memory, 002-12878 Rev. *F**.

[3] **S25FL256L/S25FL128L 256-Mb (32-MB)/128-Mb (16-MB), 3.0 V FL-L Flash Memory, 002-00124 Rev. *H**.

Revision history

Document version	Date of release	Description of changes
**	2018-12-21	New Application Note
*A	2021-05-06	Updated to Infineon template

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