Migration from Micron M29W/M28W to Infineon S29GL-S NOR Flash Family

About this document

Scope and purpose

This application note provides guidelines for migrating from Micron M29W/M28W to Infineon S29GL-S NOR Flash families.

Intended audience

This is intended for Infineon NOR flash memory users who intend to migrate from Micron M29W/M28W to Infineon S29GL-S NOR Flash families.

Table of contents

1 Introduction

This application note provides guidelines for migrating from Micron M29W and M28W to Infineon S29GL-S NOR Flash families.

The discussions will focus on same-density migrations, specifically the cases when migrating from M29W to S29GL-S, and from the M28W to S29GL-S. Considerations on migration to and from other densities can be extrapolated from these discussions. This application note is based on information currently available from data sheets and other application notes publicly available from Infineon and Micron. You should also see the latest relevant specifications.

2 Feature Comparison

Table 1 shows a feature comparison summary of the Micron M29W, M28W flash memory device to the Infineon S29GL-S MirrorBit™ flash family device.

Table 1 General Feature Comparison

Products	M29W	M28W	S29GL-S	Migration Issue
Process Node	65 nm	65 nm	65 nm	No
V_{CC}	2.7 ~ 3.6 V	2.7 ~ 3.6 V	2.7 ~ 3.6 V	No
V_{IO}	1.65 ~ 3.6 V	N/A	1.65 ~ V_{CC} V	No
Random Access Time	128 Mbit: 60 ns, 70 ns, 80 ns 256 Mbit: 60 ns, 70 ns, 80 ns 512 Mbit: 80 ns, 90 ns	70ns	Density: V_{CC}=V_{IO}/Versatile I/O 128 Mbit: 90 ns/100 ns 256 Mbit: 90 ns/100 ns 512 Mbit: 100 ns/110 ns 1 Gbit: 100 ns/110 ns	Maybe
Page Access Time	25 ns, 30 ns	25 ns	Density: V_{CC}=V_{IO}/Versatile I/O 128 Mbit: 15 ns/25 ns 256 Mbit: 15 ns/25 ns 512 Mbit: 15 ns/25 ns 1 Gbit: 15 ns/25 ns	No
Test Condition (Output Load Capacitance)	30 pF	50 pF	30 pF	No
Buffer Programming	70 µs (Typ.) per 64 bytes	10 us (Typ.) per 16 bytes	451 us (Typ.) per 512 bytes	No
Sector Erase (128 KB)	500 ms (Typ.)	1000 ms (Typ.)	535 ms (Typ.)	No
Active Read at 5 MHz, 30 pF	10 mA	9 mA	60 mA	Maybe
Program Current Consumption	20 mA	10 mA	100 mA	Maybe
Erase Current Consumption	20 mA	10 mA	100mA	Maybe
Standby Current Consumption	100 µA (Grade 6) 200 µA (Grade 3)	15 µA	100 µA (+85°C) 200 µA (+105°C) 215 µA (+125°C)	Maybe
Density				
64 Mbit	Yes	Yes	Yes	No
128 Mbit	Yes	No	Yes	No
256 Mbit	Yes	No	Yes	No
512 Mbit	Yes	No	Yes	No
1024 Mbit	No	No	Yes	No
Sector Architecture				
Parameter Block	No	Yes	No	Maybe

Feature Comparison

Products	M29W	M28W	S29GL-S	Migration Issue
Uniform (128 KB)	Yes	No	Yes	No
Access				
x8 Data Bus Width	Yes	Yes	No	Maybe
x16 Data Bus Width	Yes	Yes	Yes	No
Asynchronous	Yes	Yes	Yes	No
Read Page Mode	Yes	Yes	Yes	No
Read Page Size	16 bytes	8 bytes	32 bytes	No
Write Buffer Size	64 bytes	16 bytes	512 bytes	No
Security				
Individual Sector Protection	Yes	No	Yes	No
Secure Silicon OTP Area	256 bytes	16 bytes	2 × 512 bytes	No
Other				
12V Accelerated Programming	Yes	No	No	Maybe
Unlock Bypass Command	Yes	No	No	Maybe
Multi-Sector Erase	Yes	No	No	Maybe
Blank Check	No	No	Yes	No
Suspend/Resume	Yes	Yes	Yes	No
Device ID	Yes	No	Yes	No
Autoselect Access	Yes	No	Yes	No
CFI	Yes	Yes	Yes	No
Status via Data Polling	Yes	Yes	Yes	No
Status via Status Register	Yes	Yes	Yes	No
Packaging and Ordering Options				
48-pin TSOP	No	Yes	No	Maybe
56-pin TSOP	Yes	No	Yes	No
64-ball FAA BGA 10 x 13 mm	Yes	No	No	Maybe
64-ball LAA BGA 11 x 13 mm	Yes	No	Yes	No
64-ball LAE BGA 9 x 9 mm	No	No	Yes	No
56-ball VBU BGA 9 x 7 mm	No	No	Yes	No

2.1 Density

M29W/M28W families are available in monolithic 64, 128, 256, and 512 Mbit densities. S29GL-S family is available in monolithic 64, 128, 256, 512, and 1024 Mbit densities.

2.2 Sector Architecture

S29GL-S and M29W families have 128-KB uniform sectors while the M28W family has 64-KB uniform and total eight of 8-KB parameter sectors. Modifications are required if software was structured to M28W parameter sector architecture.

2.3 Data Bus Width

S29GL-S only supports x16 data bus width. The BYTE# input on previous generations of MirrorBit GL devices (Pin 53 on 56-TSOP and Pad F7 on 64-BGA) will be reserved for future use on the S29GL-T. The BYTE# input on existing designs should be pulled high to force operation in x16 data mode to enable migration to S29GL-S.

2.4 Read Page Size

S29GL-S has a 32-byte read page buffer, which is double the depth of M29W (four times the depth of M28W) to facilitate larger processor cache line fill operations. No software modifications are required to operate with 32-byte maximum page transfers supported by S29GL-S. Software can be modified to take advantage of the deeper read page buffer on S29GL-S by querying the CFI programming buffer depth register at address 4Ch (x16 address bus reference) and configuring software to perform additional page read cycles.

2.5 Write Buffer Size

S29GL-S has a 512-byte write buffer, eight times the depth of the existing M29W. No software modifications are required to continue use of a 64-byte write buffer fill supported by M29W. Software can be modified to take advantage of the deeper write buffers by querying the CFI programming buffer depth register at address 2Ah (x16 address bus reference) and configuring software to perform larger buffer fills.

2.6 Synchronous Mode

M29W, M28W, and S29GL-S devices do not support synchronous mode operation.

2.7 Asynchronous Mode

All the devices support asynchronous mode. S29GL-S supports asynchronous single and page read modes. Software can be modified to take advantage of the wider read page buffer on S29GL-S by querying the CFI programming buffer depth register at address 4Ch (x16 address bus reference) and configuring software to perform additional page read cycles.

2.8 Secure Silicon OTP Area

The Secure Silicon Region (SSR) provides an extra flash memory area that can be programmed once and permanently protected from further changes i.e. it is a One Time Program (OTP) area. The SSR is 1024 bytes in length. It consists of 512 bytes for Factory Locked Secure Silicon Region and 512 bytes for Customer Locked Secure Silicon Region.

The sector address supplied during the Secure Silicon Entry command selects the Flash Memory Array sector that is overlaid by the Secure Silicon Region address map.

The SSR is overlaid starting at location 0 in the selected sector. Use of the Sector 0 address is recommended for future compatibility. While the SSR ASO is entered the content of all other sectors is undefined. Locations above the maximum defined address of the SSR ASO to the maximum address of the selected sector have undefined data.

2.9 Sector Protection

M29W supports Volatile/Nonvolatile Protection through block locking that has a different method than S29GL-S. S29GL-S supports Advanced Sector Protection (ASP) program and erase protection via password, non-volatile and volatile control. Details of ASP program and erase protection implementations can be found in S29GL-S data sheets.

2.10 Program Erase Suspend and Resume

M29W and M28W support program erase suspend and resume in the same way as S29GL-S.

2.11 Data Polling

M29W and S29GL-S support data polling. These are referred to as DQ bits as they appear on the data bus during a read access while an embedded algorithm is in progress. DQ bits 15 to 8, DQ4, and DQ0 are reserved and provide undefined data. Status monitoring software must mask the reserved bits and treat them as don't care.

Note that data polling may not be supported on future smaller process MirrorBit GL flash families. Status Register reads will be required to determine the status of embedded program and erase operations if data polling is not supported.

2.12 Accelerated Programming

S29GL-S does not support accelerated programming while the M29W supports accelerated programming.

3 Package Comparison

There are different pinouts and ballouts between M29W and S29GL-S regarding TSOP and BGA, as shown in **Figure 1** through **Figure 5**.

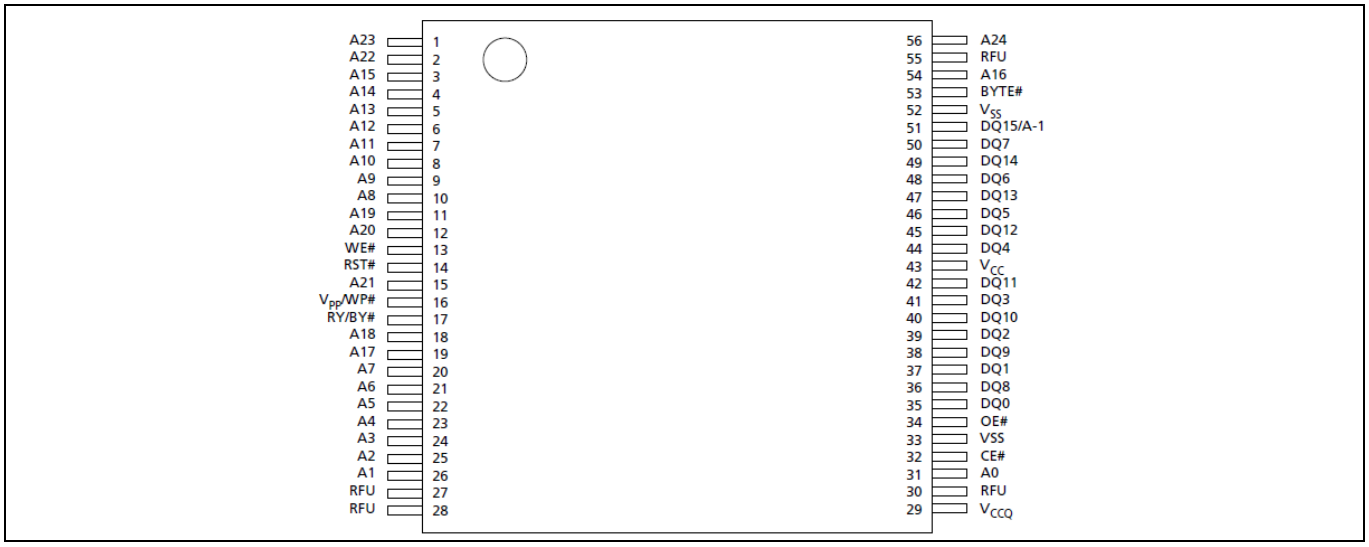

Figure 1 512 Mbit M29W 56-Lead TSOP

Note:

1. *A24 = A[MAX].*
2. *A-1 is the least significant address bit in x8 mode.*

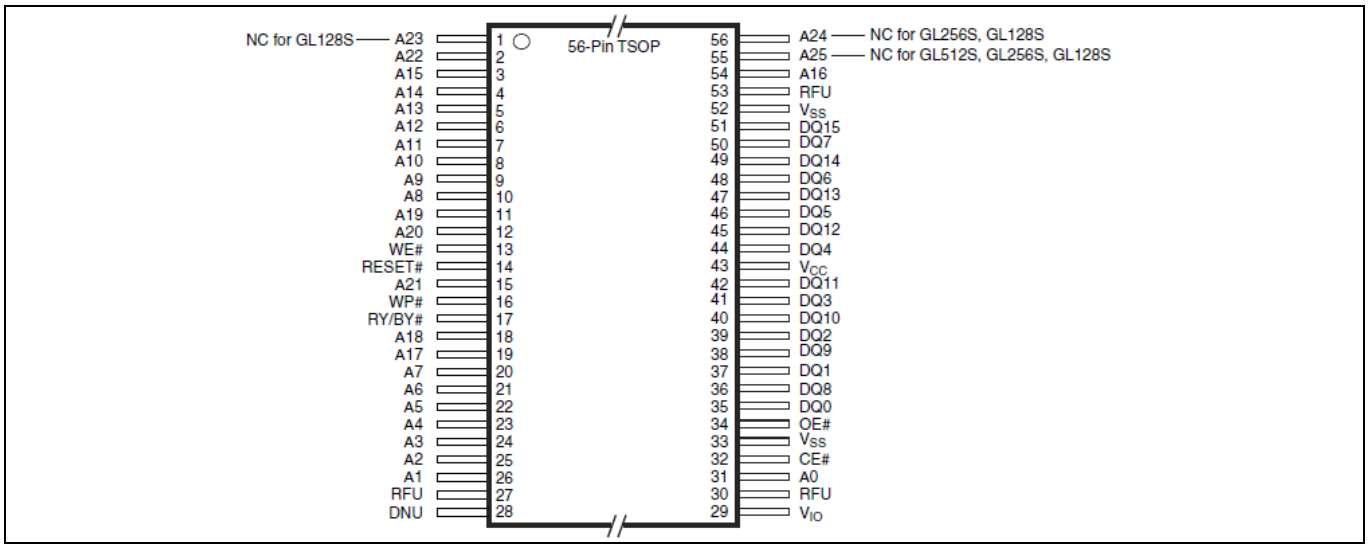

Figure 2 Figure. S29GL-S 56-Lead TSOP

Note:

1. *Pin 28, Do Not Use (DNU), a device internal signal is connected to the package connector. The connector may be used by Infineon for test or other purposes and is not intended for connection to any host system signal. Do not*

use these connections for PCB Signal routing channels. Though not recommended, the ball can be connected to VCC or VSS through a series resistor.

2. *Pin 27, 30, and 53 Reserved for Future Use (RFU).*

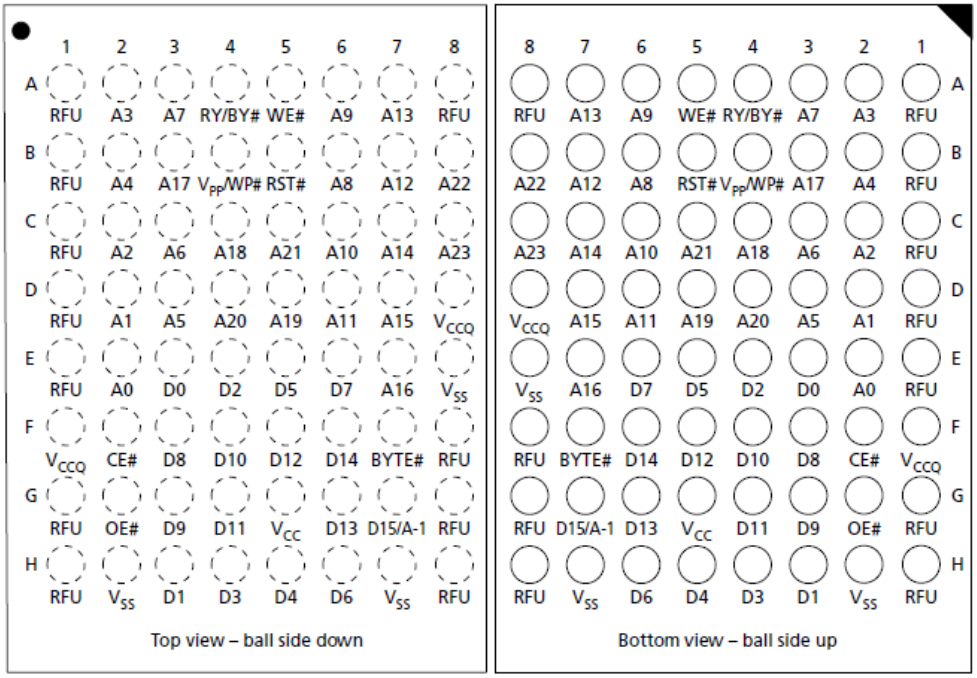

Figure 3 256Mbit M29W 64-ball Fortified BGA and 64-Ball TBGA

Note:

1. *A23 = A[MAX].*
2. *A-1 is the least significant address bit in x8 mode.*

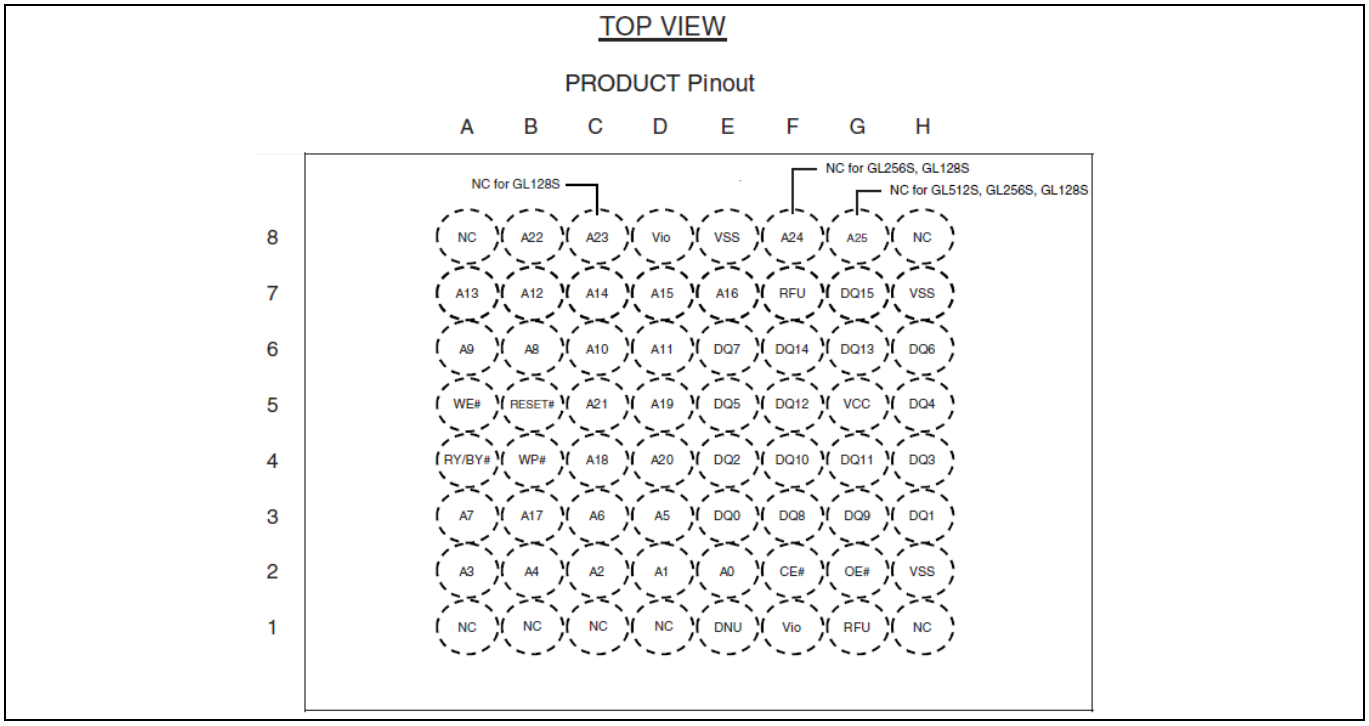

Figure 4 S29GL-S 64-Ball Fortified BGA

Note:

1. *Ball E1, Do Not Use (DNU), a device internal signal is connected to the package connector. The connector may be used by Infineon for test or other purposes and is not intended for connection to any host system signal. Do not use these connections for PCB Signal routing channels. Though not recommended, the ball can be connected to VCC or VSS through a series resistor.*
2. *Balls F7 and G1, Reserved for Future Use (RFU).*
3. *Balls A1, A8, C1, D1, H1, and H8, No Connect (NC).*

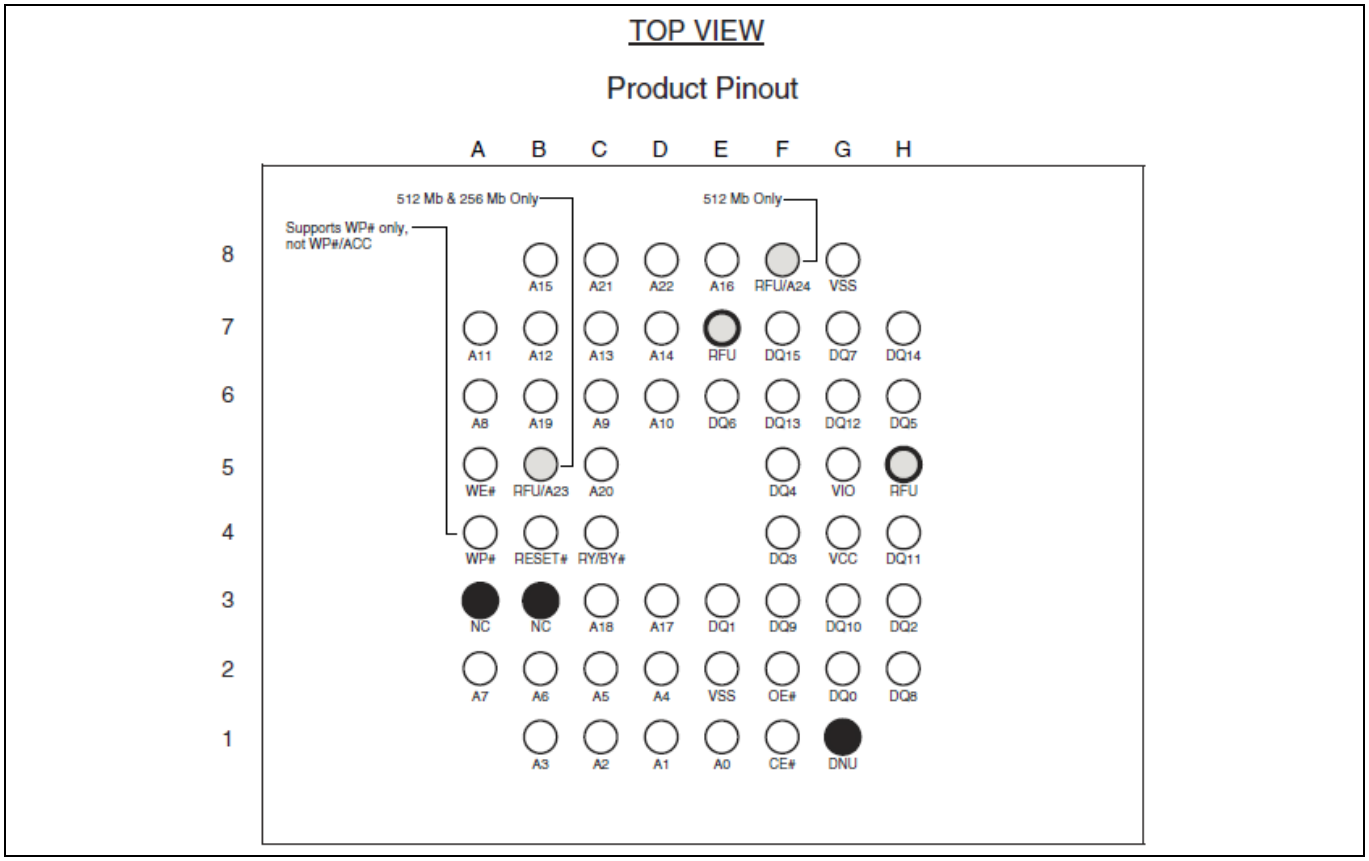

Figure 5 S29GL-S 56-Ball Fortified BGA

Note:

1. *Ball G1, Do Not Use (DNU), a device internal signal is connected to the package connector. The connector may be used by Infineon for test or other purposes and is not intended for connection to any host system signal. Do not use these connections for PCB Signal routing channels. Though not recommended, the ball can be connected to VCC or VSS through a series resistor.*
2. *Balls E7, F8, and H5, Reserved for Future Use (RFU).*
3. *Balls A3 and B3, No Connect (NC).*

4 Signal Comparison

Table 2 shows a signal comparison summary of Infineon S29GL-S to M29W/M28W.

Table 2 Signal Comparison

M29W/M28W		S29GL-S	
Symbol	**Description**	**Symbol**	**Description**
RESET#	Hardware Reset	RESET#	Hardware Reset
CE#	Chip Enable	CE#	Chip Enable
OE#	Output Enable	OE#	Output Enable
WE#	Write Enable	WE#	Write Enable
A_{MAX}–A0	Address inputs A24–A0 for 512Mbit A23–A0 for 256Mbit A22–A0 for 128 Mbit A21–A0 for 64 Mbit	A_{MAX}–A0	Address inputs A25–A0 for S29GL01GS A24–A0 for S29GL512S A23–A0 for S29GL256S A22–A0 for S29GL128S A21–A0 for S29GL064S
DQ15–DQ0	Data inputs and outputs	DQ15–DQ0	Data inputs and outputs
V_{PP}/WP#	V_{PP}/Write Protect	WP#	Write Protect
BYTE#	Byte/Word organization select (M29W only)	–	–
RY/BY#	Ready/Busy	RY/BY#	Ready/Busy
V_{CC}	Supply voltage	V_{CC}	Core power supply
V_{CCQ}	I/O supply voltage (M29W only)	V_{IO}	Versatile I/O power supply
V_{SS}	Ground	V_{SS}	Power supplies ground
NC	Not Connected internally	NC	Not Connected internally
RFU	Reserved for Future Use	RFU	Reserved for Future Use
DNU	Do Not Use	DNU	Do Not Use

5 Command Set Comparison

For comparison, M29W/M28W and S29GL-S device commands vary from one to seven bus cycles, as shown in **Table 3** and **Table 4**.

Table 3 M29W/M28W Command Set (x16)

Command and Code/Subcode	Cycles	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
Read and Autoselect Operations														
Read/Reset	1	X	F0											
	3	555	AA	2AA	55	X	F0							
Read CFI	1	55	98											
Autoselect	4	555	AA	2AA	55	555	90	*2	*2					2, 3, 4
Bypass Operations														
Unlock Bypass	3	555	AA	2AA	55	555	20							
Unlock Bypass Reset	2	X	90	X	00									
Program Operations														
Program	4	555	AA	2AA	55	555	A0	PA	PD					
Unlock Bypass Program	2	X	A0	PA	PD									5
Write to Buffer Program	5	555	AA	2AA	55	BAd	25	BAd	N	PA	PD			6, 7, 8
Unlock Bypass Write to Buffer Program	3	BAd	25	BAd	N	PA	PD							5
Write to Buffer Program Confirm	1	BAd	29											
Buffered Program Abort and Reset	3	555	AA	2AA	55	555	F0							
Enter Enhanced Buffered Program	3	555	AA	2AA	55	555	38							
Enhanced Buffered Program	3	BAd	33	BAd	Data	BAd	Data							9
Exit Enhanced Buffered Program	2	X	90	X	00									
Enhanced Buffered Program Abort	3	555	AA	2AA	55	555	F0							
Program Suspend	1	X	B0											
Program Resume	1	X	30											
Erase Operations														

Command Set Comparison

Command and Code/Subcode	Cycles	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10	
Unlock Bypass Chip Erase	2	X	80	X	10									5
Block Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	BAd	30	10
Unlock Bypass Block Erase	2	X	80	BAd	30									5
Erase Suspend	1	X	B0											
Erase Resume	1	X	30											

Note:

1. *A = Address; D = Data; X = Don't Care; BAd = Any address in the block; N = Number of bytes to be programmed; PA = Program Address; PD = Program Data; Gray shading = Not applicable. All values in the table are hexadecimal. Some commands require both a command code and subcode.*
2. *These cells represent read cycles (versus write cycles for the others).*
3. *Autoselect enables the device to read the Device ID, Block Protection Status, and Extended Memory Block Protection Indicator.*
4. *Autoselect addresses and data are specified in **Table 5**.*
5. *For any Unlock-Bypass-Erase/Program command, the first two Unlock cycles are unnecessary.*
6. *BAd must be the same as the address loaded during the Write-to-Buffer Program third and fourth cycles.*
7. *Write-to-Buffer Program operation: maximum cycles = 68 (x8) and 36 (x16). Unlock Bypass Write-to-Buffer Program operation: maximum cycles = 66 (x8) and 34 (x16). Write-to-Buffer Program operation: N + 1 = bytes to be programmed; maximum buffer size = 64 bytes (x8) and 32 words (x16).*
8. *For x8, A[MAX:5] address pins should remain unchanged while A[4:0] and A-1 pins are used to select a byte within the N + 1 byte page. For x16, A[MAX:5] address pins should remain unchanged while A[4:0] pins are used to select a word within the N + 1 word page.*
9. *The following is content for address/data cycles 256 through 258: BAd (FE) - Data; BAd (FF) - Data; BAd (00) - 29.*
10. *Block Erase address cycles can extend beyond six address/data cycles, depending on the number of blocks to erase.*

Table 4 S29GL-S Major Command Set (x16)

Command Sequence *1	Cycles	Address and Data Cycles											
		1st		2nd		3rd		4th		5th		6th	
		A	D	A	D	A	D	A	D	A	D	A	D
Read *6	1	RA	RD										
Reset/ASO Exit *7, *16	1	XXX	F0										
Status Register Read	2	555	70	XXX	RD								
Status Register Clear	1	555	71										
Word Program	4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer	6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD
Program Buffer to Flash	1	SA	29										

Command Set Comparison

Command Sequence [*1]	Cycles	Address and Data Cycles											
		1st		2nd		3rd		4th		5th		6th	
		A	D	A	D	A	D	A	D	A	D	A	D
Write-to-Buffer-Abort Reset [*11]	3	555	AA	2AA	55	555	F0						
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend/Program Suspend Legacy Method [*9]	1	XXX	B0										
Erase Suspend Enhanced Method	1	XXX	B0										
Erase Resume/Program Resume Legacy Method [*10]	1	XXX	30										
Erase Resume Enhanced Method	1	XXX	30										
Program Suspend Enhanced Method	1	XXX	51										
Program Resume Enhanced Method	1	XXX	50										
Blank Check	1	(SA) 55	33										
ID-CFI (Autoselect) ASO													
ID (Autoselect) Entry	3	555	AA	2AA	55	(SA) 555	90						
CFI Enter [*8]	1	(SA) 55	98										
ID-CFI Read	1	RA	RD										
Reset/ASO Exit [*7, *16]	1	XXX	F0										

Legend:

X = Don't care.

RA = Address of the memory to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed.

PD = Data to be programmed at location PA.

SA = Address of the sector selected. Address bits AMAX–A16 uniquely select any sector.

WBL = Write Buffer Location. The address must be within the same Line.

WC = Word Count is the number of write buffer locations to load minus 1.

PWAx = Password address for Word 0 = 00h, Word 1 = 01h, Word 2 = 02h, and Word 3 = 03h.

PWDx = Password data Word 0, Word 1, Word 2, and Word 3.

Command Set Comparison

Note:

1. *See Interface States for description of bus operations on the S29GL-S datasheet.*
2. *All values are in hexadecimal.*
3. *Except for the following, all bus cycles are write cycle: read cycle during Read, ID/CFI Read (Manufacturing ID / Device ID), Indicator Bits, Secure Silicon Region Read, SSR Lock Read, and 2nd cycle of Status Register Read.*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD, PD, WC and PWD.*
5. *Address bits AMAX–A11 are don't care for unlock and command cycles, unless SA or PA required. (AMAX is the highest address pin.).*
6. *No unlock or command cycles required when reading array data.*
7. *The Reset command is required to return to reading the array data when the device is in the ID-CFI (Autoselect) mode, or if DQ5 goes HIGH (while the device is providing the status data).*
8. *The command is valid when the device is ready to read array data or when device is in ID-CFI (Autoselect) mode.*
9. *The system can read and program/program suspend in non-erasing sectors, or enter the ID-CFI ASO, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
10. *The Erase Resume/Program Resume command is valid only during Erase Suspend/Program Suspend modes.*
11. *Issue this command sequence to return to read mode after detecting device is in a Write-to-Buffer-Abort state.* ***IMPORTANT:*** *The full command sequence is required if resetting out of ABORT.*
12. *The Exit command returns the device to reading the array.*
13. *The password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.*
14. *For PWDx, only one portion of the password can be programmed per each A0 command. Portions of the password must be programmed in sequential order (PWD0–PWD3).*
15. *All Lock Register bits are one-time programmable. The program state = 0 and the erase state = 1. Also, both the Persistent Protection Mode Lock Bit and the Password Protection Mode Lock Bit cannot be programmed at the same time; the Lock Register Bits Program operation aborts and returns the device to read mode if you attempt this. Lock Register bits that are reserved for future use are undefined.*
16. *If any of the Entry commands was issued, an Exit command must be issued to reset the device into read mode.*
17. *Protected State = 00h, Unprotected State = 01h. The sector address for DYB set, DYB clear, or PPB Program command may be any location within the sector - the lower order bits of the sector address are don't care.*

6 Device ID Comparison

This section provides a comparison between Micron and Infineon flash memory Device ID.

Table 5 Device ID Comparison

			Infineon	**Micron**
		Address (x16)	**S29GL512S**	**M29W 512 Mbit**
Manufacturer ID		(Base)+00h	0001h	0020h
Device ID	Word 1	(Base)+01h	227Eh	227Eh
	Word 2	(Base)+0Eh	2223h	2222h
	Word 3	(Base)+0Fh	2201h	2201h
			Infineon	**Micron**
		Address (x16)	**S29GL256S**	**M29W 256 Mbit**
Manufacturer ID		(Base)+00h	0001h	0020h
Device ID	Word 1	(Base)+01h	227Eh	227Eh
	Word 2	(Base)+0Eh	2222h	2222h
	Word 3	(Base)+0Fh	2201h	2201h
			Infineon	**Micron**
		Address (x16)	**S29GL128S**	**M29W 128 Mbit**
Manufacturer ID		(Base)+00h	0001h	0020h
Device ID	Word 1	(Base)+01h	227Eh	227Eh
	Word 2	(Base)+0Eh	2221h	2221h
	Word 3	(Base)+0Fh	2201h	2201h

7 Status Register Comparison

M29W supports Status Register reads as an alternative method to data polling to determine the embedded operation status. The Status Register feature is also supported on S29GL-S family. The 16-bit Status Register is accessed via a two-cycle sequence consisting of a Read Status Register Command write cycle followed immediately by a read cycle to the same targeted sector address. Using the Status Register is advantageous because, unlike legacy data polling, software does not need to track active address regions or compare sequential polling read values to determine embedded algorithm status; one Status Register access provides all the information necessary to determine the flash state. A Clear Status Register command is available to reset the last completed embedded operation portion of the Status Register.

Status Register usage is optional. If required, software can be modified to take advantage of this feature by querying the Lower Software Bits at offset 000Ch in Autoselect mode. If Bit 0 is set, the Status Register functionality is supported. Details of the Status Register implementation are provided in the S29GL-S datasheet.

The Status Register contains bits related to the results – success or failure – of the most recently completed Embedded Algorithms (EA) and bits related to the current state of any EA in process:

- Erase Status (Bit 5)
- Program Status (Bit 4)
- Write Buffer Abort (Bit 3)
- Sector Locked Status (Bit 1)
- RFU (Bit 0)

Current State of EA in Process:

- Device Busy (Bit 7)
- Erase Suspended (Bit 6)
- Program Suspended (Bit 2)

The Current State bits indicate whether an EA is in process, suspended, or completed. The upper eight bits (Bits 15:8) are reserved. These have undefined HIGH or LOW value that can change from one status read to another. These bits should be treated as don't care and ignored by any software reading the status. The Soft Reset Command will clear bits [5, 4, 1, 0] of the status register to 0 if Status Register Bit 3 =0. This will not affect the current state bits. The Clear Status Register command will clear the results-related bits of the status register to 0, but will not affect the Current State bits.

Table 6 M29W Status Register

Bit	Name	Settings	Description	Note
DQ7	Data Polling Bit	0 or 1, depending on operations	Monitors whether the program/erase has successfully completed its operation, or has responded to an Erase Suspend operation.	2, 3, 4
DQ6	Toggle Bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors whether the program/erase has successfully completed its operations, or has responded to an Erase Suspend operation. During a Program/Erase operation, DQ6 toggles from 0 to 1, 1 to 0, and so on, with each successive read operation from any address.	3, 4, 5
DQ5	Error Bit	0 = Success 1 = Failure	Identifies errors detected by the program/erase. DQ5 is set when a Program, Block Erase, or Chip Erase operation fails to write the correct data to the memory.	4, 6

Status Register Comparison

Bit	Name	Settings	Description	Note
DQ3	Erase Timer Bit	0 = Erase not in progress 1 = Erase in progress	Identifies the start of program/erase operation during a Block Erase command. Before the program/erase controller starts, this bit set to 0, and additional blocks to be erased can be written to the command interface.	4
DQ2	Alternative Toggle Bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors the program/erase during Erase operations. During Chip Erase, Block Erase, and Erase Suspend operations, DQ2 toggles from 0 to 1, 1 to 0, and so on, with each successive read operation from addresses within the blocks being erased.	3, 4
DQ1	Buffered Program Abort Bit	1 = Abort	Indicates a buffer program operation abort. The Buffered Program Abort and Reset command must be issued to return the device to read mode.	

Note:

1. *The Status Register can be read during Program, Erase, or Erase Suspend operations; the Read operation outputs data on DQ[7:0].*
2. *For a Program operation in progress, DQ7 outputs the complement of the bit being programmed. For a read operation from the address previously programmed successfully, DQ7 outputs the existing DQ7 data. For a read operation from addresses with blocks to be erased while an Erase Suspend operation is in progress, DQ7 outputs 0; upon a successful completion of the Erase Suspend operation, DQ7 outputs 1. For an erase operation in progress, DQ7 outputs 0; upon either operation's successful completion, DQ7 outputs 1.*
3. *After the successful completion of a Program or Erase operation, the device returns to read mode.*
4. *During Erase Suspend mode, read operations to addresses within blocks not being erased output the memory array data as if in read mode. A protected block is treated in the same way as a block not being erased.*
5. *During Erase Suspend mode, DQ6 toggles when addressing a cell within a block being erased. The toggling stops when the program/erase has suspended the erase operation.*
6. *When DQ5 is set to 1, a Read/Reset command must be issued before any subsequent command.*

Table 7 S29GL-S Status Register

Bit #	15:8	7	6	5	4	3	2	1	0
Bit Description	Reserved	Device Ready Bit	Erase Suspend Status Bit	Erase Status Bit	Program Status Bit	Write buffer Abort Status Bit	Program Suspend Status Bit	Sector Lock Status Bit	Reserved
Bit Name		DRB	ESSB	ESB	PSB	WBASB	PSSB	SLSB	
Reset Status	X	1	0	0	0	0	0	0	0
Busy Status	Invalid	0	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
Ready Status	X	1	0 = No erase in suspension 1 = Erase in suspension	0 = Erase successful 1 = Erase fail	0 = Program successful 1 = Program fail	0 = Program not aborted 1 = Program	0 = No program in suspension 1 = Program in suspension	0 = Sector not locked during operation	X

Bit #	15:8	7	6	5	4	3	2	1	0
						aborted during Write to Buffer command		1 = Sector locked error	

Note:

1. *Bits 15 through 8, and 0 are RFU and may display as 0 or 1. These bits should be ignored (masked) when checking the status.*
2. *Bit 7 is 1 when there is no Embedded Algorithm in progress in the device.*
3. *Bits 6 through 1 are valid only if Bit 7 is 1.*
4. *All bits are put in their reset status by a cold reset or warm reset.*
5. *Bits 5, 4, 3, and 1 are cleared by the Clear Status Register command or Reset command.*
6. *Upon issuing the Erase Suspend Command, you must continue to read the status register until DRB becomes 1.*
7. *ESSB is cleared by the Erase Resume Command.*
8. *ESB reflects the success or failure of the most recent erase operation.*
9. *PSB reflects the success or failure of the most recent program operation.*
10. *During Erase Suspend, programming to the suspended sector, will cause program failure and set the Program status bit.*
11. *Upon issuing the Program Suspend Command, you must continue to read the status register until DRB becomes 1.*
12. *PSSB is cleared by the Program Resume command.*
13. *SLSB indicates that a program or erase operation failed because the sector was locked.*
14. *SLSB reflects the status of the most recent program or erase operation.*

8 DC Specifications

S29GL-S and M29W have primarily compatible specifications. Differences in DC Characteristics between the devices are highlighted in **Table 8**. The potential impact of any parameter specification differences should be evaluated and validated. Refer to the respective Micron M29W and Infineon S29GL-S datasheets to verify the latest specifications.

Table 8 DC Specifications

	Infineon			Micron								
	S29GL-S			M29W 128 Mbit			M29W 256 Mbit			M29W 512 Mbit		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
Input Load Current		+0.02 µA	± 1.0 µA			±1 µA			±1 µA			±1 µA
Output Leakage Current		+0.02 µA	± 1.0 µA			±1 µA			±1 µA			±1 µA
V_{CC} Active Read Current (5 MHz)		55 mA	60 mA			10 mA			10 mA			10 mA
V_{CC} Intra-Page Read Current		9 mA	25 mA			15 mA			1 mA			1 mA
V_{CC} Active Erase/Program Current		45 mA	100 mA			20 mA			20 mA			20 mA
V_{CC} Standby Current		70 µA	100 µA			100 µA			100 µA			200 µA
V_{CC} Reset Current		10 mA	20 mA		1 µA	5 µA		1 µA	5 µA		1 µA	5 µA
Automatic Sleep Mode		3 mA	6 mA									
V_{CC} current during power up		53 mA	80 mA									
Input LOW Voltage	−0.5 V		0.3 × V_{IO} V	−0.5 V		0.3 × V_{IO} V	−0.5 V		0.3 × V_{IO} V	−0.5 V		0.3 × V_{IO} V
Input HIGH Voltage	0.7 × V_{IO} V		V_{IO} + 0.4 V	0.7 × V_{IO} V		V_{IO} + 0.4 V	0.7 × V_{IO} V		V_{IO} + 0.4 V	0.7 × V_{IO} V		V_{IO} + 0.4 V
Output LOW Voltage			0.15 × V_{IO} V			0.15 × V_{IO} V			0.15 × V_{IO} V			0.15 × V_{IO} V
Output HIGH Voltage	0.85 × V_{IO} V			0.85 × V_{IO} V			0.85 × V_{IO} V			0.85 × V_{IO} V		

9 Program or Erase Suspend / Resume

There are specification differences at Program or Erase Suspend / Resume specifications between Micron and Infineon flash memory devices.

Table 9 Program or Erase Suspend / Resume Specification

		Infineon S29GL-S		Micron M29W	
		Typ	**Max**	**Typ**	**Max**
Erase	Erase Suspend latency		50 µs	25 µs	45 µs
Erase Suspend	Erase Resume to next Erase Suspend	100 µs		1 ms	
Program	Program Suspend latency		50 µs	5 µs	15 µs
Program Suspend	Program Resume to next Program Suspend	100 µs			

10 Power Up Timing

This section provides a comparison of power up timings of Micron and Infineon flash memory devices.

Table 10 Power Up Timing Specification

	Infineon	Micron
	S29GL-S	M29W
	Min	Min
V_{CC} setup time to first access	300 µs	55 µs
V_{IO} setup time to first access	300 µs	55 µs
RESET# LOW to CE# LOW during embedded operation	35 µs (Max)	55 µs (Max)
RESET# pulse width during embedded operation	200 ns	20 µs
Time between RESET# HIGH and CE# LOW	50 ns	55 ns

References

[1] Micron Parallel NOR Flash Embedded Memory M29W128GH, M29W128GL datasheet

[2] Micron Parallel NOR Flash Embedded Memory M29W256GH, M29W256GL datasheet

[3] Micron Parallel NOR Flash Embedded Memory M29W512GH70N3E, M29W512GH7AN6E datasheet

[4] Micron 64 Mbit (4 Mb x 16, boot block) 3 V supply Flash memory M28W640HCT, M28W640HCT datasheet

Revision history

Document version	Date of release	Description of changes
**	2018-12-19	Initial release
*A	2021-06-11	Updated to Infineon template

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