Designing with EXCELON™ LP SPI F-RAM low-power modes

About this document

Scope and purpose

This application note provides an overview of the three low-power modes of EXCELON™ low-power (LP) SPI F-RAMs and their use case with examples showing advantages and disadvantages to help when selecting the appropriate low-power mode for power-efficient, battery-operated system designs.

Intended audience

This document is primarily intended for anyone who wants to design low-power modes with EXCELON™ LP SPI F-RAM.

Associated part family

CY15x102Qx, CY15x104Qx, CY15x108Qx

Table of contents

1 Introduction

The EXCELON™ LP SPI F-RAMs offer three low-power modes which include standby (I_{SB}), deep-power-down (I_{DPD}), and hibernate (I_{HIB}). Any of these three-low power modes can be effectively applied in system designs to optimize the system power consumption while the system is either in power saving mode or shutdown, thus can help enhancing the system battery life.

Standby mode is the default low-power mode for the EXCELON™ LP SPI F-RAM when its chip-select ($\overline{CS}$) pin is de-asserted to a logic HIGH to terminate an ongoing device operation. If the device is in standby mode, $\overline{CS}$ transition from HIGH to LOW exits the standby mode and the device is immediately available for access. The deep-power-down or hibernate mode entry is command (opcode) based; therefore, the EXCELON™ LP SPI F-RAM enters either deep-power-down or hibernate mode only after specific command is issued, followed by $\overline{CS}$ transitioning to HIGH.

The deep-power-down or hibernate mode exits when $\overline{CS}$ is de-asserted to logic LOW, like when exiting the standby mode. However, exiting from deep-power-down or hibernate mode is not immediate and exit delay is associated with an internal wake up cycle time. This means that even though the deep-power-down and hibernate modes draw lower currents than standby mode, they may not necessarily offer the lowest total energy consumption always because of the overheads associated with the low-power mode entry and exit timings.

This application note guides you through the details of EXCELON™ LP SPI F-RAM low-power modes, analyzes various use cases, and highlights associated overheads with each low-power mode based upon the system duty cycle to access the EXCELON™ LP SPI F-RAM. Selecting an effective low-power mode of operation of the EXCELON™ LP SPI F-RAM can help reduce the total system power in power-sensitive, battery-operated systems.

2 Low-power modes in EXCELON™ LP F-RAMs

This section describes in detail the three low-power modes supported by EXCELON™ LP SPI F-RAM.

2.1 Standby mode

Standby mode is the default power saving mode when any normal memory operation is inhibited. Standby mode is enabled by de-asserting the chip select pin ($\overline{CS}$) to a logic HIGH. **Figure 1** highlights instances when the EXCELON™ LP SPI F-RAM enters and exits the standby mode.

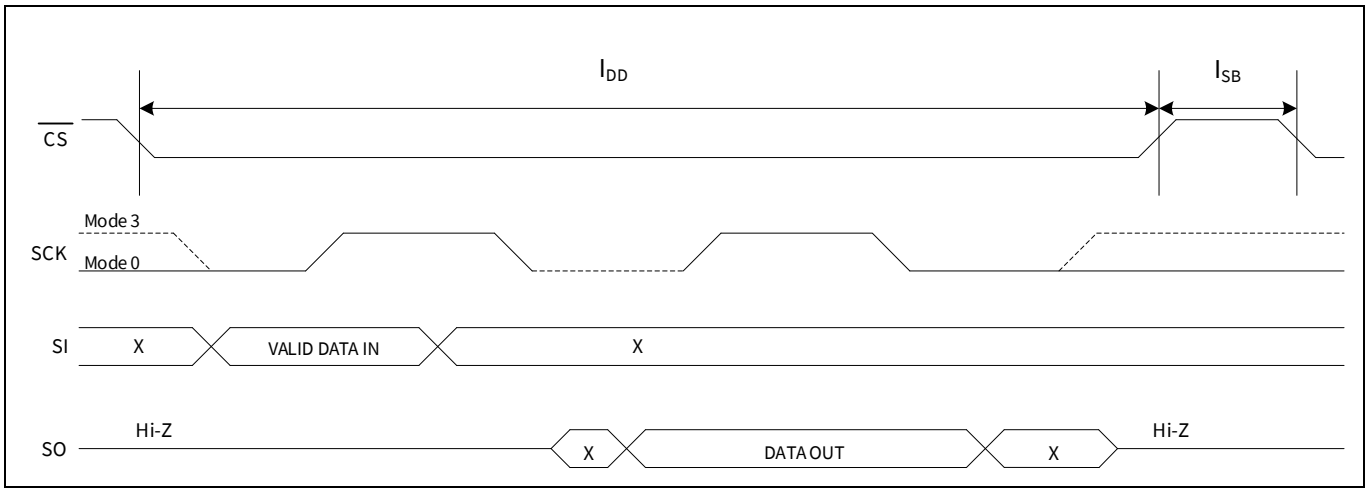

Figure 1 EXCELON™ LP SPI F-RAM standby mode

2.2 Deep-power-down (DPD) mode

Deep-power-down mode is a lower power mode than the standby mode. The EXCELON™ LP SPI F-RAM device enters deep-power-down mode with the Deep Power Down Enable opcode (DPD). Once the device receives the DPD opcode followed by $\overline{CS}$ de-asserted to a logic HIGH, the device current drops to deep-power-down mode current (I_{DPD}) after t_{ENTDPD} time. The device wakes up from deep-power-down mode only after a logic LOW pulse of width t_{CSDPD} (max) is applied on the $\overline{CS}$ pin. It takes t_{EXTDPD} (max) time to wake up from deep-power-down mode. **Table 1** and **Table 2** show EXCELON™ LP SPI F-RAM deep-power-down mode enter and exit timings. **Figure 2** highlights instances when the EXCELON™ LP SPI F-RAM enters and exits deep-power-down mode.

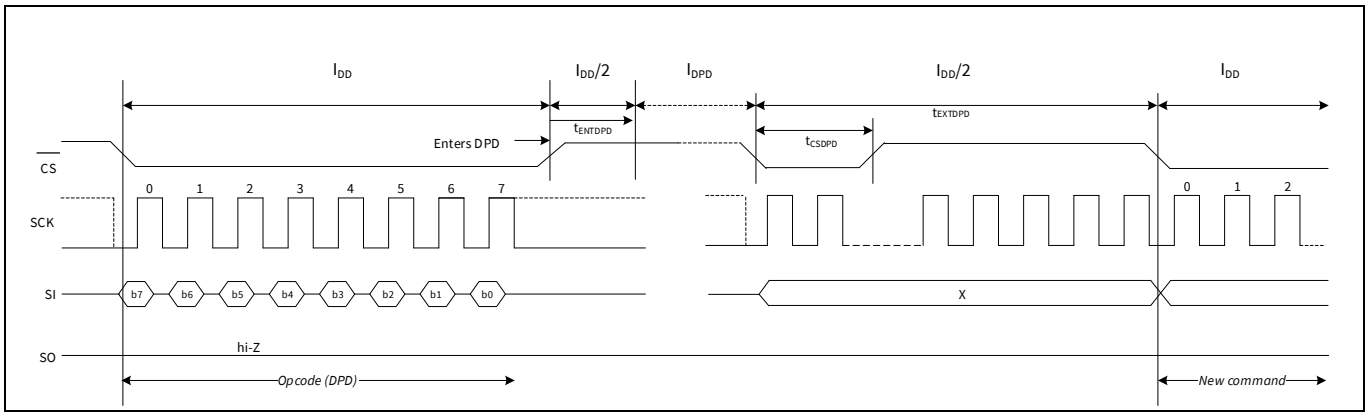

Figure 2 EXCELON™ LP SPI F-RAM deep-power-down (DPD) mode

2.3 Hibernate mode

Hibernate mode is the lowest power mode in EXCELON™ LP SPI F-RAMs. The EXCELON™ LP SPI F-RAM device enters hibernate mode with the hibernate enable opcode (HBN). Once the device receives the HBN command followed by $\overline{CS}$ transitioning to a logic HIGH, the device current drops to hibernate mode current (I_{HIB}) after the t_{ENTHIB} time. The device wakes up from hibernate mode only after the $\overline{CS}$ pin is asserted to a logic LOW. It takes the t_{EXTHIB} (max) time to wake up from hibernate mode. **Table 1** and **Table 2** show EXCELON™ LP SPI F-RAM hibernate mode enter and exit timings. **Figure 3** highlights instances when the EXCELON™ LP SPI F-RAM enters and exits hibernate mode.

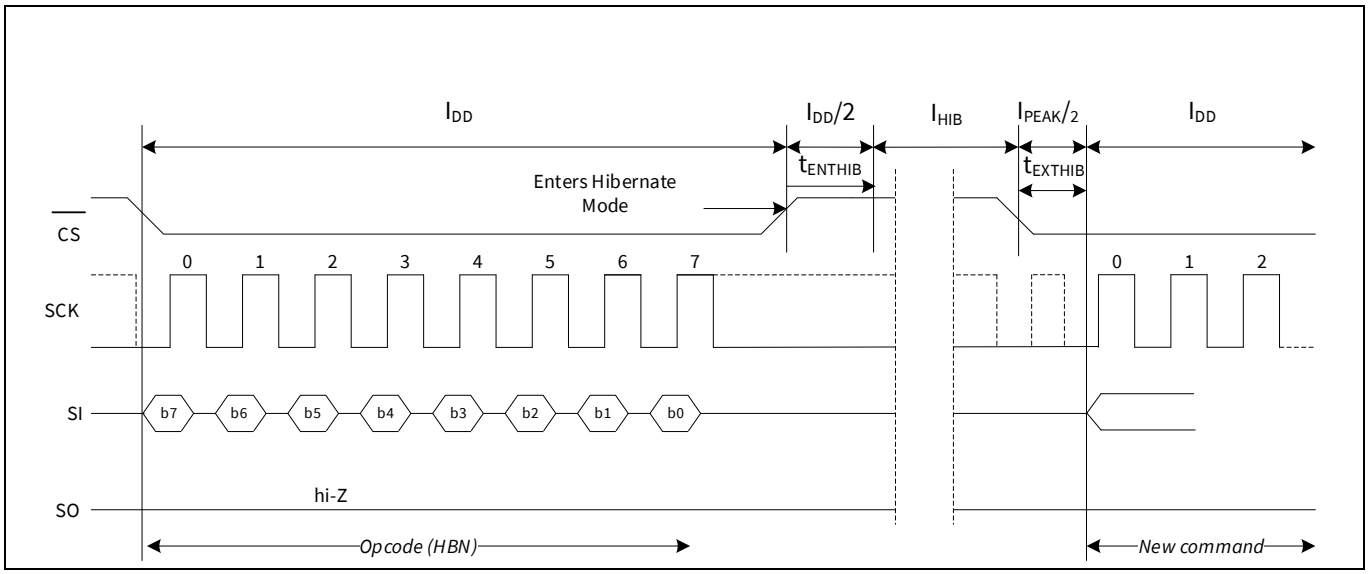

Figure 3 EXCELON™ LP SPI F-RAM hibernate mode

3 Use case analysis

Figure 1 to **Figure 3** illustrate different power modes of EXCELON™ LP SPI F-RAMs and highlight specific current consumed in each power mode. This section analyzes three different use cases based upon system duty cycle to understand total current consumption (active + low-power mode). A point to note is that the energy calculations provided in this section include energy consumption for the EXCELON™ LP SPI F-RAM device alone; to get the combined system-level power, you should include the host controller and other associated circuits also.

Table 2 lists the entry and exit timings for various low-power modes as well as the associated currents which are the basis for energy calculations under various use-case scenarios. The data provided in **Table 2** has considered the specifications of the EXCELON™ LP SPI F-RAM with inrush current control (CY15B104QI) which are primarily designed for battery powered applications. However, the energy calculation method used in this application note will also apply as is for EXCELON™ LP SPI F-RAM devices with non-inrush current control.

Table 1 Low-power mode enter/exit timings

Low-power modes	Enter time	Exit time
Standby mode	Immediate	Immediate
Deep-power-down mode	$\leq t_{ENTDPD}$	$\leq t_{EXTDPD}$
Hibernate mode	$\leq t_{ENTHIB}$	$\leq t_{EXTHIB}$

Table 2 Low-power mode specifications for energy calculation

EXCELON™ LP SPI F-RAM specification (CY15B104QI)	Value	Unit
V_{DD}	3.0	V
V_{DD} supply current - I_{DD} @ 3 MHz	500	µA
Inrush current (I_{PEAK})	1600	µA
Average current during wakeup from hibernate (I_{PEAK} /2)	800	µA
Average current during wakeup from deep-power-down (I_{DD}/2)	250	µA
V_{DD} Standby current (I_{SB})	2.6	µA
Deep-power-down-current (I_{DPD})	0.8	µA
Hibernate mode current (I_{HBN})	0.1	µA
Time to enter deep-power-down (t_{ENTDPD})	3	µs
Time to enter hibernate ($t_{ENTHBIN}$)	3	µs
Time to exit deep-power-down (t_{EXTDPD})	150	µs
Time to exit hibernate (t_{EXTHBN})	5000	µs

Use case analysis

3.1 Energy calculation equation

E=V*I*T

Where:

E = Energy in µJ

V = Supply voltage V_{DD} in volt

I = Current in mA

T = Time in millisecond

Active mode energy = V_{DD}*Active mode Current*Time in active mode

= V_{DD}*I_{DD}*Time in active mode

Standby mode energy = V_{DD}*Standby mode Current*Time in standby mode

= V_{DD}*I_{SB}*Time in standby mode

Deep-power-down mode energy = Energy to enter deep-power-down + Energy while in deep-power-down + Energy to exit deep-power-down

= V_{DD}*I_{DD}/2*t_{ENTDPD} + V_{DD}*I_{DPD}*Time in deep-power-down + V_{DD}*I_{DD}/2*t_{EXTDPD}

Hibernate mode energy = Energy to enter hibernate + Energy while in hibernate + Energy to exit hibernate

= V_{DD}*I_{DD}/2*t_{ENTHIB} + V_{DD}*I_{HBN}*Time in hibernate + V_{DD}*I_{DD}/2*t_{EXTHIB}

3.2 Use case 1: Sampling interval every 10 milliseconds

This use case analysis considers a sampling interval where the system wakes up every 10 milliseconds, enters active mode, stays in active mode for a percentage of the sampling interval and the remaining time is in standby, deep-power-down or hibernate mode, and compares the total energy consumed (active + low-power) across all three low-power modes for varying duty cycles.

Table 3 Use case 1: Energy calculations in different low-power modes

System duty cycle	EXCELON™ LP SPI F-RAM Different operating mode timings (ms)				EXCELON™ LP SPI F-RAM Active + low power mode energy (E = V*I*T) - µJ		
System active (%)	When in active mode	When in standby mode	When in DPD mode	When in hibernate mode	Active+ standby	Active+ DPD	Active+ hibernate
0.1	0.01	9.99	9.837	4.987	0.09	0.15	12.02
0.2	0.02	9.98	9.827	4.977	0.11	0.17	12.04

Use case analysis

System duty cycle	EXCELON™ LP SPI F-RAM Different operating mode timings (ms)				EXCELON™ LP SPI F-RAM Active + low power mode energy (E = V*I*T) - µJ		
System active (%)	When in active mode	When in standby mode	When in DPD mode	When in hibernate mode	Active+ standby	Active+ DPD	Active+ hibernate
0.3	0.03	9.97	9.817	4.967	0.12	0.18	12.05
0.4	0.04	9.96	9.807	4.957	0.14	0.20	12.07
0.5	0.05	9.95	9.797	4.947	0.15	0.21	12.08
0.6	0.06	9.94	9.787	4.937	0.17	0.23	12.10
0.7	0.07	9.93	9.777	4.927	0.18	0.24	12.11
0.8	0.08	9.92	9.767	4.917	0.20	0.26	12.13
0.9	0.09	9.91	9.757	4.907	0.21	0.27	12.14
1	0.1	9.9	9.747	4.897	0.23	0.29	12.16
2	0.2	9.8	9.647	4.797	0.38	0.44	12.31
3	0.3	9.7	9.547	4.697	0.53	0.59	12.46
4	0.4	9.6	9.447	4.597	0.67	0.74	12.61
5	0.5	9.5	9.347	4.497	0.82	0.89	12.76
6	0.6	9.4	9.247	4.397	0.97	1.04	12.91
7	0.7	9.3	9.147	4.297	1.12	1.19	13.06
8	0.8	9.2	9.047	4.197	1.27	1.34	13.21
9	0.9	9.1	8.947	4.097	1.42	1.49	13.36
10	1	9	8.847	3.997	1.57	1.64	13.51
15	1.5	8.5	8.347	3.497	2.32	2.38	14.26
20	2	8	7.847	2.997	3.06	3.13	15.01
25	2.5	7.5	7.347	2.497	3.81	3.88	15.76
30	3	7	6.847	1.997	4.55	4.63	16.51
35	3.5	6.5	6.347	1.497	5.30	5.38	17.26
40	4	6	5.847	0.997	6.05	6.13	18.01
45	4.5	5.5	5.347	0.497	6.79	6.88	18.76
50	5	5	4.847	0	7.54	7.63	19.51
55	5.5	4.5	4.347	0	8.29	8.38	20.26
60	6	4	3.847	0	9.03	9.12	21.01
65	6.5	3.5	3.347	0	9.78	9.87	21.76
70	7	3	2.847	0	10.52	10.62	22.51
75	7.5	2.5	2.347	0	11.27	11.37	23.26
80	8	2	1.847	0	12.02	12.12	24.01
85	8.5	1.5	1.347	0	12.76	12.87	24.76
90	9	1	0.847	0	13.51	13.62	25.51
95	9.5	0.5	0.347	0	14.25	14.37	26.26
99	9.9	0.1	0	0	14.85	14.96	26.86

Use case analysis

Note: *The 0 millisecond for both deep-power-down and hibernate modes indicates that the EXCELON™ LP SPI F-RAM device doesn't have sufficient time to stay in respective low-power mode for those specific duty cycles.*

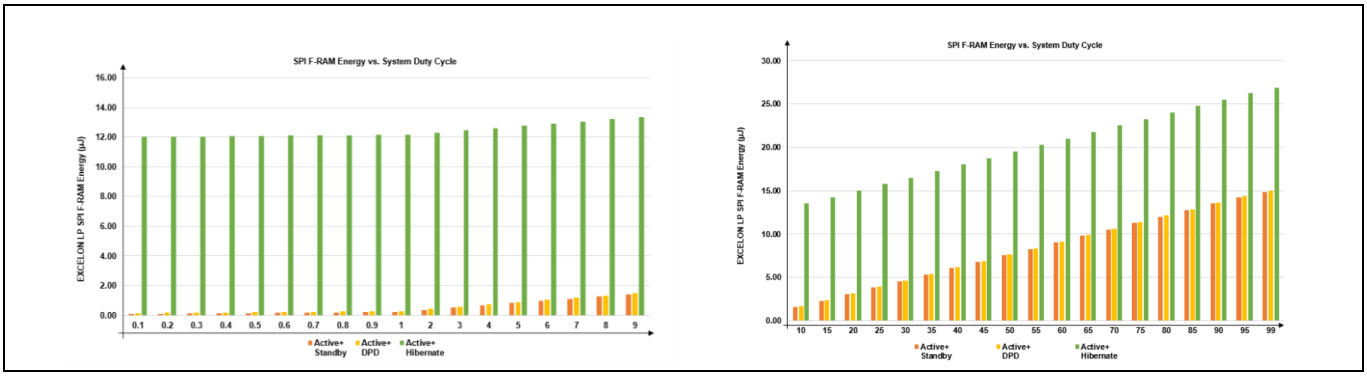

Figure 4 **Use case 1: Energy calculations in different low-power modes**

3.3 Use case 2: Sampling interval every second

This use case analysis considers a sampling interval where the system wakes up every second, enters active mode, stays in active mode for a percentage of the sampling interval and the remaining time is in standby, deep-power-down, or hibernate mode, and compares the total energy consumed (active + low-power) across all three low-power modes for varying duty cycles.

Table 4 **Use case 2: Energy calculations in different low-power modes**

System duty cycle	EXCELON™ LP SPI F-RAM Different operating mode timings (ms)				EXCELON™ LP SPI F-RAM Active + low power mode energy (E = V*I*T) - µJ		
System active (%)	**When in active mode**	**When in standby mode**	**When in DPD mode**	**When in hibernate mode**	**Active+standby**	**Active+DPD**	**Active+hibernate**
0.1	1	999	998.847	993.997	9.29	4.01	13.81
0.2	2	998	997.847	992.997	10.78	5.51	15.31
0.3	3	997	996.847	991.997	12.28	7.01	16.80
0.4	4	996	995.847	990.997	13.77	8.50	18.30
0.5	5	995	994.847	989.997	15.26	10.00	19.80
0.6	6	994	993.847	988.997	16.75	11.50	21.30
0.7	7	993	992.847	987.997	18.25	13.00	22.80
0.8	8	992	991.847	986.997	19.74	14.50	24.30
0.9	9	991	990.847	985.997	21.23	15.99	25.80
1	10	990	989.847	984.997	22.72	17.49	27.30
2	20	980	979.847	974.997	37.64	32.47	42.30
3	30	970	969.847	964.997	52.57	47.44	57.30
4	40	960	959.847	954.997	67.49	62.42	72.29
5	50	950	949.847	944.997	82.41	77.39	87.29
6	60	940	939.847	934.997	97.33	92.37	102.29

Use case analysis

System duty cycle	EXCELON™ LP SPI F-RAM Different operating mode timings (ms)				EXCELON™ LP SPI F-RAM Active + low power mode energy (E = V*I*T) - µJ		
System active (%)	When in active mode	When in standby mode	When in DPD mode	When in hibernate mode	Active+standby	Active+DPD	Active+hibernate
7	70	930	929.847	924.997	112.25	107.35	117.28
8	80	920	919.847	914.997	127.18	122.32	132.28
9	90	910	909.847	904.997	142.10	137.30	147.28
10	100	900	899.847	894.997	157.02	152.27	162.28
15	150	850	849.847	844.997	231.63	227.15	237.26
20	200	800	799.847	794.997	306.24	302.03	312.25
25	250	750	749.847	744.997	380.85	376.91	387.23
30	300	700	699.847	694.997	455.46	451.79	462.22
35	350	650	649.847	644.997	530.07	526.67	537.20
40	400	600	599.847	594.997	604.68	601.55	612.19
45	450	550	549.847	544.997	679.29	676.43	687.17
50	500	500	499.847	494.997	753.90	751.31	762.16
55	550	450	449.847	444.997	828.51	826.19	837.14
60	600	400	399.847	394.997	903.12	901.07	912.13
65	650	350	349.847	344.997	977.73	975.95	987.11
70	700	300	299.847	294.997	1052.34	1050.83	1062.10
75	750	250	249.847	244.997	1126.95	1125.71	1137.08
80	800	200	199.847	194.997	1201.56	1200.59	1212.07
85	850	150	149.847	144.997	1276.17	1275.47	1287.05
90	900	100	99.847	94.997	1350.78	1350.35	1362.04
95	950	50	49.847	44.997	1425.39	1425.23	1437.02
99	990	10	9.847	4.997	1485.08	1485.14	1497.01

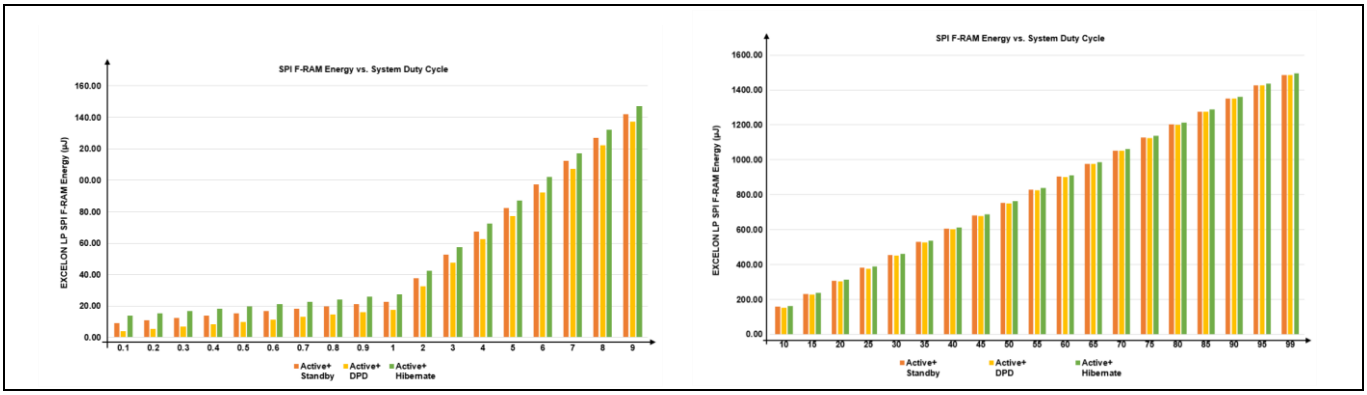

Figure 5 Use case 2: Energy calculations in different low-power modes

3.4 Use case 3: Sampling interval every 100 seconds

This use case analysis considers a sampling interval where the system wakes up every 100 seconds, enters active mode, stays in active mode for a percentage of the sampling interval and the remaining time is in standby, deep-power-down, or hibernate mode, and compares the total energy consumed (active + low-power) across all three low-power modes for varying duty cycles.

Table 5 Use case 3: Energy calculations in different low-power modes

System duty cycle	EXCELON™ LP SPI F-RAM Different operating mode timings (ms)				EXCELON™ LP SPI F-RAM Active + low power mode energy (E = V*I*T) - µJ		
System active (%)	When in active mode	When in standby mode	When in DPD mode	When in hibernate mode	Active+standby	Active+DPD	Active+hibernate
0.1	100	99900	99899.85	99895	929.22	389.87	191.98
0.2	200	99800	99799.85	99795	1078.44	539.63	341.95
0.3	300	99700	99699.85	99695	1227.66	689.39	491.92
0.4	400	99600	99599.85	99595	1376.88	839.15	641.89
0.5	500	99500	99499.85	99495	1526.10	988.91	791.86
0.6	600	99400	99399.85	99395	1675.32	1138.67	941.83
0.7	700	99300	99299.85	99295	1824.54	1288.43	1091.80
0.8	800	99200	99199.85	99195	1973.76	1438.19	1241.77
0.9	900	99100	99099.85	99095	2122.98	1587.95	1391.74
1	1000	99000	98999.85	98995	2272.20	1737.71	1541.71
2	2000	98000	97999.85	97995	3764.40	3235.31	3041.41
3	3000	97000	96999.85	96995	5256.60	4732.91	4541.11
4	4000	96000	95999.85	95995	6748.80	6230.51	6040.81
5	5000	95000	94999.85	94995	8241.00	7728.11	7540.51
6	6000	94000	93999.85	93995	9733.20	9225.71	9040.21
7	7000	93000	92999.85	92995	11225.40	10723.31	10539.91
8	8000	92000	91999.85	91995	12717.60	12220.91	12039.61
9	9000	91000	90999.85	90995	14209.80	13718.51	13539.31
10	10000	90000	89999.85	89995	15702.00	15216.11	15039.01
15	15000	85000	84999.85	84995	23163.00	22704.11	22537.51
20	20000	80000	79999.85	79995	30624.00	30192.11	30036.01
25	25000	75000	74999.85	74995	38085.00	37680.11	37534.51
30	30000	70000	69999.85	69995	45546.00	45168.11	45033.01
35	35000	65000	64999.85	64995	53007.00	52656.11	52531.51
40	40000	60000	59999.85	59995	60468.00	60144.11	60030.01
45	45000	55000	54999.85	54995	67929.00	67632.11	67528.51
50	50000	50000	49999.85	49995	75390.00	75120.11	75027.01
55	55000	45000	44999.85	44995	82851.00	82608.11	82525.51
60	60000	40000	39999.85	39995	90312.00	90096.11	90024.01

Use case analysis

System duty cycle	EXCELON™ LP SPI F-RAM Different operating mode timings (ms)				EXCELON™ LP SPI F-RAM Active + low power mode energy (E = V*I*T) - µJ		
System active (%)	When in active mode	When in standby mode	When in DPD mode	When in hibernate mode	Active+standby	Active+DPD	Active+hibernate
65	65000	35000	34999.85	34995	97773.00	97584.11	97522.51
70	70000	30000	29999.85	29995	105234.00	105072.11	105021.01
75	75000	25000	24999.85	24995	112695.00	112560.11	112519.51
80	80000	20000	19999.85	19995	120156.00	120048.11	120018.01
85	85000	15000	14999.85	14995	127617.00	127536.11	127516.51
90	90000	10000	9999.847	9994.997	135078.00	135024.11	135015.01
95	95000	5000	4999.847	4994.997	142539.00	142512.11	142513.51
99	99000	1000	999.847	994.997	148507.80	148502.51	148512.31

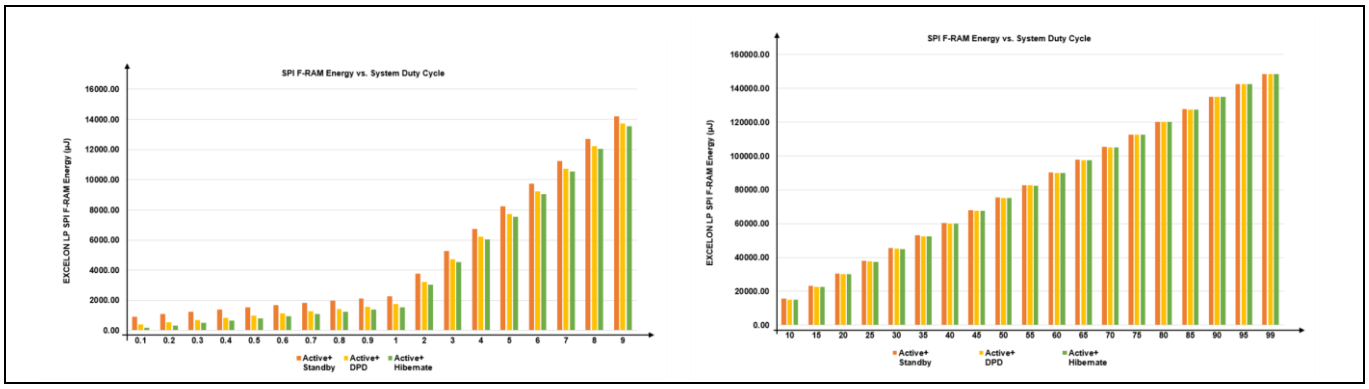

Figure 6 Use case 3: Energy calculations in different low-power modes

3.5 Use case analysis summary

The three low-power mode analyses show that EXCELON™ LP SPI F-RAM energy efficiency primarly varies with EXCELON™ LP SPI F-RAM active to low-power mode transition frequency (or sampling interval) and the duty cycle (percentage of the time EXCELON™ LP SPI F-RAM goes into active mode for every sampling interval). **Table 6** summarizes all the three use cases and recommended EXCELON™ LP SPI F-RAM low-power mode for each use case. Point to note here is that the recommendations are purely based on power efficiency. Other system requirements should overide these recommendations whenever necessary.

Table 6 EXCELON™ LP SPI F-RAM low-power mode use case analysis summary

Sampling interval (Ts)	Duty cycle	Standby	Deep-power-down	Hibernate	Comment
Ts < 25 ms	<10%	✓			
	>10%	✓	✓		Deep-power-down takes t_{EXTDPD} time to wake.
25 ms ≤ Ts <10,000 ms	<10%		✓		
	>10%	✓	✓	✓	Deep-power-down and hibernate take t_{EXTDPD} and t_{EXTHBN} time to wake.

Use case analysis

Sampling interval (Ts)	Duty cycle	Standby	Deep-power-down	Hibernate	Comment
Ts ≥ 10,000 ms	<10%			✓	
	>10%	✓	✓	✓	Deep-power-down and hibernate take t_{EXTDPD} and t_{EXTHBN} time to wake.

Use case 1 – **Table 3** and energy comparison graphs in **Figure 4** show that when the system is accessing EXCELON™ LP SPI F-RAM frequently (i.e., every 25 milliseconds or even faster), keeping the EXCELON™ LP SPI F-RAM in standby mode is more energy efficient than the other two low-power modes. Using hibernate mode should be avoided in this use case. In addition, unlike deep-power-down and hibernate mode, there is no wakeup time penalty when using standby mode.

Use case 2 – **Table 4** and energy comparison graphs in **Figure 5** show that when the system is accessing EXCELON™ LP SPI F-RAM less frequently than in Use case 1 (i.e., every 10 seconds or faster down to 25 milliseconds), keeping the EXCELON™ LP SPI F-RAM in deep-power-down mode is more energy efficient than the other two low-power modes. However, exiting deep-power-down mode takes t_{EXTDPD} time before the device is ready for access, which needs to be considered in the system design.

Use case 3 – **Table 5** and energy comparison graphs in **Figure 6** show that when when the system is accessing EXCELON™ LP SPI F-RAM at a slow interval (i.e., every 10 seconds or slower), putting the EXCELON™ LP SPI F-RAM in hibernate mode is more energy efficient than the other two low-power modes. However, exiting hibernate mode takes t_{EXTHBN} time before device is ready for access, which needs to be considered in the system design.

4 Other considerations for low-power mode current consumption

This section summarizes other system considerations that can influence the low-power measurements in EXCELON™ LP SPI F-RAMs. **Figure 7** shows an example of EXCELON™ LP SPI F-RAM interface with a SPI host controller.

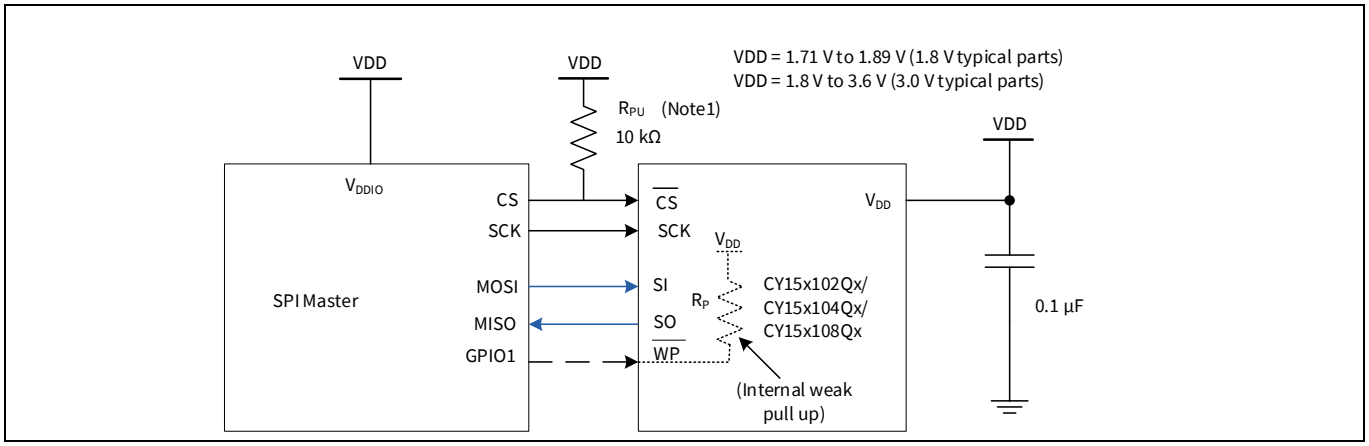

Figure 7 System Interface with EXCELON™ LP SPI F-RAM

The signal and device nomenclature used in **Figure 7** is as follows:

MOSI: Master-out-slave-in; *MISO:* Master-in-slave-out

CY15x102Qx/CY15x104Qx/CY15x108Qx – EXCELON™ LP SPI F-RAMs including Inrush current controlled parts.

CY15V102Qx/CY15V104Qx/CY15V108Qx – 1.8 V typical V_{DD} parts

CY15B102Qx/CY15B104Qx/CY15B108Qx – 3.3 V typical V_{DD} parts

Data lines (Input, Output) ——————

Control line ($\overline{CS}$ and SCK) ——————

(Optional connections) - - - - - - - -

System conditions that can influence the EXCELON™ LP SPI F-RAM current measurements are described below:

1. Operating voltage (V_{DD}) is outside datasheet limits.
2. Input voltage not swinging to appropriate logic levels of EXCELON™ LP SPI F-RAM.
3. The $\overline{WP}$ input pin provides an on-chip internal weak pull-up (R_P) to V_{DD}, as shown in **Figure 7**. Therefore, if this pin is biased to a logic HIGH, the input voltage level must at V_{DD} to avoid any current leakage through R_P. If the $\overline{WP}$ is not controlled, it is recommended to leave the pin to floating or short to V_{DD}.

Revision history

Document version	Date of release	Description of changes
**	2018-11-07	Initial release
*A	2021-09-23	Migrated to Infineon template

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2021-09-23
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Go to www.cypress.com/support

Document reference
002-25301 Rev. *A

IMPORTANT NOTICE
The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.