Design and Layout Guide for SEMPER™ Flash Memory

About this document

Scope and purpose

AN224153 describes system PCB layout recommendations for optimizing signal layout and power supply lines to prevent signal integrity problems when using SEMPER™ Flash with Quad SPI, Octal Interface, and HYPERBUS™ interface devices.

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1 Introduction

This document provides general design recommendations for a PCB that uses SEMPER™ Flash Memory products. These guidelines include recommendations for both signal routing and power delivery to the device.

To achieve the best performance, the PCB design should provide an impedance- and loss-controlled environment, support a low-impedance power delivery system, and control the electromagnetic interference (EMI).

This document serves as an initial reference for PCB designs using SEMPER™ Flash Memory products. It does not eliminate the need to perform signal integrity and power delivery simulations. Use Infineon-provided IBIS models as well as IBIS models from controller vendors for signal timing and crosstalk simulations. You should verify actual characteristics empirically on prototype and validation build units.

If a design cannot meet the recommendations provided herein, perform detailed simulations to determine whether deviations from the recommendations affect the bus performance.

As a flash user, you may already be familiar with the basic operations in NOR flash devices: Read, Program, and Erase. The SEMPER™ Flash Family provides many other features to satisfy the diverse needs of different users. You should first seek to understand the datasheet before reading this document, especially if you are not familiar with SEMPER™ Flash devices in general.

SEMPER™ Flash families of products are built on an advanced 45-nm MIRRORBIT™ process technology. Among the advances are higher bandwidth through higher frequency (400 MB/s–200 MHz), interface data integrity through Interface CRC, and enhanced endurance/retention through EnduraFlex™. Semper Flash is designed for functional safety in automotive systems with development according to the ISO 26262 standard to achieve ASIL-B compliance and ASIL-D readiness.

1.1 SEMPER™ Flash with Quad SPI family

The S25HS-T/S25HL-T SEMPER™ Flash with Quad SPI family devices are 1.8 V/3.0 V NOR Flash memories with Serial Peripheral Interface (SPI) (1-1-1)[1], Quad (1-4-4) and Quad Peripheral Interface (QPI) (4-4-4), and support Double Data Rate (DDR) frequency (102 MB/s, 02 MHz). These interfaces serially transfer transactions reducing the number of interface connection signals. SPI supports Single Data Rate (SDR) whereas Quad and QPI supports both SDR and DDR reads.

1.2 SEMPER™ Flash with Octal Interface family

The S28HS-T/S28HL-T SEMPER™ Flash with Octal Interface family devices are 1.8 V/3.0 V NOR Flash memories with Octal (8-8-8) and SPI (1-1-1) interfaces, and support DDR frequency (400 MB/s, 200 MHz). Both interfaces serially transfer transactions reducing the number of interface connection signals. SPI supports SDR whereas OPI supports both SDR and DDR reads.

1.3 SEMPER™ Flash with HYPERBUS™ Interface family

The S26HS-T/S26HL-T SEMPER™ Flash with HYPERBUS™ Interface family devices are 1.8 V/3.0 V NOR Flash memories with HYPERBUS™ and SPI (1-1-1) interfaces, support DDR frequency (400 MB/s, 200 MHz). Both interfaces serially transfer transactions reducing the number of interface connection signals. SPI supports SDR whereas HYPERBUS™ supports DDR reads.

1 Define transaction interface (Command - Address - Data).

2 Signal descriptions and schematic

2.1 SEMPER™ Flash with Quad SPI

Table 1 summarizes the I/O found on all Infineon Quad SPI devices: not all are present on any given package. See product-specific datasheets listed in Related documents to determine the I/O connections that are available for a device and for additional information regarding their function and operation.

Table 1 Signal descriptions

Signal	Type	Mandatory/ Optional	Description
CS#	Input	Mandatory	Chip Select (CS#) All bus transactions are initiated with a HIGH-to-LOW transition on CS# and terminated with a LOW-to-HIGH transition on CS#. Driving CS# LOW enables the device, placing it in the Active mode. When CS# is driven HIGH, the device enters the Standby mode, unless an internal embedded operation is in progress. All other input pins are ignored, and the output pins are put in High-Z state. On parts where the pin configuration offers a dedicated RESET# pin, it remains active when CS# is HIGH. During power on or hardware reset, the CS# pin must be HIGH when the process is completed (t_{PU}).
CK	Input	Mandatory	Clock (CK). Clock provides timing of the serial interface. Transactions are latched on the rising edge of the clock. In SDR protocol, command, address, and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock. In DDR protocol, command, address, and data inputs are latched on both edges of the clock, and data is output on both edges of the clock.
DQ0 / SI	Input / Output	Mandatory	DQ0 Input/ Output for Dual or Quad SPI protocol Serial Input (SI) for Single SPI protocol
DQ1 / SO	Input / Output	Mandatory	DQ1 Input/ Output for Dual or Quad SPI protocol Serial Output (SO) for Single SPI protocol
DQ2 / WP#	Input / Output (Weak Pull-up)	Mandatory	DQ2 Input/ Output for Quad SPI protocol Write Protect (WP#) for Single and Dual SPI protocol The signal has an internal pull-up resistor and can be left unconnected in the host system if not used for Quad transactions or write protection. If write protection is enabled, the host system is required to drive WP# HIGH or LOW during write register transactions.
DQ3 / RESET#	Input / Output (Weak Pull-up)	Mandatory	DQ3 Input/ Output for Quad SPI protocol The signal has an internal pull-up resistor and can be left unconnected in the host system if not used for Quad SPI transactions or RESET#. RESET# for single or dual SPI protocol. This signal can be configured as RESET# when CS# is HIGH or Quad SPI protocol is disabled.

Signal descriptions and schematic

Signal	Type	Mandatory/ Optional	Description
RESET#	Input (Weak Pull-up)	Optional	Hardware Reset (RESET#) When LOW, the device will self-initialize and return to the array read state. DQ[3:0] are placed into the High-Z state when RESET# is LOW. RESET# includes a weak pull-up, meaning that if RESET# is left unconnected, it will be pulled up to the HIGH state on its own.
V_{CC}	Power Supply	Mandatory	Core power supply
V_{SS}	Power Supply	Mandatory	Core ground
DNU			Do Not Use. Do not route any PCB trace to DNU pins.

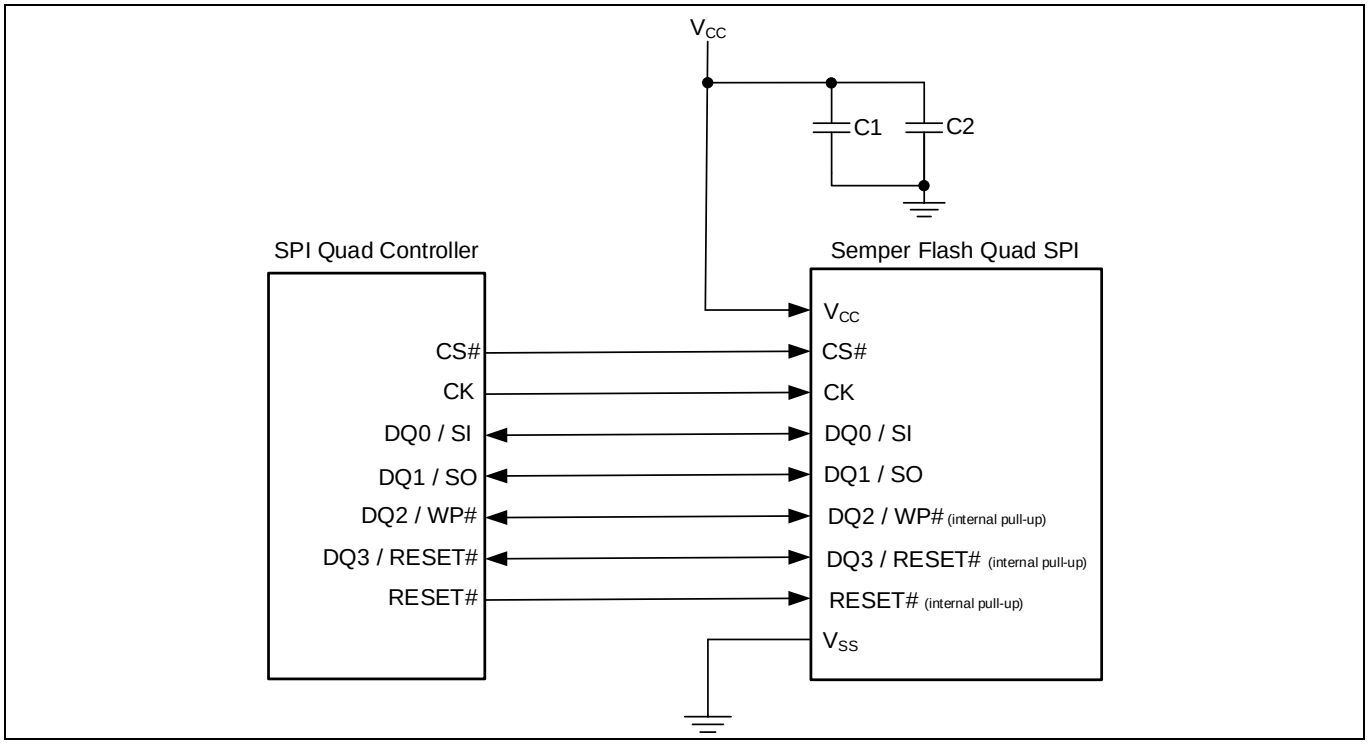


Figure 1 Quad SPI recommended schematic

Table 2 Recommended Capacitor Terminations

Parameter	Symbol	Recommended	Unit	Description
V_{CC} capacitor values[2]	C1	2 x 0.1	µF	Decoupling capacitors should be connected as close as possible to V_{CC} and V_{SS}.
	C2	2 x 1.0		

During signal routing, you should give priority to the signal groups to ensure that they maintain a high-quality signal. Table 3 ranks the signal integrity priority of the five groups, where '1' represents the highest priority and '5' represents the lowest.

[2] See section Power Delivery guidelines on page 20 for details.

Table 3 Signal Integrity Priority of Signal groups

Signal group	Pin names	Signal Integrity priority
Clock	CK	1
Data	DQ0/SI, DQ1/SO, DQ2/WP#, DQ3/RESET#	2
Chip Select	CS#	3
Other Controls	RESET#	4
Power / Ground	V_{CC}, V_{SS}	5

The signal integrity priority denotes the importance of treating that signal group as a high-speed signal. Note that the signal integrity priority does not necessarily dictate the order of signal routing.

2.2 SEMPER™ Flash with Octal Interface

Table 4 summarizes the I/O connections found on Octal devices and may not reflect an individual device. See the product-specific datasheet listed in Related documents to determine the I/O connections for a device and for additional information regarding their function and operation.

Table 4 Signal descriptions

Signal	Type	Mandatory/ Optional	Description
CS#	Input	Mandatory	Chip Select (CS#) All bus transactions are initiated with a HIGH-to-LOW transition on CS# and terminated with a LOW-to-HIGH transition on CS#. Driving CS# LOW enables the device, placing it in the Active mode. When CS# is driven HIGH, the device enters the Standby mode, unless an internal embedded operation is in progress. All other input pins are ignored and the output pins are put in High-Z state. On parts where the pin configuration offers a dedicated RESET# pin, it remains active when CS# is HIGH. During power on or hardware reset, the CS# pin must HIGH when the process is completed (t_{PU}).
CK	Input	Mandatory	Clock (CK) Clock provides timing of the serial interface. Transactions are latched on the rising edge of the clock. In SDR protocol, command, address, and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock. In DDR protocol, command, address, and data inputs are latched on both edges of the clock, and data is output on both edges of the clock.
DS	Output	Mandatory	Read Data Strobe (DS) DS is used for data read operations only, and indicates output data valid for SDR/DDR modes. DS is always enabled in DDR mode but configured by nonvolatile and volatile Configuration Register 5 bit 7 (CFR5N[7] / CFR5V[7]) for SDR mode. When enabled, during a read transaction while CS# is LOW, DS toggles to synchronize data output until CS# goes HIGH. When not enabled, DS is put in High-Z state.

Signal descriptions and schematic

Signal	Type	Mandatory/ Optional	Description
DQ[7:0]	Input / Output	Mandatory	Serial Data (DQ[7:0]) Bidirectional signals that transfer command, address, and data information. Legacy (x1) SPI Interface: DQ[0] is an input (SI) and DQ[1] is an output (SO). Octal (x8) Interface: DQ[7:0] are input and output.
INT#	Output (Open Drain)	Optional	System Interrupt (INT#) When LOW, the device is indicating that an internal event has occurred. This signal is intended to be used as a system-level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output. The recommended pull-up resistor for INT# outputs is 5 kΩ to 10 kΩ.
RESET#	Input (Weak Pull-up)	Optional	Hardware Reset (RESET#) When LOW, the device will self-initialize and return to the array read state. DS and DQ[7:0] are placed into the High-Z state when RESET# is LOW. RESET# includes a weak pullup; it means that if RESET# is left unconnected, it will be pulled up to the HIGH state on its own.
V_{CC}	Power Supply	Mandatory	Core power supply
V_{CCQ}	Power Supply	Mandatory	Input / Output Power
V_{SS}	Power Supply	Mandatory	Core Ground
V_{SSQ}	Power Supply	Mandatory	Input / Output Ground
DNU			Do Not Use. Do not route any PCB trace to DNU pins.

Signal descriptions and schematic

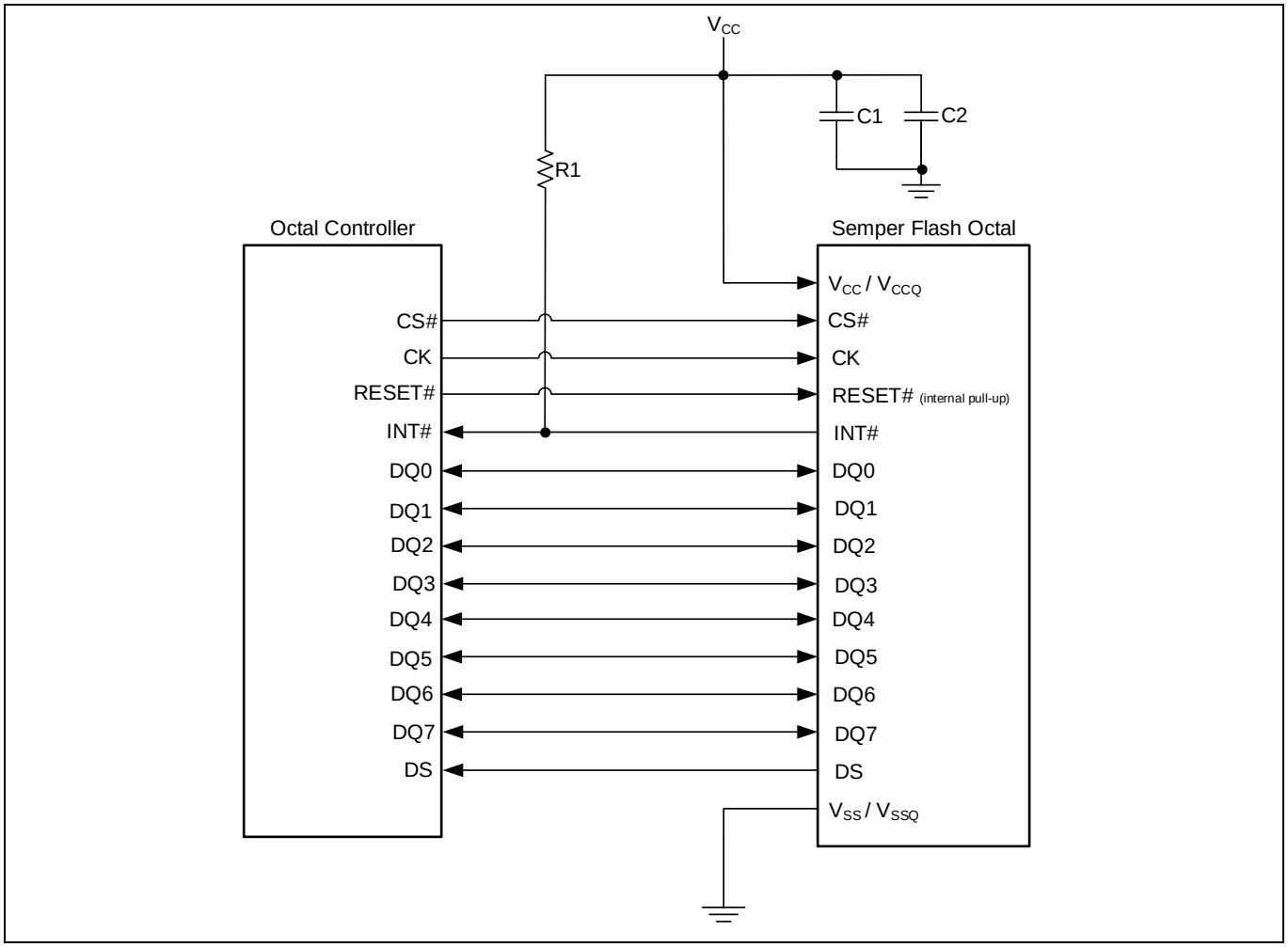


Figure 2 Octal Interface recommended schematic

Table 5 Recommended Resistor and Capacitor terminations

Parameter	Symbol	Recommended	Unit	Description
INT#	R1	5 to 10	KΩ	Prevent Interrupt pin floating and transitory interrupt signals.
V_{CC} and V_{CCQ} capacitor values[3]	C1	3 x 0.1	µF	Decoupling capacitors should be connected as close as possible to V_{CC} (or V_{CCQ}) and V_{SS} (or V_{SSQ}).
	C2	2 x 1.0		

[3] See section Power Delivery guidelines on page 20 for details.

Signal descriptions and schematic

During signal routing, you should give priority to the signal groups to ensure they maintain a high-quality signal. Table 6 ranks the signal integrity priority of the five groups, where '1' represents the highest priority and '5' represents the lowest.

Table 6 Signal Integrity priority of Signal groups

Signal group	Pin names	Signal Integrity priority
Clock	CK	1
Data	DQ[7:0]	2
Read/Write Control	CS#, DS	3
Other Controls	INT#, RESET#	4
Power / Ground	V_{CC}, V_{CCQ}, V_{SS}, V_{SSQ}	5

The signal integrity priority denotes the importance of treating that signal group as a high-speed signal. Note that the signal integrity priority does not necessarily dictate the order of signal routing.

2.3 Semper Flash with HYPERBUS™ Interface

Table 7 summarizes the I/O connections found on HYPERBUS™ Flash devices and may not reflect an individual device. See the product-specific datasheet listed in Related documents to determine the I/O connections for a device and for additional information regarding their function and operation.

Table 7 Signal descriptions

Signal	Type	Mandatory/ Optional	Description
CS#	Input	Mandatory	Chip Select (CS#) All bus transactions are initiated with a HIGH to LOW transition on CS# and terminated with a LOW to HIGH transition on CS#. Driving CS# LOW enables the device, placing it in the Active mode. When CS# is driven HIGH, the device enters the Standby mode, unless an internal embedded operation is in progress. All other input pins are ignored, and the output pins are put in High-Z state. During power on or hardware reset, the CS# pin must be HIGH when the process is completed (t_{PU}).
CK, CK#	Input	Mandatory	Clock (CK, CK#) Clock provides timing of the serial interface. Single-ended and differential clock modes are offered. Transactions are latched either on the rising edge of the CK signal (single-ended) or on the crossing of the CK and CK# signals (differential). In the legacy (x1) SPI interface, command, address, and data inputs are latched on the rising edge of the clock, and data is output on the falling edge of the clock. In HYPERBUS™ (x8) interface, for single-ended clock, command, address, and data input are latched with respect to the rising and falling edges of CK. In differential clock mode, command, address, and data inputs are latched with respect to the crossing of CK and CK#.

Signal descriptions and schematic

Signal	Type	Mandatory/ Optional	Description
			Differential Clock CK and CK# are used. Single-ended CK is used (CK# is not used and can be left floating).
DS	Output	Mandatory	Read Data Strobe (DS) DS is used for data read operations only, and indicates output data valid for the HYPERBUS™ interface. During a read transaction while CS# is LOW, DS toggles to synchronize data output until CS# goes HIGH. Output data during read transactions are edge-aligned with DS.
DQ[7:0]	Input / Output	Mandatory	Serial Data (DQ[7:0]) Bidirectional signals that transfer command, address, and data information. Legacy (x1) SPI Interface DQ[0] is an input (SI) and DQ[1] is an output (SO). HYPERBUS™ (x8) Interface DQ[7:0] are input and output.
RESET#	Input (Weak Pull-up)	Optional	Hardware Reset (RESET#) When LOW, the device will self-initialize and return to the array read state. DS and DQ[7:0] are placed into the High-Z state when RESET# is LOW. RESET# includes a weak pullup; this means that if RESET# is left unconnected, it will be pulled up to the HIGH state on its own.
INT#	Output (Open Drain)	Optional	System Interrupt (INT#) When LOW, the device indicates that an internal event has occurred. This signal is intended to be used as a system-level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output.
RSTO#	Output (Open Drain)	Optional	Reset Output (RSTO#) RSTO# is an open-drain output used to indicate when a POR is occurring within the device and can be used as a system-level reset signal. Upon completion of the internal POR, the RSTO# signal will transition from LOW to High-Z after a user-defined timeout period has elapsed. Upon transition to the High-Z state, the external pull-up resistance will pull RSTO# HIGH and the device immediately is placed into the Standby state.
V_{CC}	Power Supply	Mandatory	Core Power
V_{CCQ}	Power Supply	Mandatory	Input / Output Power
V_{SS}	Power Supply	Mandatory	Core Ground
V_{SSQ}	Power Supply	Mandatory	Input / Output Ground
DNU			Do Not Use. Do not route any PCB trace to DNU pins.

Signal descriptions and schematic

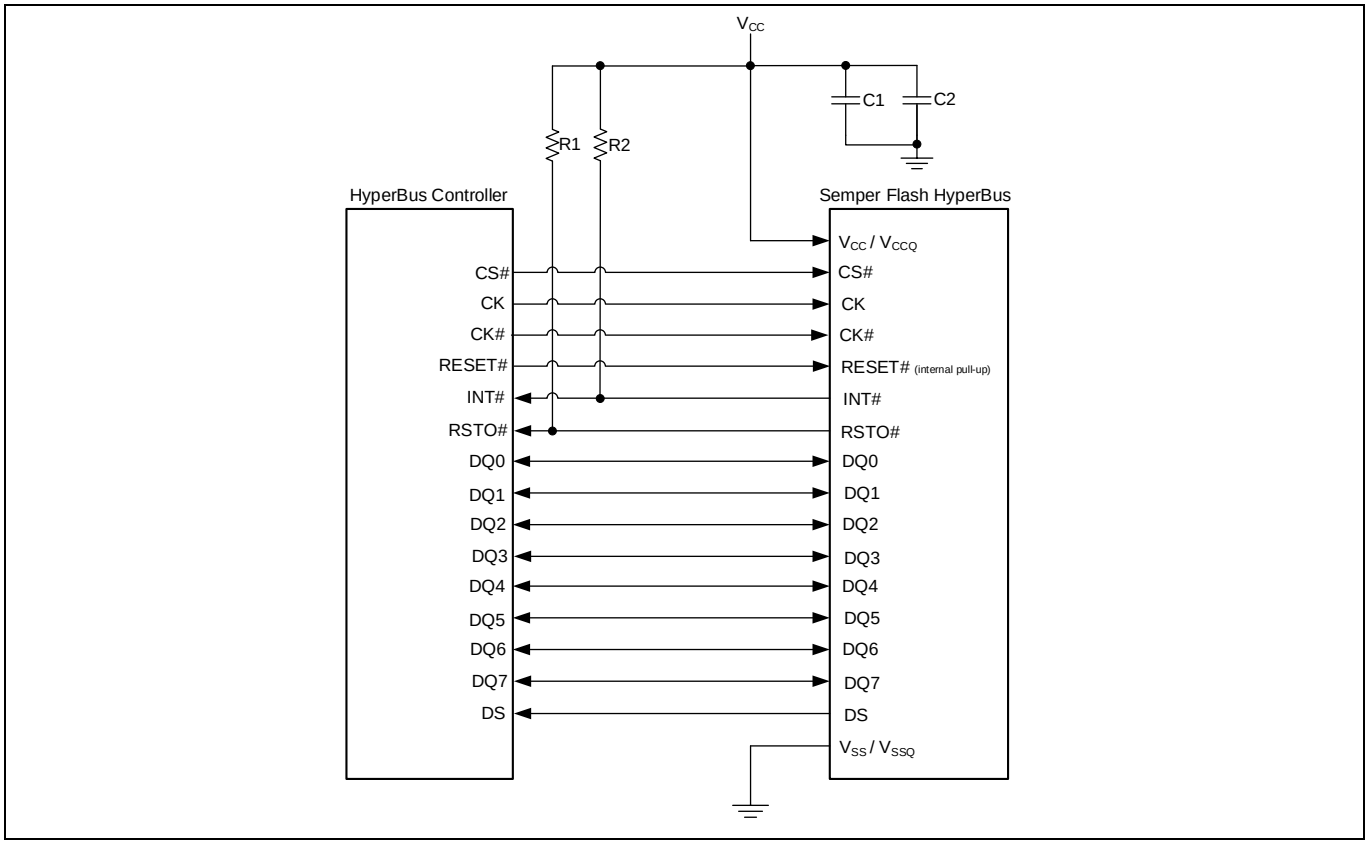


Figure 3 HYPERBUS™ Interface recommended schematic

Table 8 Recommended Resistor and Capacitor terminations

Parameter	Symbol	Recommended	Unit	Description
RSTO#	R1	5 to 10	kΩ	Upon transition to the tristate, the external pull-up resistance will pull RSTO# HIGH and the device immediately is placed into the Standby mode.
INT#	R2	5 to 10	kΩ	Prevent Interrupt pin floating and transitory interrupt signals.
V_{CC} and V_{CCQ} capacitor values[4]	C1	3 x 0.1	µF	Decoupling capacitors should be connected as close as possible to V_{CC} (or V_{CCQ}) and V_{SS} (or V_{SSQ}).
	C2	2 x 1.0		

[4] See section Power Delivery guidelines on page 20 for details.

Signal descriptions and schematic

During signal routing, you should give priority to the signal groups to ensure that they maintain a high-quality signal. Table 6 ranks the signal integrity priority of the five groups, where '1' represents the highest priority and '5' represents the lowest.

Table 9 Signal Integrity priority of Signal groups

Signal group	Pin names	Signal Integrity priority
Clock	CK, CK#	1
Data	DQ[7:0]	2
Read/Write Control	CS#, DS	3
Other Controls	INT#, RESET#, RSTO#	4
Power / Ground	V_{CC}, V_{CCQ}, V_{SS}, V_{SSQ}	5

The signal integrity priority denotes the importance of treating that signal group as a high-speed signal. Note that the signal integrity priority does not necessarily dictate the order of signal routing.

3 Signal Integrity and Impedance Control

Infineon recommends the following actions to improve signal integrity and impedance control.

- Break out all signals on the top PCB layer, if the second layer is a ground plane. This will allow better impedance control and smaller impedance mismatch between breakout traces and traces outside the breakout area.
- Connect V_{CC} and V_{CCQ} to the nearest power plane through vias that are located as close to the target power ball/pin as possible. Traces from the land pad to the vias should be as thick as possible.
- Connect V_{SS} to the nearest ground plane through vias that are located as close to the target ground ball/pin as possible. Traces from the land pad to the vias should be as thick as possible.
- Use a smaller trace width (between 4 mil and 6 mil) and space the adjacent traces approximately three trace widths apart to achieve a 50-ohm impedance. The impedance of data traces depends on the PCB stack-up and the trace width. Use either Microstrip or Stripline interconnects so long as the continuous trace impedance is 50 ohms (±10 percent) throughout the routing path.
- Use buried vias and as few vias as possible to reduce impedance discontinuities due to additional capacitive loading arising from through-hole vias. Any via attached to a trace will alter the signal delay of that trace.
- Route all signal groups on the same signal layer and in the same signal configuration, either all microstrip or all stripline.

4 Signal Routing guidelines

The following guidelines define the recommended trace width and trace spacing, total length limitation, and length matching requirements to achieve optimal signal integrity and timing margins. These recommendations assume point-to-point routing between the host controller and the SEMPER™ Flash memory for simplicity. If this is not the case, you should first select the topology type to follow star, T, or daisy chain. Infineon recommends star or T topology with appropriate termination resistors determined from IBIS simulations. Consider performing signal integrity simulations using Infineon-provided IBIS models to determine guidelines tailored to your specific application (including lower frequency for a particular interface).

- Determine the exact values of signal trace width and trace spacing based on the trace impedance requirement.
- Make the V_{SS} plane serve as a primary reference or return path for all signals. The power layer should only serve as a secondary signals reference option where a solid, continuous ground reference is present.
- Avoid gaps or voids in reference planes to minimize or eliminate return current discontinuity.
- Avoid routing traces at the edge of the reference plane.
- When routing data signals, route the longest signals first. This allows adjustment for signals with shorter lengths.
- Isolate the ground return path of analog signals from digital noise whenever possible.
- Keep all recommended signal routing lengths equal to the distance from package pin (source) to package pin (destination) by considering package length compensation.
- Use signal integrity tools to estimate actual trace velocities and path delays to validate the electrical properties depending on the dielectric material. Infineon determines electrical properties of signal routing by assuming that the dielectric material is FR4. With this assumption, 1 inch equals approximately166 ps.

4.1 Maximum Total Length

- The total load capacitance, which directly affects signal integrity, defines the absolute maximum length of signals with respect to their reference plane.
  - The total load capacitance should remain below the Load Capacitance (C_L) value listed in the datasheet.
  - Total load capacitance includes the following:
    - Total trace length capacitance (~3.3 pF/inch with FR4 assumption)
    - Maximum pin capacitance associated with any parasitic capacitance of connected devices such as connectors and series resistors
    - Maximum pin capacitance of the controller package.
- The Read/Write operation timing requirements bound the total length of clock, control, and data signal routing lines, as stated in the product datasheet. Perform a channel timing simulation to ensure that the system meets these critical timing requirements.
- The recommended practice is to begin with AC timing equations for key timing parameters provided on the Semper Flash and controller datasheets for the flash interface.

4.2 Length matching

- Length matching refers to trace lengths from the memory package pin to the signal pin of the controller. Length matching must include the effective electrical length of any vias.
- Table 10 provides signal skew recommendations for various signal groups. It is important to note the signal polarities (rising-edge and falling-edge triggers) as well as the lead and lag timing to determine whether a specific control signal should always lead or lag compared to another signal or data bus.

Table 10 Length Match recommendations for Signal groups

Signal group	Length Match recommendation for 200 MHz
CK to CK#	±10 mils
DS to DQ[0:7]	±15 mils
DQx [0:7] to DQy [0:7]	±30 mils
CK/CK# to DQ[0:7]	±200 mils
CK/CK# to CS#	±1500 mils
CK/CK# to DS	±1500 mils
RESET# to RSTO# to CS#	±2000 mils

- Avoid routing these signals adjacent to higher-frequency signals to minimize noise from crosstalk.

4.3 Signal spacing

- The center-to-center trace spacing should be greater than three times ‘H’ within a signal group is, where H is the dielectric height between the signal and ground reference layer.
- The center-to-center trace spacing between signal groups should be greater than three times the trace width. In addition, the center-to-center trace spacing between flash signals and other interface signals should be greater than three times the trace width as well. Figure 4 provides a visualization of the recommended signal trace spacing.

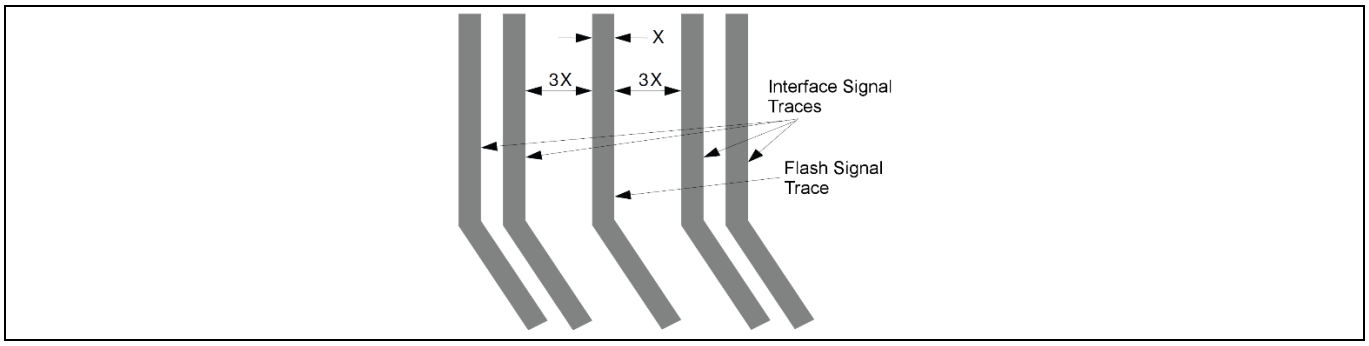


Figure 4 Recommended Signal Trace spacing on the PCB

4.4 Termination

Review the drive strength/impedance of the controller I/O as well as transmission line routing to determine whether series termination is required on these lines. Drive strength for all three (fab process corner, voltage, and temperature [PVT]: typical, minimum, and maximum corners) can be determined by reviewing the IBIS IV/VT curves.

5 Package Connection diagrams

5.1 SEMPER™ Flash Quad SPI

Quad SPI devices are provided in 16-lead SOIC, 8-pin plastic small outline, 8-connector, or 24-ball BGA 5 x 5 ball footprint packages with 6 mm x 8 mm and 8 mm x 8 mm body. The package height is device-dependent.

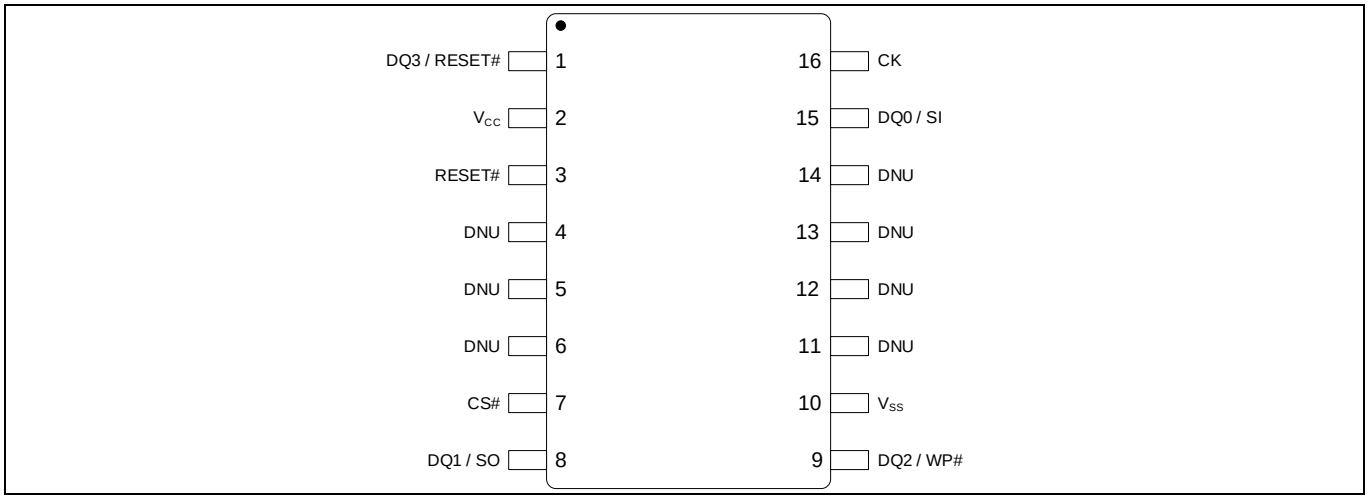


Figure 5 16-lead SOIC package, Top view

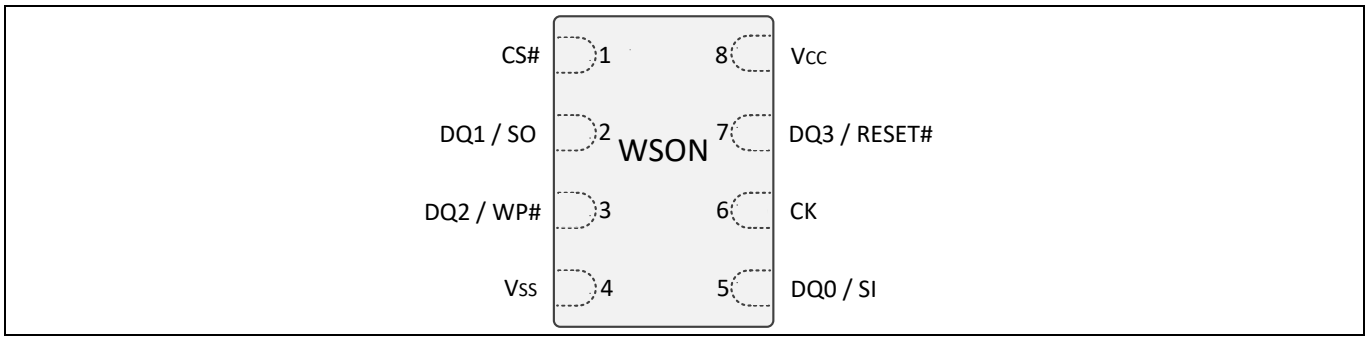


Figure 6 8-connector package (WSON 6 x 8), Top view

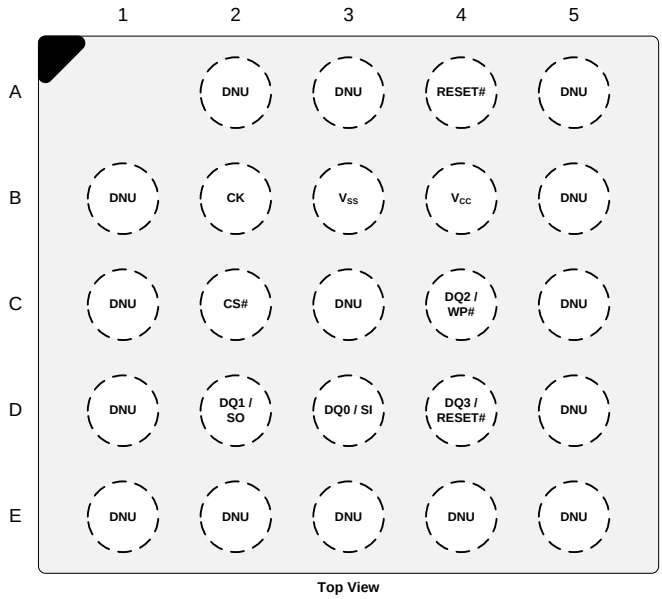


Figure 7 24-ball BGA, 5 x 5 ball footprint, Top view

5.2 SEMPER™ Flash with Octal Interface

Octal devices are provided in Fortified Ball Grid Array (FBGA), 24-ball, 5 x 5 ball array footprint, with 6 mm x 8 mm and 8 mm x 8 mm body. The package height is device-dependent.

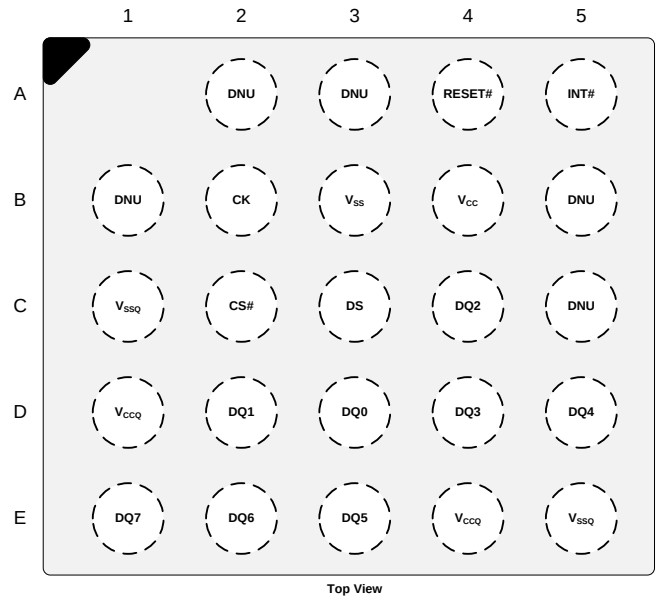


Figure 8 24-ball FBGA, 5 x 5 ball footprint, Top view

5.3 SEMPER™ Flash HYPERBUS™ Interface

HYPERBUS™ devices are provided in FBGA, 24-ball, 5 x 5 ball array footprint, with 6 mm x 8 mm and 8 mm x 8 mm body. The package height is device-dependent.

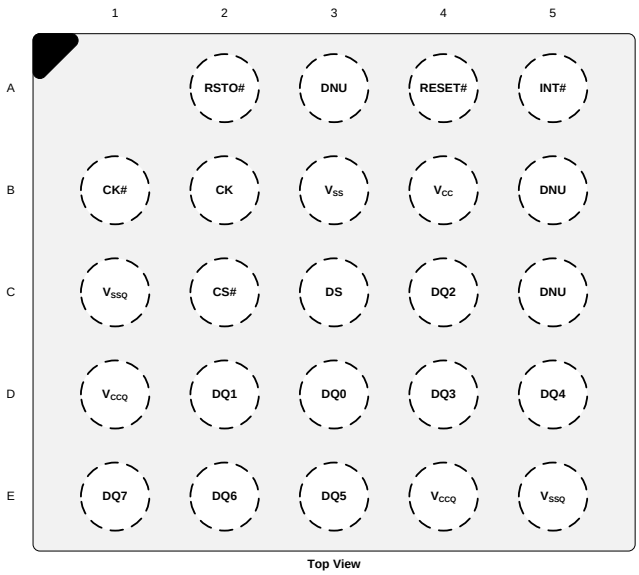
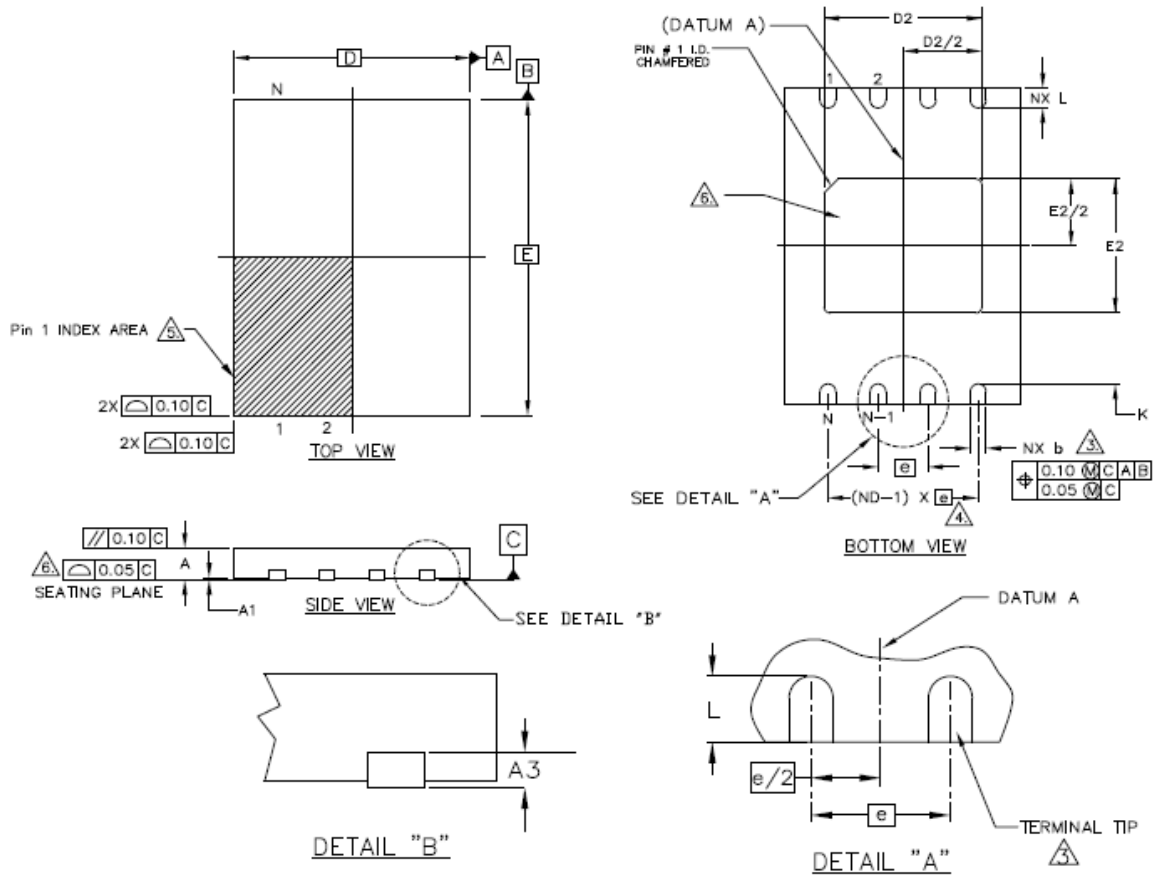


Figure 9 24-ball FBGA, 5 x 5 ball footprint, Top view

5.4 Package drawings

Applicable package drawings are provided in each SEMPER™ Flash datasheet. These drawings are included herein. See the product datasheet for the latest package outline information.



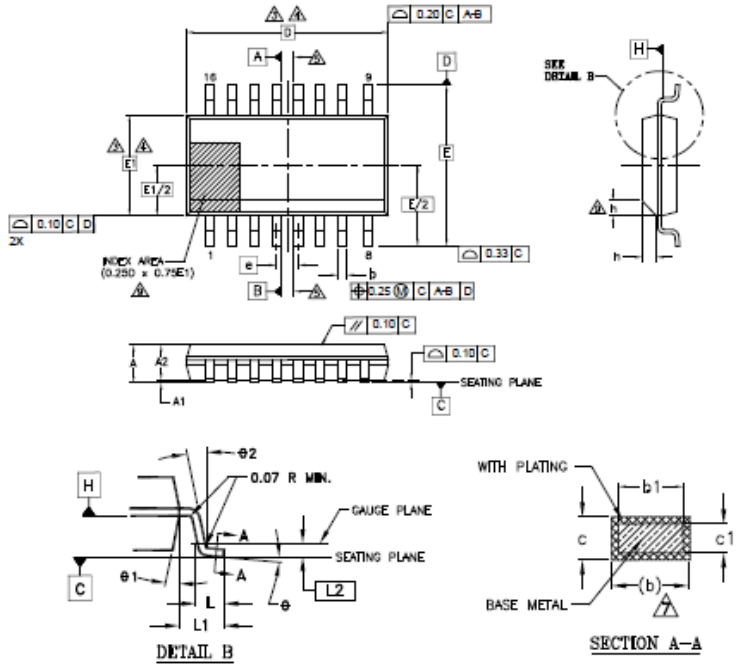
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		1.27 BSC.	
N		8	
ND		4	
L	0.45	0.50	0.55
b	0.35	0.40	0.45
D2	3.90	4.00	4.10
E2	3.30	3.40	3.50
D		6.00 BSC	
E		8.00 BSC	
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3		0.20 REF	
K	0.20	-	-

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A

Figure 10 WSON 8-contact 6 x 8 mm leadless (WNH008)

Package Connection diagrams



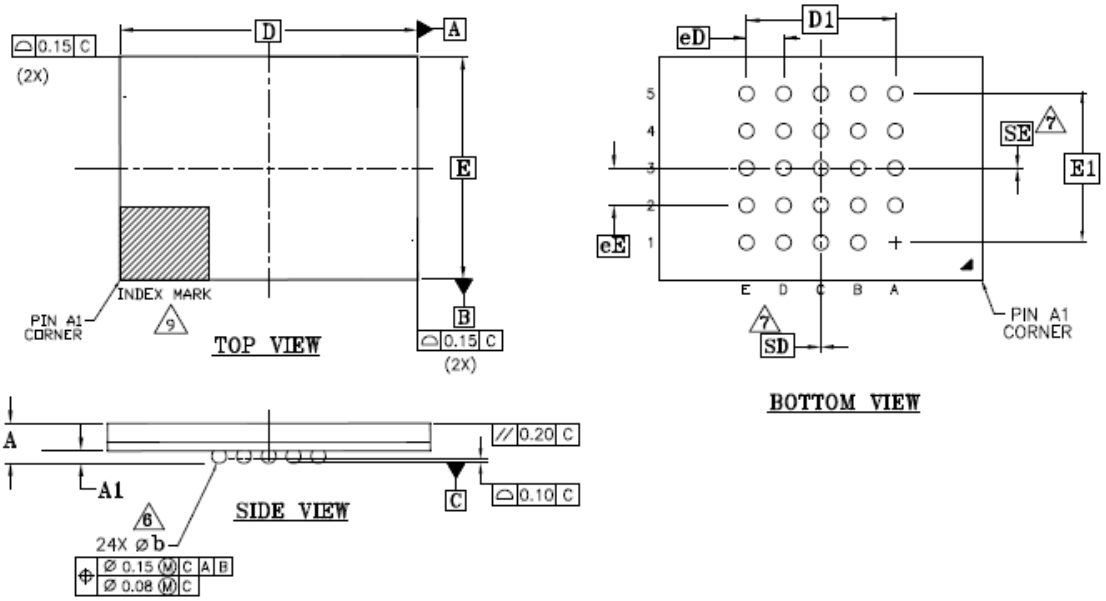
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.35	-	2.65
A1	0.10	-	0.30
A2	2.05	-	2.55
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.20	-	0.33
c1	0.20	-	0.30
D	10.30 BSC		
E	10.30 BSC		
E1	7.50 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.40 REF		
L2	0.25 BSC		
N	16		
h	0.25	-	0.75
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

Figure 11 SOIC 16-lead, 300-mil body width (SO3016)

Package Connection diagrams



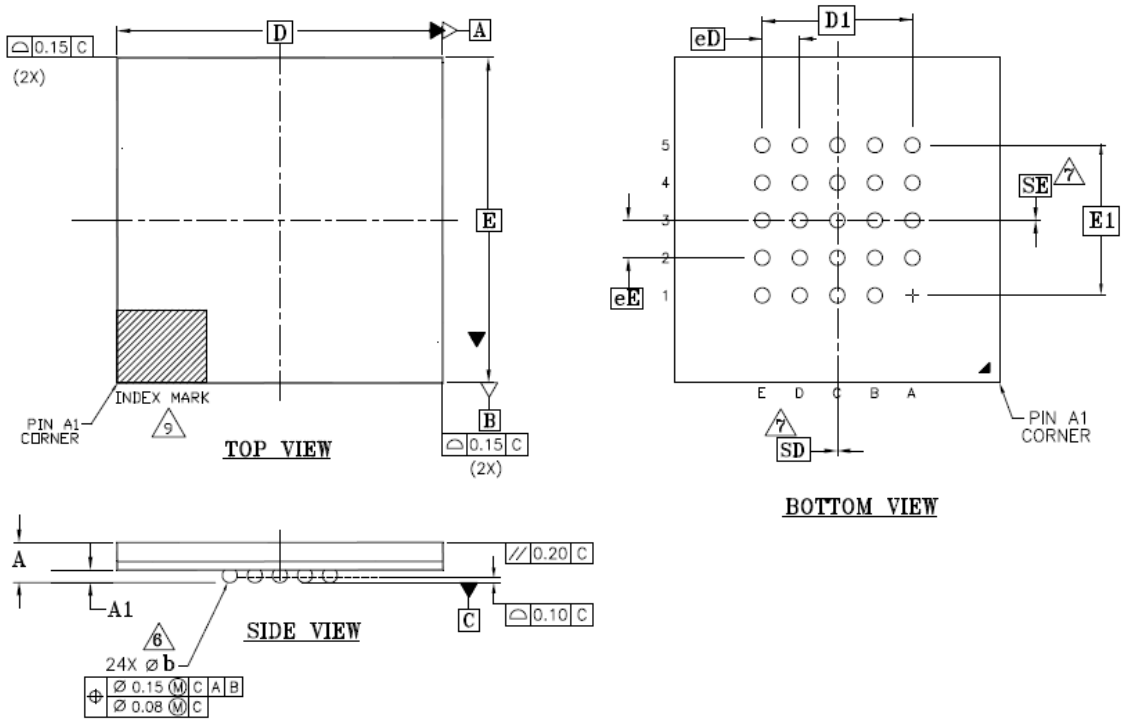
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.20	-	-
D		8.00 BSC	
E		6.00 BSC	
D1		4.00 BSC	
E1		4.00 BSC	
MD		5	
ME		5	
N		24	
Ø b	0.35	0.40	0.45
eE		1.00 BSC	
eD		1.00 BSC	
SD		0.00 BSC	
SE		0.00 BSC	

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. .
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. JEDEC SPECIFICATION NO. REF: N/A

Figure 12 Fortified ball grid array 24-ball 6 x 8 x 1.0 mm (VAA024)

Package Connection diagrams



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.20	-	-
D		8.00 BSC	
E		8.00 BSC	
D1		4.00 BSC	
E1		4.00 BSC	
MD		5	
ME		5	
N		24	
∅ b	0.35	0.40	0.45
eE		1.00 BSC	
eD		1.00 BSC	
SD		0.00 BSC	
SE		0.00 BSC	

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. .
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. JEDEC SPECIFICATION NO. REF: N/A

Figure 13 Ball grid array 24-ball 8 x 8 mm (VAC024)

5.5 Land pattern recommendations

Applicable PCB land pattern recommendations for SO3016, WNH008, VAA024 and 8 mm x 8 mm BGA packages are provided here in Figure 14 to Figure 17.

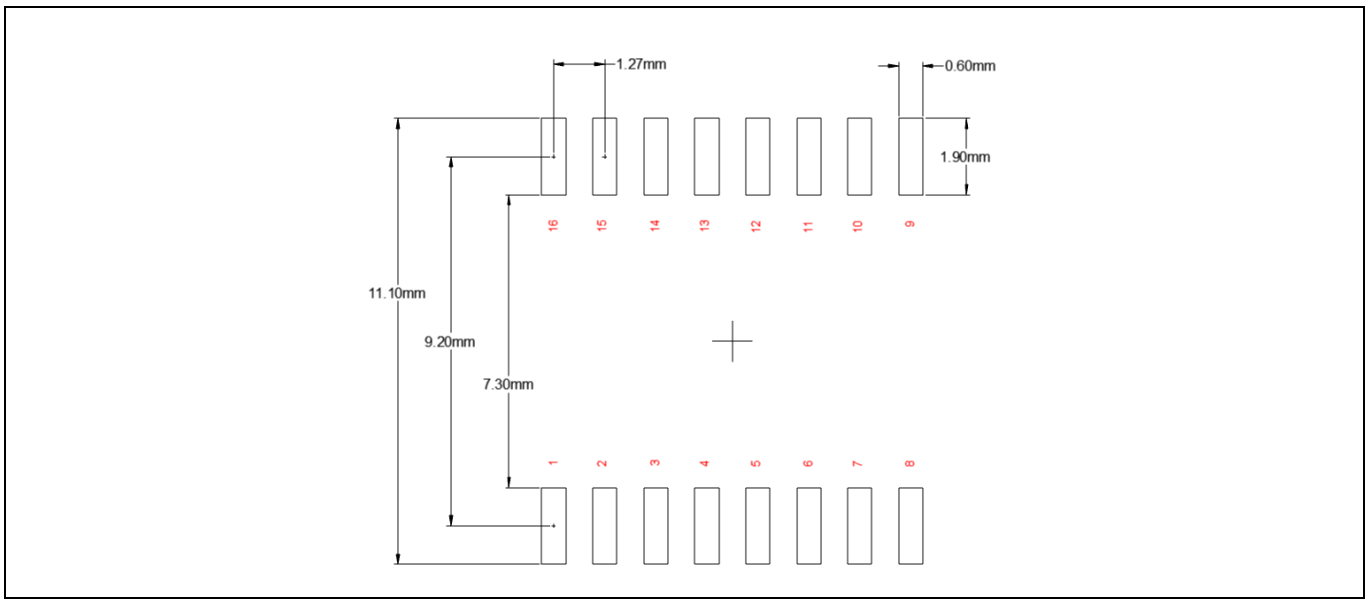


Figure 14 SO3016 proposed land pattern

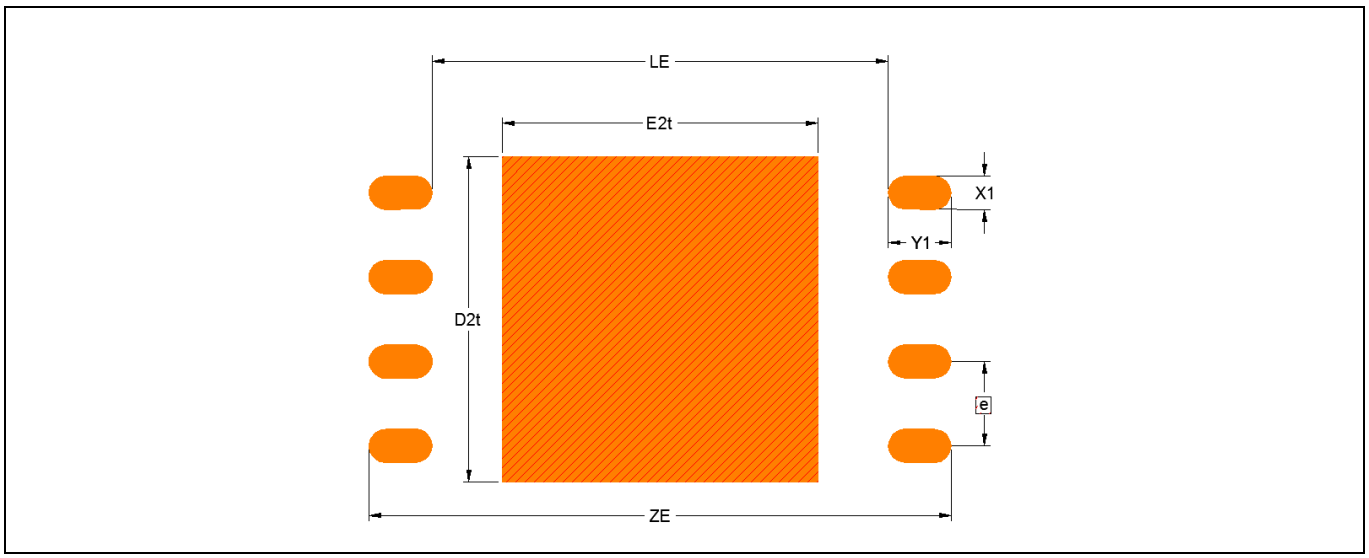


Figure 15 WNH008 proposed land pattern

Table 11 Details

Package	Package code	e (Lead Pitch)	LE (min)	ZE (max)	D2t (max)	E2t (max)	Y1	X1
WSON 8L	WNH008	1.27	6.85	8.75	4.10	3.50	0.95	0.45

Package Connection diagrams

The WSON 8L land patterns are shown above. It is recommended that the center slug should be solder mask define (SMD) to avoid bridging. The mask opening should be 0.05 mm–0.1 mm smaller than the center pad on all four sides. At the pin, it should be non-solder-mask defined (NSMD) with the mask opening 3 mil larger than the copper pad on all sides. At the center slug, the stencil should also have small multiple openings with solder paste coverage about 40%–70% of the exposed pad area to prevent bridging between the center slug and pins.

Applicable PCB land pattern recommendation for BGA packages is provided in Figure 16.

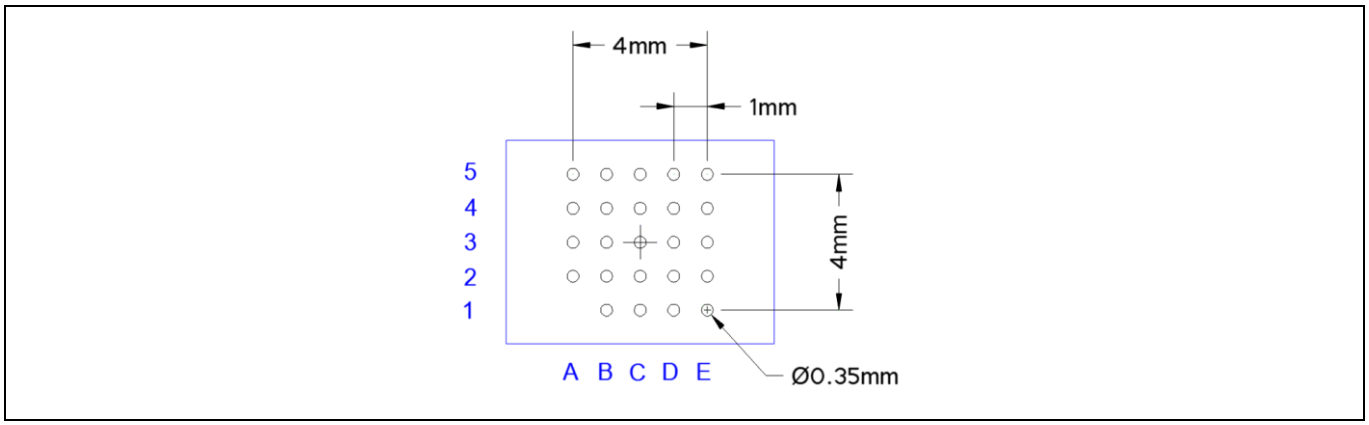


Figure 16 BGA proposed land pattern

PCB solder-ball land pads can be either non-solder-mask defined (NSMD) or solder-mask-defined (SMD). For NSMD configurations, there is a small gap between the solder pad and the solder mask. Solder will flow into the gap between the pad and the solder mask (reference Figure 17). For SMD configurations, the solder mask covers the outer edge of the solder pad. Solder is prevented from flowing over the edges of the pad by the solder mask.

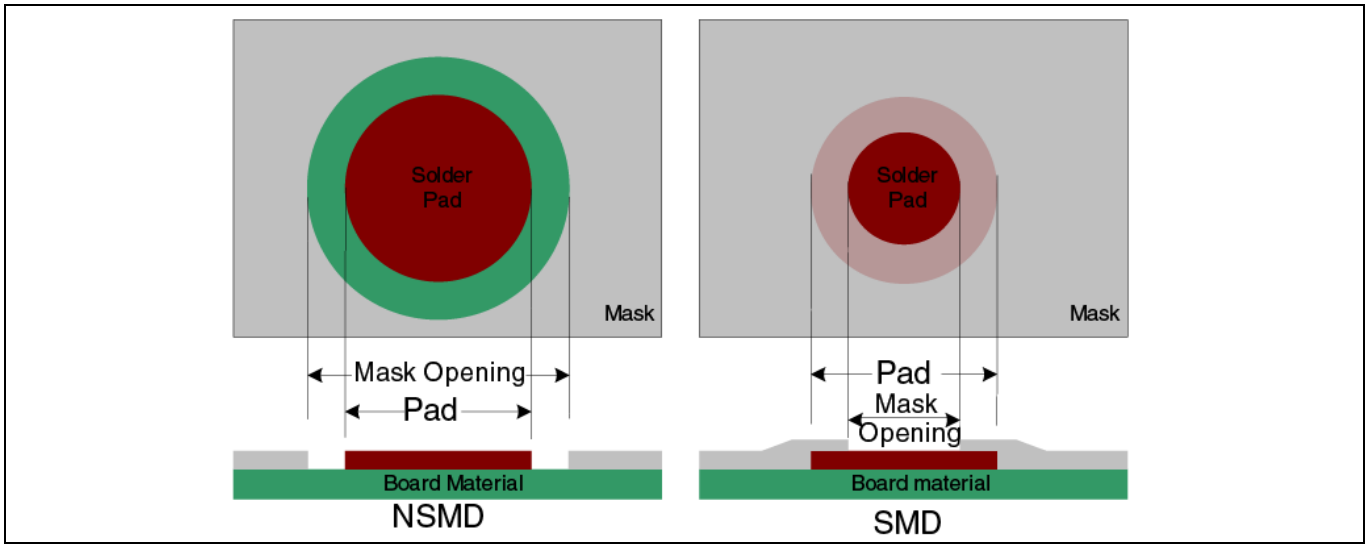


Figure 17 SMD vs. NSMD Landing Pad definition

Package Connection diagrams

NSMD is generally the recommended land pad configuration because it enables a stronger bond between the solder pad and the solder ball with less stress concentration.

For SMD configurations, it is a good practice to make the solder mask opening the same size as the diameter of the solder ball. On NSMD configurations, the solder pad should be between 80% and 100% of the solder ball diameter and the solder mask opening should be 0.15 mm larger than the solder pad to provide ample space for excess solder. Table 12 provides dimensional recommendations for SMD and NSMD configurations suitable for use with the BGA packages.

Table 12 NSMD and SMD Dimensional recommendations for BGA packages

Configuration	Opening	Recommended Dimension
SMD	Solder Pad	0.55 mm
	Solder Mask	0.45 mm
NSMD	Solder Pad	0.35 mm
	Solder Mask	0.60 mm

6 Power Delivery guidelines

The following power delivery guidelines will help ensure that there are no power issues within the system.

- Connect each V_{SS} (and V_{SSQ}) pin/ball to a solid ground plane with its own unique via to improve IR drop.
- Connect V_{CC} (and V_{CCQ}) pins/balls to a supply plane with its own unique via to improve IR drop.
- Gaps between power planes should be at least 20 mil where possible. A gap of at least 80 mil should exist between power islands on the same layer if possible. The air gap between power islands must be greater than 40 mil, preferably as much as 100 mil.
- Power islands, such as V_{CC} island, should be at least 250-mil wide at the narrowest point to avoid bottlenecks.
- Maintain a minimum trace width of 20 mil for all supply traces, except at the package breakout area where vias tie the supply to the nearest supply plane. Route the supply and ground traces (or planes) close to each other to avoid large inductive loops.
- Keep the supply trace lengths less than or equal to 400-mil and keeping the trace widths greater than or equal to 20 mil.
- Use trace widths greater than 20 mil to maintain low impedance from the voltage regulator to the flash voltage supply pins/balls as well as from the voltage regulator to the controller flash interface supply pins/balls.
- If the voltage regulator is not on the same PCB as the flash package when using a module configuration, maintain the lowest possible impedance on traces to V_{CC} and V_{SS}. Wider traces can help to ensure a lower impedance.
- If there is a connector between the host controller and Semper Flash device, use a G: S/P: G type connector configuration where ‘S’ refers to signal, ‘G’ refers to V_{SS}, and ‘P’ refers to V_{CC}.
- It is best to add V_{CC} and V_{SS} test points as close as possible to each flash package and next to the voltage regulator. These test points allow the measurement of V_{CC}-V_{SS} and V_{CCQ}-V_{SSQ} waveforms at both VRM and the package.

6.1 Decoupling Capacitor recommendations

- Place the PCB decoupling capacitors as close to the package as possible.
- Select decoupling capacitors that have low equivalent series inductance (ESL) and equivalent series resistance (ESR).
- V_{CC} and V_{SS} trace routing from the capacitor should be as wide as possible to avoid inductive and resistive effects.
- A minimum two 1-µF 0402 ceramic capacitors should be placed between V_{CC} and V_{SS} near each side of the package.
- In addition to decoupling capacitors, two 0.1-µF 0402 ceramic capacitors should be placed as close to the package as possible between V_{CC} and V_{SS}.
- Recommends using X7R or X5R capacitors with a rated voltage greater than or equal to at least two times V_{CC} max.
- The decoupling capacitor trace length should remain short and should have a unique via, not shared with another decoupling capacitor. Figure 18 presents good and poor examples of decoupling capacitor routing techniques.

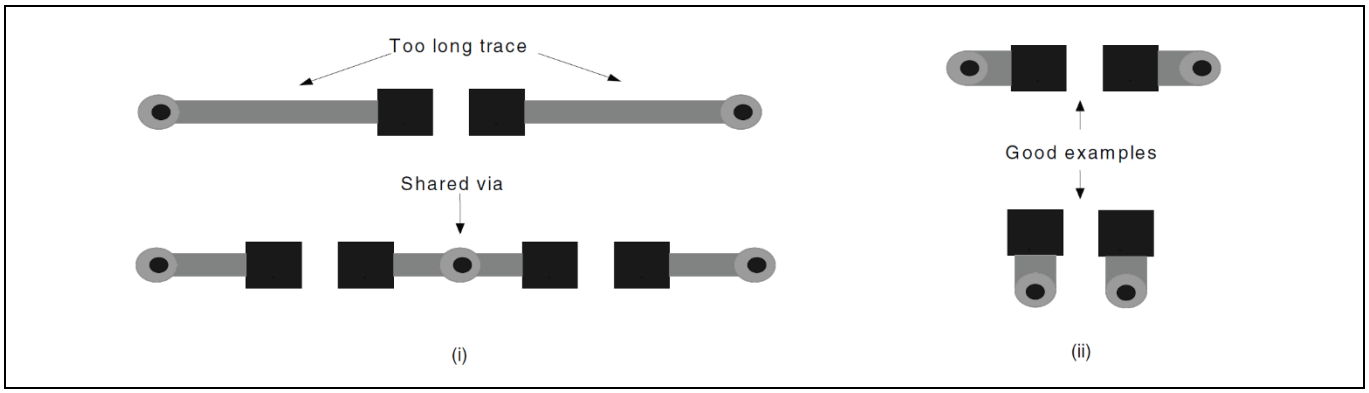


Figure 18 Decoupling Capacitor Routing Techniques: (i) Poor Routing examples, (ii) Good Routing examples

7 Test Points and Oscilloscope measurements

You should perform signal quality, timing, and power delivery characterization using industry-standard digital signal evaluation techniques. The statements below outline a few of those techniques.

- Test points should be as close as possible to the controller and the Semper Flash package pins for DQ[7:0] signals. In addition, the test points should be located as close as possible to the Semper Flash memory package pin for the remaining the signals.
- Measure meaningful signals as close to the flash memory device as possible when the controller is driving. When the flash memory device is driving, the opposite is true.
- While creating a test pad, the stub (extra inductance and capacitance) resulting from the test pad should be minimized. It is better to probe at the breakout via rather than creating test pad stubs. In addition, in the case of 4-layer PCBs with through-hole vias, probe signals at the bottom of the PCB on the through-hole vias if possible.
- While performing scope measurements, use a 3-GHz or greater bandwidth scope and low-impedance probes. This will provide a more accurate representation of the waveform transition (such as the rising and the falling portion of the waveform).
- Always measure V_{CC}-V_{SS} at the controller, the voltage regulator, next to the connector (either side), and at the flash memory. This needs to be performed prior to making any signal measurements to ensure that the supply is not noisy, which will affect the signal timing. In addition, these measurements establish the IR drop from regulator to controller or the regulator to the flash device.
- While measuring signals, it is a good idea to set the trigger on the most common switching signals, such as CS# or CK.

Related documents

[1] S25HS-T/S25HL-T

- 002-12345: Datasheet: S25HS256T, S25HS512T, S25HS01GT, S25HL256T, S25HL512T, S25HL01GT, 256 Mb/512 Mb/1 Gb SEMPER™ Flash Quad SPI, 1.8 V/3.0 V
- 002-12340: Datasheet: S25HS02GT, S25HS04GT, S25HL02GT, S25HL04GT, 2 Gb/4 Gb SEMPER™ Flash Quad SPI, 1.8 V/3.0 V

[2] S28HS-T/S28HL-T

- 002-18216: Datasheet: S28HS256T, S28HS512T, S28HS01GT, S28HL256T, S28HL512T, S28HL01GT, 256 Mb/512 Mb/1 Gb SEMPER™ Flash Octal interface, 1.8 V/3.0 V
- 002-23755: Datasheet: S28HS02GT, S28HS04GT, S28HL02GT, S28HL04GT, 2 Gb/4 Gb SEMPER™ Flash Octal interface, 1.8 V/3.0 V

[3] S26HS-T/S28HL-T

- 002-12337: Datasheet: S26HS256T, S26HS512T, S26HS01GT, S26HL256T, S26HL512T, S26HL01GT, 256 Mb/512 Mb/1 Gb SEMPER™ Flash HYPERBUS™ interface, 1.8 V/3.0 V
- 002-23793: Datasheet: S26HS02GT, S26HS04GT, S26HL02GT, S26HL04GT, 2 Gb/4 Gb SEMPER™ Flash HYPERBUS™ interface, 1.8 V/3.0 V

Revision history

Document version	Date of release	Description of changes
**	2018-07-02	New spec.
*A	2018-12-19	Updated Introduction: Updated description. Added “Semper Flash with Quad SPI Family”. Added “Semper Flash with Octal Interface Family”. Added “Semper Flash with HyperBus Interface Family”. Updated Signal Descriptions and Schematic: Replaced “Signal Descriptions” with “Signal Descriptions and Schematic” in heading. Removed description. Updated Semper Flash with Quad SPI: Updated description. Removed figure “Quad SPI Interface”. Added figure “Quad SPI Recommended Schematic”. Added table “Recommended Capacitor Terminations”. Updated Semper Flash with Octal Interface: Updated description. Removed figure “Octal Interface”. Added figure “Octal Interface Recommended Schematic”. Added table “Recommended Resistor and Capacitor Terminations”. Updated Semper Flash with HyperBus Interface: Updated description. Removed figure “HyperBus Interface”. Added figure “HyperBus Interface Recommended Schematic”. Added table “Recommended Resistor and Capacitor Terminations”.
*B	2021-03-16	Migrated to Infineon template.
*C	2023-10-18	Updated Signal Routing guidelines: Updated Length Matching: Updated Table 10. Updated Package Connection diagrams: Updated Land Pattern Recommendations: Updated Table 11. Updated Related documents: Updated details. Updated to new template.

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