Automotive Safety Applications with S6BP501A, S6BP502A, and Traveo MCU

About this document

Scope and purpose

AN223893 provides design guidelines on how to implement Cypress S6BP501A and S6BP502A automotive-grade power management ICs (PMICs) as a power supply for electronic devices including Cypress Traveo™ MCUs in an automotive electric and electronic system that targets the ISO 26262 functional safety standard.

Associated Part Family

S6BP501A, S6BP502A

Related Application Notes

AN99435, **AN219802**

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1 Introduction

Cars today are getting more electrified and the electronic equipment is getting sophisticated. More and more semiconductor devices are integrated in an electronic control unit (ECU), facilitating drivers' safety. For these ECUs, power supply failure is a significant hazard; therefore, functional safety for power management ICs (PMIC) must be taken into consideration when implemented in a system. Cypress offers safety-aware PMICs that are used in conjunction with safety microcontrollers to ensure that the power supply system meets safety standard requirements.

This application note provides design guidelines on how to implement S6BP501A and S6BP502A as a power supply for electronic devices including Cypress Traveo™ microcontroller unit (MCU) in an automotive electric and electronic system that targets ISO 26262 functional safety standard.

2 S6BP501A and S6BP502A features

S6BP501A and S6BP502A series PMICs regulate three power rails to supply electrical power to electric and electronic devices as shown in **Figure 1**. Additionally, they provide safety functions for the system to satisfy the ISO 26262 safety requirement. This section gives the list of the features of S6BP501A and S6BP502A.

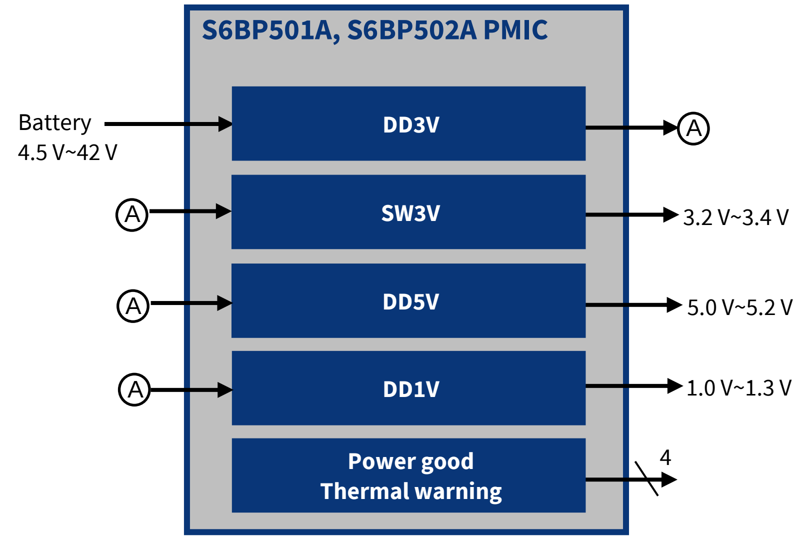

Figure 1 Power management system block diagram

Power good and thermal warning are the function names of the PMIC (refer to the **datasheet**).

Table 1 Combination between Traveo MCU and PMIC by Cypress

Traveo MCU	PMIC
S6J3310, S6J3320, S6J3330, S6J3340, S6J3350 series (Core voltage: 1.15 V)	S6BP501A 5 V / 1.3 A, 3.3 V / 1.6 A, 1.15 V / 1.4 A
S6J3200, S6J32E, S6J32F, S6J32G series (Core voltage: 1.20 V)	S6BP502A *1 5 V / 1.3 A, 3.3 V / 1.9 A, 1.20 V / 2.0 A

*1: In this case, S6BP501A can also be used as long its current capability satisfies system's required current.

2.1 Voltage regulators

S6BP501A and S6BP502A include three Switching Mode Power Supplies (SMPS) – DD3V, DD5V, and DD1V.

2.1.1 DD3V primary DC/DC switching controller

These PMICs have a three-channel output for the high-voltage step-down DC/DC controller (DD3V). The DD3V controller has two MOSFET gate drivers to drive the external high-side MOSFET and the external low-side MOSFET for a buck regulator. SW3V is the load switch for DD3V. DD3V has overcurrent protection (OCP) and overvoltage protection (OVP).

2.1.2 DD5V and DD1V secondary DC/DC switching converters

These PMICs have one step-down DC/DC converter with built-in switching FETs (DD1V), and one step-up DC/DC converter with built-in switching FETs (DD5V). DD5V and DD1V have overcurrent protection (OCP) and overvoltage protection (OVP) as protection functions.

2.1.3 Overcurrent protection (OCP)

Overcurrent protection prohibits the output current from going beyond the rated value, thus protecting subsequent devices. The inductor's peak current is checked at every switching cycle and will be limited once it reaches the threshold current value. As a result, the output voltage drops during OCP, but the switching operation continues.

The method of checking an inductor's peak current differs depending on each SMPS channel. See **Table 2**.

Table 2 Safe states for the assumed system

SMPS channel	Method of checking inductor's peak current
DD3V	Voltage between CSP and CSN terminal (voltage on Rs)
DD5V	Conducted current of low side switching FET inside PMIC
DD1V	Conducted current of high side switching FET inside PMIC

2.1.4 Overvoltage protection (OVP)

Overvoltage protection stops switching operations of all SMPS channels to protect subsequent devices when output voltage rises. Switching operation of all SMPS channels will be restarted when the voltage of the release detection terminals becomes 0.94 V or lower. Release detection terminals are different for each SMPS channels. See the 'Over voltage protection (OVP) voltage' and 'Over voltage protection release voltage' sections of each SMPS channel under 'Electrical Characteristics' in the datasheet.

2.2 Power-good monitor for each output

S6BP501A and S6BP502A provide active HIGH open-drain indicators for each voltage regulator as overvoltage detection (OVD) and undervoltage detection (UVD) to ensure that the output voltages are in the prescribed range. If S6BP501 and S6BP502A fail to regulate any of the power rails, the device detects the error and de-asserts the Power-Good signal.

2.3 Thermal warning indicator (TWI) and thermal shutdown (TSD)

S6BP501A and S6BP502A have active LOW open-drain Thermal Warning Indicators to alert subsequent devices when the device temperature reaches +140 °C (typ.), which is close to the temperature limit. The temperature is monitored locally along with the voltage regulators. When the device temperature reaches +165 °C (typ.), Thermal shutdown occurs so that switching operations of DD3V, DD5V, and DD1V stop.

2.4 Undervoltage lockout (UVLO)

S6BP501 and S6BP502A are equipped with UVLO functions to prevent themselves from operating unintentionally under low-voltage conditions, thus destroying or deteriorating subsequent devices. This function monitors the VB voltage as the power supply to the control block. Switching operations of DD3V, DD5V, and DD1V stop when the VB voltage drops to 4.3 V (typ.).

3 Safety considerations for S6BP501A/S6BP502A with Traveo MCU

This section describes how to use S6BP501A and S6BP502A with Traveo family MCUs, which are automotive-grade microcontrollers from Cypress, for safety applications.

An instrument cluster system is taken as an application example of interest. The instrument cluster comprises a speedometer, gas gauge, tachometer, coolant temperature gauge, gear position indicator, telltales, and a color TFT LCD. **Figure 2** depicts a block diagram of the system where S6BP502A (or S6BP501A) and Traveo family MCU are used.

In this example, the MCU connects to a Display through an RGB video interface (3.3-V bus connect), and Low Voltage Diferential Signaling is not used. Note that that bypass capacitors for the Traveo MCU are not illustrated; refer to the Technical Reference Manual of the Traveo family for the requirements for bypass capacitors.

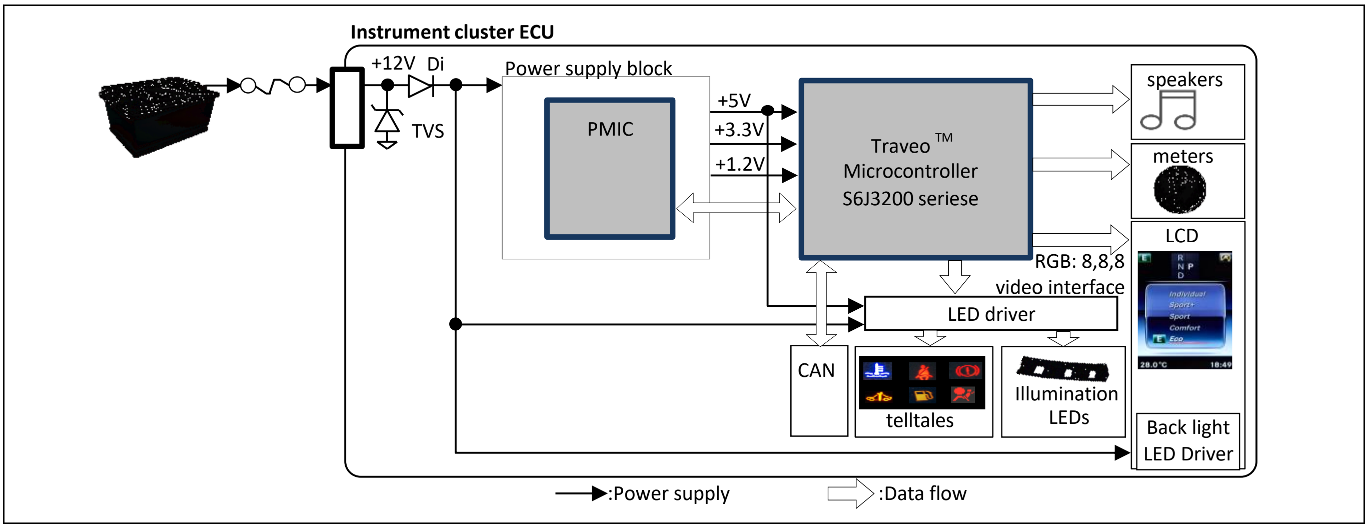

Figure 2 Instrument cluster block diagram

3.1 Safety mechanisms

To mitigate the risk of hazards caused by system failures, it is recommended to use safety mechanisms provided by PMIC, Traveo MCU, and other devices.

3.1.1 Power fail management

Power rail regulation faults lead to malfunction of connected devices such as a Traveo MCU. The Power-good feature of S6BP501A or S6BP502A detects such faults and triggers safety mechanisms to bring the system to a safe state.

- The Power-good signals (PG) should be pulled up to the same power rail which provides power for the MCU GPIO terminals (e.g., interrupt), through resistors on the order of 100 kΩ.
- The PG signal should be connected to the Traveo MCU's interrupt inputs. Upon receiving a low-level interrupt signal, the MCU can transition into the SysSafe-4 state.

Note: Apart from Power-good signals, Traveo MCUs have low-voltage detection (LVD) mechanisms that monitor the integrity of their own power sources.

3.1.2 Power-up sequence management

To provide safe power up, S6BP501A and S6BP502A have a UVLO function that prevents contingent and/or uncertain operation of the device under low supply voltage conditions.

Enable terminals (EN1V and EN3V) should be controlled by the Traveo MCU to configure an appropriate power up sequence for the system. **Figure 3** illustrates the power up sequence in the system depicted in **Figure 2**.

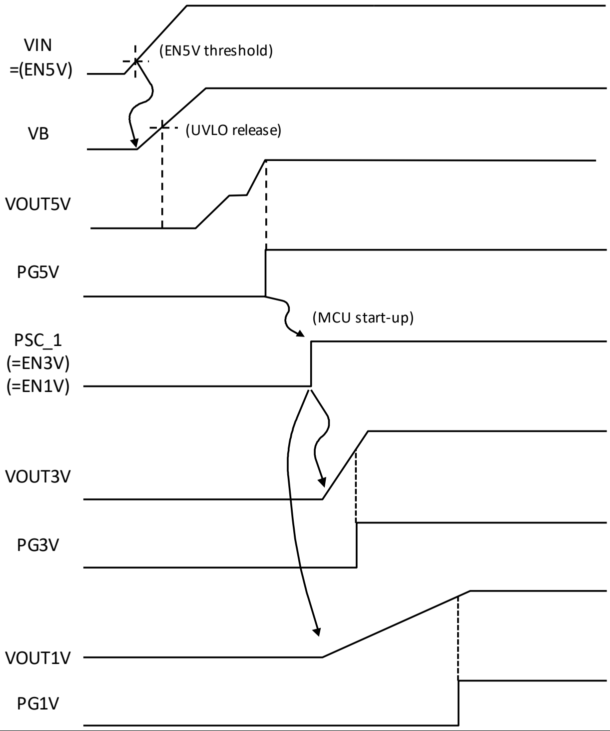

Figure 3 Power up sequence

Regulator (VB) in S6BP502A starts working when the EN5V threshold voltage is reached after 12 V is supplied. Shortly after the VB voltage reaches the UVLO threshold voltage, VOUT5V is initialized and the PG5 voltage starts to rise. For the detailed sequence, see the Function Description – Operation sequence described in the **S6BP502A Datasheet**. MCU initialization starts according to the rising edge of the PG5V signal. At the end of initialization, the Traveo MCU asserts PSC_1, which is connected to EN3V and EN1V, to power up 3.3 V and 1.2 V as VOUT3V and VOUT1V.

3.1.3 Thermal management

Overheating can cause malfunction of devices. Even though the devices usually shut themselves down in overheat conditions for safety reasons, it is recommended to manage overheating before losing the system's functionality.

- The thermal warning signal (HOT) should be pulled up to the 5.0 V power rail through a resistor on the order of 100 kΩ.
- The HOT signal can be connected to the Traveo MCU for regular monitoring.
- Upon receiving the HOT signal, the Traveo MCU can cool the system using external measures (e.g., turning on a cooling fan) or reduce the heat dissipation (e.g., lower the MCU clock speed by reducing workload, dimming the LCD backlight and illuminations).

3.1.4 Requirements for external components

To prevent electrical overstress (EOS) from damaging S6BP501A and S6BP502A, the following external devices must be installed in the system (refer to **Figure 2**).

- Reverse polarity protection
  To protect the devices from reverse polarity battery connection, which is often caused by human error during battery replacement, a rectifier diode shall be installed between the vehicle battery and VIN terminal.
- Load dump protection
  To protect the devices from a load dump surge caused by the disconnection of the vehicle battery from the alternator while the battery is being charged, a transient voltage suppressor (TVS) shall be installed to clamp the surge voltage.
- Fuse
  Although the S6BP series PMIC provides overcurrent protection, it is highly recommended to install a fuse to prevent the devices from being damaged by unexpected high current. A proper selection of fuse is necessary.
- Watchdog timer
  The watchdog timer should be serviced by the Traveo MCU. It applies an asynchronous reset to the Traveo MCU in case it finds discrepancies.
  Because the Traveo MCU plays an important role for safety, its hang-up or malfunction must be detected and handled properly to bring the system into a SysSafe state.

3.2 Safe state definitions

Table 3 defines Safe States for the assumed system. This table is same as in **AN219802**.

Table 3 Safe states for the assumed system

State name	Description
SysSafe-1 state	The system has a blank screen on the LCD while the Traveo MCU is unpowered. It is assumed that the system is designed in a way to show nothing (blank screen) on the LCD when the Traveo MCU is unpowered in order not to give false information to the driver. The transition from powered to unpowered state and the other way around is expected to be covered by the system to maintain this safe state.
SysSafe-2 state	The system has a blank screen on the LCD while the Traveo MCU is being reset. It is assumed that the safety-related signals are kept in safe states during the reset state without proper control by the Traveo MCU. Pull-down resistors and pull-up resistors are typically used.
SysSafe-3 state	The system is working correctly in fault-free condition (e.g., correct software execution, correct representation of the safety-related graphical information, warning icons.) It is assumed that the system maintains its safe state if the Traveo MCU is free of faults and operates correctly.
SysSafe-4 state	The system is working with errors being detected. The failure detection state of the MCU after a safety mechanism detected any failure and reacted appropriately (such as activated/deactivated an external error notification pin, automatically disabled the display output, display output resulting in no picture at all or in a blank screen). It is assumed that the system enters and maintains its safe state if a failure in the MCU has been detected and reported. This is expected to be done within the appropriate fault tolerant time interval.

3.3 Open and short faults

Figure 4 illustrates the connections between just a vehicle battery, a PMIC and a Traveo MCU to simplify the analysis. The balloons in the figure show the locations of possible open-faults and short-faults of PMIC during operation. **Table 4** and **Table 5** show how open faults and short faults are brought to a SysSafe state, respectively.

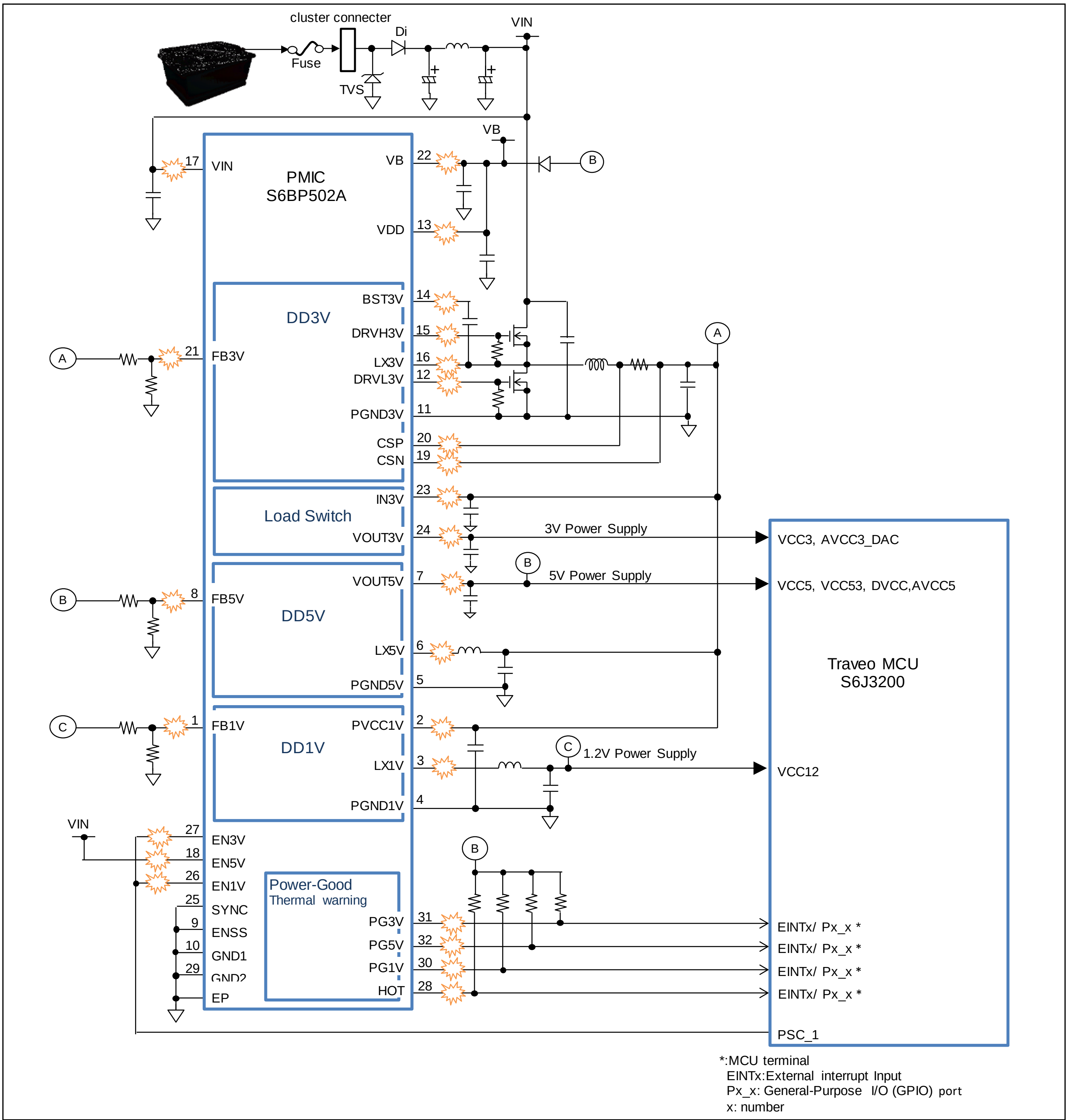

Figure 4 Faults handled by MCU and/or PMIC

Table 4 Open fault handling

Terminal number	Fault mode	Results in	Description
1	open	–	Open fault at FB1V causes PG1 unstable state and unstable voltage due to FB1V floating gate. Output voltage ranges from 0 V to 3.3 V.
2, 3	open	SysSafe-1	No output voltage at VOUT1V. PG1 turns LOW. The system turns to SysSafe-1 state.
6, 7	open	SysSafe-1	No output voltage at VOUT5V. PG5 turns LOW. The system turns to SysSafe-1 state.
8	open	SysSafe-1	Open fault at FB5V causes PG5 unstable state and unstable voltage due to FB5V floating gate. Output voltage ranges from 0 V to 6 V. OVP triggers and all channels are turned off. The system turns to SysSafe-1 state.
12	open	–	Open at DRVL3V turns the low side FET OFF and leads to asynchronous switching due to body diode. Consequently, there will be low side FET heating. However, output voltage stays normal.
13	open	SysSafe-1	Open at VDD means there is no DD3V drive power and both FETs are OFF. Therefore, all PG pins stay LOW and no output voltage across all channels. The system turns to SysSafe-1 state.
14	open	SysSafe-2	Open at BST3V causes constant 5 V at BST3V. Therefore, output voltage at DD3V is only around 2 V due to Vgs at FET. This triggers UVD and high side FET always stays ON. In this case, MCU resets and the system turns into SysSafe-2 state.
15	open	SysSafe-1	DRVH3V open results in 0-V gate voltage of high side FET. Therefore, high side FET stops switching. Consequently, no output voltage across all channels. The system turns to SysSafe-1 state.
16	open	–	Open at LX3V means high side drive circuit power supply is open, thus no voltage can be applied to high side FET. FET stops working which leads to no output voltage across all channels. The system turns to SysSafe-1 state.
17	open	–	System continues to operate normally on VB after start up. However, restart is not available.
18	open	SysSafe-1	Open at EN5V means IC is disabled. No output at all channels. The system turns to SysSafe-1 state.
19, 20	open	SysSafe-2	High side FET OFF timing becomes abnormal thus lead to unstable output voltage. PG3 turns LOW. The system turns in to SysSafe-2 state.
21	open	SysSafe-1	Open fault at FB3V causes PG3 unstable state and unstable voltage due to FB3V floating gate. Output voltage ranges from 0 V to 3.85 V. OVP triggers and all channels are turned OFF. The system turns to SysSafe-1 state.
22	open	SysSafe-1	Due to the UVLO function, a VB open-fault deactivates the power rail regulation. The Traveo MCU becomes unpowered, and the system turns into SysSafe-1 state.

Terminal number	Fault mode	Results in	Description
23	open	SysSafe-1	Open at IN3V disables VOUT3V output. At the same time, DD1V stops working as it loses its power supply. The system turns into SysSafe-1.
24	open	–	Open at VOUT3V means MCU loses 3.3 V voltage. However, PG3V still detects power good as it monitors VOUT3V voltage internally.
26, 27	open	SysSafe-1	Due to the integrated pull-down resistors for EN pins, EN open-fault deactivates power rail regulation. The Traveo MCU becomes unpowered, and the system turns into SysSafe-1 state.
28	open	–	Open at HOT means hot detection feature is disabled as it stays HIGH constantly regardless of temperature.
30, 31, 32	open	–	Open at PG pins leads to PG pins stays HIGH regardless of output voltage. Thus, power good monitoring feature is disabled.

Table 5 Short-to-ground fault handling

Terminal number	Fault mode	Results in	Description
1	Short-to-GND	–	In case of short-to-GND at FB1V, OVP at DD1V stops working and VOUT1 increases until reaching 3.3 V. At the same time, PG1 turns LOW due to FB1V short-to-GND.
2, 6, 7, 19, 23, 24	Short-to-GND	SysSafe-1	DD3V OCP triggers and DD3V output voltage changes to 0 V. Therefore, all channels' output voltages become 0 V. The system turns into SysSafe-1 state.
3	Short-to-GND	SysSafe-1	DD1V OCP triggers to turn DD1V output OFF. PG1 turns LOW. MCU is thus unpowered and the system turns into SysSafe-1 state.
8	Short-to-GND	SysSafe-2	Short-to-GND at FB5V causes VOUT5V to increase until OVP is triggered. All channels stop, and then restart after OVP release. This sequence repeats. The system turns into SysSafe-2 state.
12	Short-to-GND	–	DD3V low side FET shuts down thus lead to asynchronous switching due to bode diode. There will be low side FET heating.
13, 22	Short-to-GND	SysSafe-1	Short-to-GND at VDD means there is no internal power supply. All channels stop working. The system turns into SysSafe-1 state.
14, 15	Short-to-GND	SysSafe-1	DD3V high side FET shuts down. DD3V output voltage goes to 0 V, thus all channels stop working. The system turns into SysSafe-1 state.
16, 17, 18, 20	Short-to-GND	SysSafe-1	Power supply is shorted to ground. Fuse at input is burned out which causes all channels to stop working. The system turns into SysSafe-1 state.
21	Short-to-GND	SysSafe-2	DD3V output rises to trigger OVP; then IN3V voltage drops until OVP release. This sequence repeats. The system turns into SysSafe-2 state.
26	Short-to-GND	SysSafe-1	VOUT1 is disabled. PG1 turns LOW. The system turns into SysSafe-1 state.

Terminal number	Fault mode	Results in	Description
27	Short-to-GND	SysSafe-1	VOUT3 is disabled. PG3 turns LOW. The system turns into SysSafe-1 state.
28	Short-to-GND	SysSafe-4	Short-to-GND at HOT will constantly triggers thermal warning regardless of temperature. The system turns into SysSafe-4 state.
30, 31, 32	Short-to-GND	SysSafe-4	Short-to-GND at PG will constantly have power good warnings even if the system is working properly. The system turns into SysSafe-4 state.

3.4 Intra-device faults

Cypress ran a deductive fault analysis (FTA) and an inductive fault analysis (FMEDA) on the design of S6BP501A and S6BP502A, and concluded that the probability of serious failures, including both systematic and random, are low enough to satisfy the ASIL-B metric defined in ISO 26262-5:2011 (SPFM ≥ 90%, LFM ≥ 60%, PMHF ≤ 10-7 h -1.)

4 Summary

This application note describes the realization method of specific functional safety for an automotive cluster based on the hardware aspects on integrating S6BP502A (or S6BP501A) and a Traveo MCU. Using information provided in this application note, cluster designers can determine whether their cluster design satisfies the ASIL metric defined in ISO 26262 5:2011. For further information on the material in this application note, contact a Cypress sales representative.

Revision history

Document version	Date of release	Description of changes
**	2018-07-11	New application note.
*A	2021-06-14	Updated to Infineon template. Completing Sunset Review.

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