Migration Guide for Micron MT25QU to Infineon S25FS-S Quad SPI Flash

About this document

Scope and purpose

This application note provides guidelines for migration from Micron's MT25QU to Infineon S25FS-S Quad SPI Flash memory products. It describes the similarities and differences in specifications to facilitate this migration.

Intended audience

This is intended for flash memory users who intend to migrate Micron's MT25QU to Infineon S25FS-S Quad SPI flash.

Table of contents

1 Introduction

This Migration Guide compares the functionalities described in Micron MT25QU and Infineon S25FS-S datasheets. It details the similarities and differences between these two device families to facilitate migration efforts. No actual tests are performed to verify the migration results. For device-specific information, refer to individual datasheets.

2 Features Comparison

Table 1 Features Comparison

Feature/Parameter	MT25QU	S25FS-S
Densities	128 Mb, 256 Mb, and 512 Mb	128 Mb, 256 Mb, and 512 Mb
Bus Width	x1, x2, x4	x1, x2, x4
Supply Voltage	1.7 V–2.0 V	2.7 V–3.6 V
Normal Read Speed (SIO)	6.75 MB/s (54 MHz)	6.25 MB/s (50 MHz)
Fast Read Speed (SIO)	21 MB/s (166 MHz)	17 MB/s (133 MHz)
Dual Read Speed (DIO)	42 MB/s (166 MHz)	33 MB/s (133 MHz)
Quad Read Speed (QIO)	83 MB/s (166 MHz)	67 MB/s (133 MHz)
Quad Read Speed (QIO - DDR)	90 MB/s (90 MHz)	80 MB/s (80 MHz)
Program Buffer Size	256B	256B or 512B
Erase Sector Size	4 KB / 32 KB/ 64 KB	64 KB or 256 KB
Parameter Sector Size	4 KB	4 KB
Security Region / OTP	64 Bytes	1024 Bytes
Data Protection	Legacy Protection Advanced Security Protection	Legacy Protection Advanced Sector Protection
Suspend / Resume	Erase / Program	Erase / Program
Addressing	3-Byte, 4-Byte	3-Byte, 4-Byte
Hardware Reset	Yes	Yes[1]
Operating Temperature	–40°C to +105°C (128/256Mb) 40°C to +125°C (512Mb)	–40°C to +125°C
Deep Power Down	Yes	Yes
XIP Mode[2]	Yes	Yes
ID and SFDP	Yes	Yes
Packages	See **Table 14**	

1 Shared with IO3 pin

2 S25FS-S uses the mode cycle to support the XIP function, but MT25QU uses registers to enter and exit XIP mode.

3 Sector Architecture

Micron MT25QU devices have a uniform sector size of 64 KB. They also offer subsector erase size of 4 KB and 32 KB.

Infineon S25FS128S and S25FS256S devices can be configured to have a uniform 64-KB sectors, or a hybrid option with a set of eight 4-KB sectors, one 32-KB sector at the bottom or top, with all remaining sectors of 64 KB.

S25FS512S devices can be configured to have a uniform 256-KB sectors, or a hybrid option with a set of eight 4-KB sectors, one 224-KB sector at the bottom or top, with all remaining sectors of 256 KB. Depending on the application, you can configure the sector architecture by using the configuration register.

The following tables show detailed sector address maps in S25FS-S devices with different configurations.

Table 2 S25FS128S Sector Address Map, Bottom 4-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
4	8	SA00	00000000h-00000FFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA07	00007000h-00007FFFh	
32	1	SA08	00008000h-0000FFFFh	
64	255	SA09	00010000h-0001FFFFh	
		…	…	
		SA263	00FF0000h-00FFFFFFh	

Table 3 S25FS128S Sector Address Map, Top 4-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
64	255	SA00	00000000h-0000FFFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA254	00FE0000h-00FEFFFFh	
32	1	SA255	00FF0000h-00FF7FFFh	
4	8	SA256	00FF8000h-00FF8FFFh	
		…	…	
		SA263	00FFF000h-00FFFFFFh	

Table 4 S25FS128S Sector Address Map, Uniform 64-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
64	256	SA00	00000000h-0000FFFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA255	00FF0000h-00FFFFFFh	

Table 5 S25FS256S Sector Address Map, Bottom 4-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
4	8	SA00	00000000h-00000FFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA07	00007000h-00007FFFh	
32	1	SA08	00008000h-0000FFFFh	
64	511	SA09	00010000h-0001FFFFh	
		…	…	
		SA519	01FF0000h-01FFFFFFh	

Table 6 S25FS256S Sector Address Map, Top 4-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
64	511	SA00	00000000h-0000FFFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA510	01FE0000h-01FEFFFFh	
32	1	SA511	01FF0000h-01FE7FFFh	
4	8	SA512	01FF8000h-01FF8FFFh	
		…	…	
		SA519	01FFF000h-01FFFFFFh	

Table 7 S25FS256S Sector Address Map, Uniform 64-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
64	512	SA00	00000000h-0000FFFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA511	01FF0000h-01FFFFFFh	

Table 8 S25FS512S Sector Address Map, Bottom 4-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
4	8	SA00	00000000h-00000FFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA07	00007000h-00007FFFh	
224	1	SA08	00008000h-0003FFFFh	
256	255	SA09	00040000h-0007FFFFh	
		…	…	
		SA263	03FC0000h-03FFFFFFh	

Sector Architecture

Table 9 S25FS512S Sector Address Map, Top 4-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
256	255	SA00	00000000h-0003FFFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA254	03F80000h-03FBFFFFh	
224	1	SA255	03FC0000h-03FF7FFFh	
4	8	SA256	03FF8000h-03FF8FFFh	
		…	…	
		SA263	03FFF000h-03FFFFFFh	

Table 10 S25FS512S Sector Address Map, Uniform 256-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
256	256	SA00	00000000h-0003FFFFh	Sector Starting Address - Sector Ending Address
		…	…	
		SA255	03FC0000h-03FFFFFFh	

4 Command Set Comparison

Table 11 Command Set Comparison

Function	Command	Description	MT25QU	S25FS-S
Read Device ID	RDID	Read ID (JEDEC Manufacturer ID)	9Eh/9Fh	9Fh
	RSFDP	Read JEDEC Serial Flash Discoverable Parameters	5Ah	5Ah
	RDQID	Read Quad ID	AFh	AFh
Reset	RSTEN	Software Reset Enable	66h	66h
	RST/RESET	Software Reset	99h	99h
	RESET	Legacy Software Reset	–	F0h
	MBR	Mode Bit Reset	–	FFh
Deep Power Down	DPD	Deep Power Down	B9h	B9h
	RES	Release from DPD	ABh	ABh
Register Access	RDSR	Read Status Register	05h	05h
	RDSR2	Read Status Register 2	–	07h
		Read Flag Status Register	70h	–
	RDCR	Read Configuration Register 1	–	35h
		Read Non-volatile Configuration Register	B5h	–
		Read Volatile Configuration Register	85h	–
		Read Enhanced Volatile Configuration Register	65h	–
		Read Extended Address Register	C8h[3]	
		Read General Purpose Read Register	96h	–
	RDAR	Read Any Register	–	65h
	WRR	Write Register	01h	01h
		Write Non-volatile Configuration Register	B1h	–
		Write Volatile Configuration Register	81h	–
		Write Enhanced Volatile Configuration Register	61h	–
		Write Extended Address Register	C5h1	
	WRAR	Write Any Register	–	71h
	CLSR	Clear Status Register	50h	30h / 82h
	ECCRD	ECC Read	–	19h
	4ECCRD	4-Byte ECC Read	–	18h
	SBL	Set Burst Length	–	C0h
	EES	Evaluate Erase Status	–	D0h
	DLPRD	Data Learning Pattern Read	–	41h

3 256 Mb and 512 Mb only

Command Set Comparison

Function	Command	Description	MT25QU	S25FS-S
	PNVDLR	Program NV Data Learning Register	–	43h
	WVDLR	Write Volatile Data Learning Register	–	4Ah
4-Byte Mode		Enter 4-Byte Address Mode	B7h	B7h
		Exit 4-Byte Address Mode	E9h	–
Quad I/O Mode		Enter Quad Input/Output Mode	35h	–
		Reset Quad Input/Output Mode	F5h	–
Read Flash Array	READ	Read (1-1-1)	03h	03h
	FAST_READ	Fast Read (1-1-1)	0Bh	0Bh
	DOR	Dual Output Read (1-1-2)	3Bh	–
	QOR	Quad Output Read (1-1-4)	6Bh	–
	DIOR	Dual I/O Read (1-2-2)	BBh	BBh
	QIOR	Quad I/O Read (1-4-4)	EBh	EBh
	DDRFR	DDR Fast Read (1-1-1)	0Dh	–
		DDR Dual Output Read (1-1-2)	3Dh	–
		DDR Quad Output Read (1-1-4)	6Dh	–
	DDRDIOR	DDR Dual I/O Read (1-2-2)	BDh	–
	DDRQIOR	DDR Quad I/O Read (1-4-4)	EDh	EDh
	QIOWR	Quad I/O Word Read (1-4-4)	E7h	–
	4READ	4-Byte Read (1-1-1)	13h	13h
	4FAST_READ	4-Byte Fast Read (1-1-1)	0Ch	0Ch
	4DOR	4-Byte Dual Output Read (1-1-2)	3Ch	–
	4QOR	4-Byte Quad Output Read (1-1-4)	6Ch	–
	4DIOR	4-Byte Dual I/O Read (1-2-2)	BCh	BCh
	4QIOR	4-Byte Quad I/O Read (1-4-4)	ECh	ECh
	4DDRFR	4-Byte DDR Read (1-1-1)	0Eh	–
	4DDRDIOR	4-Byte DDR Dual I/O Read (1-2-2)	BEh	–
	4DDRQIOR	4-Byte DDR Quad I/O Read (1-4-4)	EEh	EEh
Write Operations	WREN	Write Enable	06h	06h
	WRDI	Write Disable	04h	04h
Program Flash Array	PP	Page Program (1-1-1)	02h	02h
		Dual Input Fast Program (1-1-2)	A2h	–
		Extended Dual Input Fast Program (1-2-2)	D2h	–
	QPP	Quad Input Fast Program (1-1-4)	32h	–
		Extended Quad Input Fast Program (1-4-4)	38h	–
	4PP	4-Byte Page Program (1-1-1)	12h	12h
	4QPP	4-Byte Quad Input Fast Program (1-1-4)	34h	–
		4-Byte Quad Input Extended Fast Program (1-4-4)	3Eh	–

Command Set Comparison

Function	Command	Description	MT25QU	S25FS-S
Erase Flash Array	P4E	4-KB SubSector Erase	20h	20h[4]
		32-KB SubSector Erase	52h	–
	SE	Sector Erase	D8h	D8h
	CE	Chip Erase / Bulk Erase	C7h/60h	C7h/60h
	4SE	4-Byte Sector Erase	DCh	DCh
	4P4E	4-Byte 4-KB SubSector Erase	21h	21h1
		4-Byte 32-KB SubSector Erase	5Ch[5]	–
Erase / Program Suspend / Resume	EPS	Erase / Program Suspend	75h	75h / 85h / B0h
	EPR	Erase / Program Resume	7Ah	7Ah / 8Ah / 30h
One-Time Programmable (OTP) Array	OTPR	OTP Read	4Bh	4Bh
	OTPP	OTP Program	42h	42h
Array Protection	ASPRD	ASP Read	–	2Bh
	ASPP	ASP Program	–	2Fh
	PLBWR	PPB Lock Bit Write	–	A6h
	PLBRD	PPB Lock Bit Read	–	A7h
	DYBRD	DYB Read	–	FAh
	DYBWR	DYB Write	–	FBh
	4DYBRD	4-Byte DYB Read	–	E0h
	4DYBWR	4-Byte DYB Write	–	E1h
	PPBRD	PPB Read	–	FCh
	PPBWR	PPB Write	–	FDh
	4PPBRD	PPB Read	–	E2h
	4PPBWR	PPB Write	–	E3h
	PPBE	PPB Erase	–	E4h
	PASSRD	Password Read	–	E7h
	PASSP	Password Program	–	E8h
	PASSU	Password Unlock	–	E9h
		Read Sector Protection	2Dh	–
		Program Sector Protection	2Ch	–
		Read Volatile Lock Bits	E8h	–
		Write Volatile Lock Bits	E5h	–
		Read Non-volatile Lock Bits	E2h	–
		Write Non-volatile Lock Bits	E3h	–
		Erase Non-volatile Lock Bits	E4h	–
		Read Global Freeze Bit	A7h	–

4 20h and 21h work for bottom or top 4-KB parameter sectors in S25FS-S.

5 512 Mb only

Function	Command	Description	MT25QU	S25FS-S
		Write Global Freeze Bit	A6h	–
		Read Password	27h	–
		Write Password	28h	–
		Unlock Password	29h	–
Advanced Function Interface		Interface Activation	9Bh	–
		Cyclic Redundancy Check	9Bh/27h	–

4.1 Identification Command

MT25QU devices can use either 9Eh or 9Fh to read the device ID. S25FS-S supports the 9Fh command only.

4.2 Status and Configuration Registers

Status Registers and Configuration Registers are defined quite differently in MT25QU and S25FS-S devices. The basic Status Register has some similar bits but all other registers are different. You must look at the bits that are currently being used with MT25QU and find the corresponding registers in S25FS-S.

Only the basic read, write, and clear Status Register commands are common in these two devices. Other register access commands in MT25QU are not supported in S25FS-S.

S25FS-S devices provide Read Any and Write Any Register commands to access all registers with an address offset. These new commands are not in MT25QU.

4.3 4-Byte Address Mode

In devices with capacities higher than 256 Mb, the 4-Byte addressing scheme is needed. Both MT25QU and S25FS-S provide a different set of commands that support 4-Byte addressing. This is the most straight-forward way to access the full range of the device.

If you prefer to keep old command values but want to use 4-Byte addressing, MT25QU supports a 4-Byte Address Mode that can be entered or exited with a command. S25FS-S uses the same 4-Byte enter command, i.e. B7h; however, to exit such mode, a hardware or software reset is required.

4.4 Read Access Commands

Basic read commands are compatible in both MT25QU and S25FS-S devices. Both of them support Normal Read (1-1-1), Fast Read (1-1-1), and DDR Quad I/O Read (1-4-4). However, Dual Output Read (1-1-2), Quad Output Read (1-1-4), Dual I/O Read (1-2-2), Quad I/O Read (1-4-4), DDR Read (1-1-1), DDR Dual I/O Read (1-2-2), DDR Dual Output Read (1-1-2) and DDR Quad Output Read (1-1-4) are not supported in S25FS-S.

Some read commands require a read latency to allow time to access the flash memory array. The read latency cycles are traditionally called dummy cycles. These dummy cycles are defined in Nonvolatile Configuration Register in MT25QU, while they are defined in Configuration Register 2 in S25FS-S. Look up the definitions of how the read latency is defined in each datasheet to find appropriate settings.

Table 12 shows the Latency Code definitions in S25FS-S Configuration Register 2.

Table 12 Infineon S25FS-S CR2 Read Latency Bits

Bits	Field Name	Function	Default State	Description
3	RL_NV (OTP) or RL_V (Volatile)	Read Latency	1	0 to 15 latency (dummy) cycles following read address or continuous mode bits.
2			0	
1			0	
0			0	

The 4-bit Read Latency field selects the number of dummy cycles between the end of mode cycle and the start of the read data output. You can write to the CR2V (Volatile register) to change the read latency value until the next power cycle during the development phase. Once you are satisfied with the final value, you may program the value into CR2NV (One Time Programmable) register so the device would default to that value after every power on reset.

Table 13 has the suggested Latency Code settings for different clock frequencies.

Table 13 Latency Codes Versus Frequency in S25FS-S

Latency Code	Read Command Maximum Frequency (MHz)			
	Fast Read (1-1-1) OTPR (1-1-1) RDAR (1-1-1) RDAR (4-4-4)	Dual I/O (1-2-2)	Quad I/O (1-4-4) Quad I/O (4-4-4)	DDR Quad I/O (1-4-4) DDR Quad I/O (4-4-4)
	Mode Cycles = 0	Mode Cycles = 4	Mode Cycles = 2	Mode Cycles = 1
0	50	80	40	N/A
1	66	92	53	22
2	80	104	66	34
3	92	116	80	45
4	104	129	92	57
5	116	133	104	68
6	129	133	116	80
7	133	133	129	80
8	133	133	133	80
9	133	133	133	80
10	133	133	133	80
11	133	133	133	80
12	133	133	133	80
13	133	133	133	80
14	133	133	133	80
15	133	133	133	80

4.5 Program Commands

Both MT25QU and S25FS-S support normal Page Programming (1-1-1) commands in 3-byte or 4-byte addressing modes. Dual Input Program (1-1-2), Extended Dual Input Program (1-2-2), Quad Input Program (1-1-4), and Extended Quad Input Program (1-4-4) are not supported in S25FS-S.

4.6 Dual I/O and Quad I/O Modes

In MT25QU devices, you can enter Dual I/O mode (2-2-2) or Quad I/O mode (4-4-4) for all commands by setting the corresponding bits in the Enhanced Volatile Configuration Register. Dual I/O mode (2-2-2) is not supported in S25FS-S devices. Quad I/O mode (4-4-4) is supported, and is known as Quad Peripheral Interface in S25FS-S

devices. You can enter QPI mode by setting one bit in the Configuration Register 2 in either the volatile or OTP version.

4.7 Erase Commands

MT25QU has 64-KB physical sectors. S25FS128S and S25FS256S also have 64-KB physical sectors, while S25FS512S has 256-KB sectors. The Sector Erase command in these devices is the same. MT25QU provides subsector erase commands for 4-KB and 32-KB subsectors. S25FS-S does not support the 32-KB subsector erase command. In S25FS-S, there is an option to have a set of eight 4-KB sectors on the bottom or on the top of the device. In such a case, 4-KB Erase command is supported on those sectors.

S25FS-S devices can also be configured with uniform 256-KB sectors. This option does not exist in MT25QU devices.

4.8 Suspend and Resume

Both MT25QU and S25FS-S support Erase and Program Suspend and Resume commands. The basic commands are the same, i.e., 75h and 7Ah. S25FS-S devices also provide additional commands for the same functions, i.e., 85h and 8Ah.

4.9 OTP Area

MT25QU has a dedicated 64-byte OTP area outside of the main memory array. S25FS-S has 1024-byte OTP area. To read or program this area, the commands are the same in these two devices.

To protect the OTP area, the methods in these two devices are different. Refer to individual datasheets for OTP protection methods.

4.10 Array Protection

Both MT25QU and S25FS-S provide legacy protection through BP bits. Furthermore, they both provide volatile and nonvolatile protections for individual sectors through registers. However, the ways of accessing these registers in MT25QU are quite different from S25FS-S. You must modify the software to support a totally new scheme of Advanced Sector Protection as described in the S25FS-S datasheet.

5 Hardware Comparison

5.1 Package Compatibility

Table 14 shows the supported packages in MT25QU and S25FS-S families with regard to their densities.

Table 14 Package Compatibility

Package Name	MT25QU			S25FS-S		
	128 Mb	256 Mb	512 Mb	128 Mb	256 Mb	512 Mb
8-pin SOIC (208 mil)	✓			✓		
16-pin SOIC (300 mil)	✓	✓	✓		✓	✓
8-Contact WSON (5 × 6 mm)	✓	✓		✓		
8-Contact WSON (6 × 8 mm)	✓	✓	✓	✓	✓	✓
5 x 5 24-ball FBGA (6 × 8 mm)	✓	✓	✓	✓	✓	✓
4 x 6 24-ball FBGA (6 × 8 mm)	✓	✓		✓	✓	

5.2 Signal Compatibility

Table 15 shows the Signal Pins comparison in MT25QU and S25FS-S families. Most signals are compatible in both device families. S25FS-S devices do not offer a separate RESET# pin. They can be configured to use the IO3 pin as the RESET# when Quad mode is not used.

Table 15 Signal Compatibility

MT25QU Signal	S25FS-S Signal	Description
S#	CS#	Chip Select
C	SCK	Serial Clock
DQ[3:0]	IO[3:0]	Data input and output
W#	WP#	Write Protect (IO2)
HOLD# (IO3)	RESET# (IO3)	Hold# (MT25QU) or RESET# (S25FS-S)
RESET#	-	Dedicated reset pin
Vcc	Vcc	Power Supply
Vss	Vss	Ground

5.3 DC Characteristics

Table 16 shows a comparison of basic DC parameters for MT25QU and S25FS-S 512-Mb density devices. For the complete parameters details specified, refer to the datasheets.

Table 16 DC Parameters Comparison (for 512-Mb density)

Symbol	Operating Parameter	MT25QU512			S25FS512S			Unit
		Min	Typical	Max	Min	Typical	Max	
V_{CC}	V_{CC} (Supply voltage)	1.7	–	2.0	1.7	–	2.0	V
V_{IL}	Input LOW Voltage	–0.5	–	0.3 x V_{CC}	–0.5	–	0.3 x V_{IO}	V
V_{IH}	Input HIGH Voltage	0.7 x V_{CC}	–	V_{CC} + 0.4	0.7 x V_{CC}	–	V_{IO} +0.4	V
V_{OL}	Output LOW Voltage	–	–	0.4		–	0.2	V

Symbol	Operating Parameter	MT25QU512			S25FS512S			Unit
		Min	Typical	Max	Min	Typical	Max	
V_{OH}	Output HIGH Voltage	V_{CC} – 0.2	–		V_{CC} – 0.2	–		V
I_{LI}	Input Leakage Current	–	–	±2	–	–	±2	µA
I_{LO}	Output Leakage Current	–	–	±2	–	–	±2	µA
I_{CC1}	Active Power Supply Current (READ) – Serial SDR@166 MHz	–	–	20	–	25	30	mA
	Active Power Supply Current (READ) – Quad DDR@90 MHz	–	–	31	–	70	90	mA
I_{CC2}	Active Power Supply Current (Page Program)	–	–	35	–	60	100	mA
I_{CC3}	Active Power Supply Current (WRR or WRAR)	–	–	35	–	60	100	mA
I_{CC4}	Active Power Supply Current (SE)	–	–	35	–	60	100	mA
I_{SB}	Standby Current (IT)	–	20	100	–	25	100	µA
	Standby Current (AT)	–	20	200	–	25	300	µA
	Standby Current (UT)	–	20	300	–	25	300	µA
I_{DPD}	Deep Power Down Current (IT)	–	2	50	–	8	50	µA
	Deep Power Down Current (AT)	–	5	100	–	8	150	µA
	Deep Power Down Current (UT)	–	5	150	–	8	250	µA

5.4 AC Characteristics

Table 17 shows a comparison of basic AC parameters for MT25QU and S25FS-S. For the complete parameters details specified, refer to the datasheets.

Table 17 AC Characteristics Comparison

Symbol	Parameter	MT25QU		S25FS-S		Unit
		Min	Max	Min	Max	
$F_{SCK, R}$	SCK Clock Frequency for READ and 4READ instructions	–	54	–	50	MHz
$F_{SCK, C}$	SCK Clock Frequency for dual and quad commands	–	166	–	133	MHz

Symbol	Parameter	MT25QU		S25FS-S		Unit
		Min	Max	Min	Max	
t_{WH}, t_{CH}	Clock HIGH Time	2.7 / 5.0 (STR / DTR)	–	45%/F_{SCK}	–	ns
t_{WL}, t_{CL}	Clock LOW Time	2.7 / 5.0 (STR / DTR)	–	45%/F_{SCK}	–	ns
t_{CRT}, t_{CLCH}	Clock Rise Time (slew rate)	0.1	–	0.1	–	V/ns
t_{CFT}, t_{CHCL}	Clock Fall Time (slew rate)	0.1	–	0.1	–	V/ns
t_{CS}	CS# HIGH Time (Any Read Instructions)	6	–	10	–	ns
	CS# HIGH Time (All other Non-Read instructions)	30	–	50	–	ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	2.7	–	2	–	ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	2.7	–	3	–	ns
t_{SU}	Data in Setup Time	1.75	–	2	–	ns
t_{HD}	Data in Hold Time	2 / 2.3 (STR / DTR)	–	3	–	ns
t_V	Clock LOW to Output Valid (30 pF)	–	6	–	8	ns
t_{HO}	Output Hold Time	1	–	1	–	ns
t_{DIS}	Output Disable Time	–	6	–	8	ns
t_{WPS}	WP# Setup Time	20	–	20	–	ns
t_{WPH}	WP# Hold Time	100	–	100	–	µs

5.5 Embedded Algorithms Performance

Table 18 shows a comparison of the program and erase performance for MT25QU and S25FS-S. For details of Program and Erase operations, refer to the datasheets.

Table 18 Program and Erase Performance Comparison

Symbol	Parameter		MT25QU		S25FS-S		Unit
			Typical	Max	Typical	Max	
t_W	Nonvolatile Register Write Time		200	1000	240	750	ms
t_{PP}	Page Programming (256 bytes)		120	2800	360	2000	µs
t_{BE}	Block Erase Time (64-KB physical sectors)		150	1000	240	725	ms
t_{CE}	Chip Erase Time	128 Mb	38	114	60	180	sec
		256 Mb	77	231	120	360	
		512 Mb	153	460	220	720	

6 Conclusion

The Infineon S25FS-S device is mostly pin-to-pin compatible with Micron MT25QU. To migrate to S25FS-S, you can keep most basic SPI commands but software modification efforts are needed to accommodate the sector architecture, register sets, and data protection methods offered by the MT25QU family.

References

[1] S25FS128S/ S25FS256S

- **002-00368: S25FS128S S25FS256S 1.8 V, Serial Peripheral Interface with Multi-I/O, MirrorBit™ Nonvolatile Flash**

[2] S25FS512S

- **002-00488: S25FS512S 512 Mbit, 1.8 V Serial Peripheral Interface with Multi-I/O Flash**

Revision history

Document version	Date of release	Description of changes
**	2018-06-14	New application note
*A	2021-04-30	Updated to Infineon template

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