Migrating from STK14C88 to STK14C88C

About this document

Scope and purpose

AN221988 discusses the key differences that need to be considered when migrating from STK14C88 to STK14C88C. STK14C88 is now “Obsolete”; this application note explains how STK14C88C is a replacement for STK14C88.

Intended audience

This document is intended for any who needs to migrate from STK14C88 to STK14C88C fast nonvolatile SRAM.

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1 Introduction

The Infineon STK14C88C is a 5 V, 256 Kbit (32 K x 8) nvSRAM in 0.13-micron technology. This part is functionally equivalent to STK14C88 in 0.8-micron technology but with some performance enhancements and a few differences in parameters. This application note highlights the differences between the STK14C88 and the STK14C88C and the parameters that must be considered while migrating.

1.1 Overview

The following tables compare the features and parameters of the two parts. As shown in **Table 1**, the 256 Kbit nvSRAM is available in x8 configuration.

Table 1 Part number description

Description	Original part number	Replacement part number
32 K x 8	STK14C88	STK14C88C

1.2 Feature set

Both the parts share the same overall feature set and are available in the operation speed bins given in **Table 2**.

Table 2 Feature set comparison

Feature Set	STK14C88	STK14C88C
AutoStore	Available	Available
Software STORE	Available	Available
Hardware STORE	Available	Available
Software RECALL	Available	Available
AutoStore Inhibit	Available	Not Available
AutoStore Enable/Disable	Not Available	Available
Preventing STORE on the fly	Available	Not Available
Speed	25 ns 35 ns 45 ns	- 35 ns -
STORE Cycles	Industrial: 1,000,000 Military: 1,000,00	Industrial: 1,000,000 Military: 1,000,00
Data Retention	100 years at 55°C	20 years at 85 °C
Operating Temperature Range	Industrial (–40 to 85°C) Military (–55 to 125°C)	Industrial (–40 to 85°C) Military (–55 to 125°C)
Packages	32-pin CDIP 32-pin CDIP (Solder dip finish)	32-pin CDIP -

2 Ordering part numbers

Table 3 lists the recommended STK14C88C ordering part numbers that correspond to STK14C88 (Obsolete) ordering part numbers.

Table 3 Recommended ordering part numbers for migration

STK14C88		STK14C88C		Comments
Ordering part number	**Status**	**Ordering part number**	**Status**	
STK14C88-C45I	Obsolete	STK14C88C-C35I	In plan	System software update is required for AC parameter difference and other features supported in STK14C88C. See **Critical considerations**.
STK14C88-5C35M		STK14C88C-5C35M		
STK14C88-5K45M		STK14C88C-5C35M		

2.1 Parameters

STK14C88C is a pin-compatible replacement for STK14C88 and will require minimum changes in the application board in most applications. However, differences in parameters should be considered before replacing one part with the other. Table 4 lists the differences in parameters between STK14C88 and STK14C88C.

Table 4 Parameter comparison

Parameter	Description	Speed	STK14C88		STK14C88C		Unit
			Min	Max	Min	Max	
DC parameters							
I_{CC1}	Average V_{CC} current	35 ns		85	-	85	mA
		45 ns	-	70	-	-	
I_{CC2}	Average V_{CC} current during STORE	-	-	3	-	15	mA
I_{CC3}	Average V_{CC} current at t_{RC} = 200 ns, 5 V, 25°C	-	10 (typ)		35 (typ)		
I_{CC4}	Average V_{CAP} current during AutoStore cycle	-	-	2	-	8	mA
I_{SB1}	Average V_{CC} standby current (Standby, cycling Input)	25 ns	-	31	Not specified		mA
		35 ns	-	26			
		45 ns	-	23			
I_{SB}	V_{CC} standby current	-	-	1.5	-	10	mA
I_{IX}	Input leakage current	-	–1	+1	–5	+5	uA
V_{IH}	Input high voltage	-	2.2		2.2	-	V
V_{OH}	Output HIGH voltage	-	-	2.4 (I_{OUT} = – 4 mA)	-	2.4 (I_{OUT} = – 2 mA)	V
V_{OL}	Output LOW voltage	-	-	0.4	-	0.4	V

Ordering part numbers

Parameter	Description	Speed	STK14C88		STK14C88C		Unit
			Min	Max	Min	Max	
				(I_{OUT} = 8 mA)		(I_{OUT} = 4 mA)	
V_{CAP}	Storage capacitor	-	68 to 220		61 to 180		µF
AC switching parameters							
t_{DOE}	Output enable to data valid	35 ns	-	15	-	15	ns
		45 ns	-	20	-	-	
t_{OHA}	Output hold after address change	-	5	-	3	-	ns
t_{LZCE}	Chip enable to output active	-	5	-	3	-	ns
t_{LZWE}	Output active after end of write	-	5	-	3	-	ns
AutoStore / Power-Up RECALL parameters							
$t_{HRECALL}$	Power-Up RECALL duration	-	-	0.55	-	20	ms
t_{STORE}	STORE cycle duration	-	-	10	-	8	ms
t_{VSBL}	Low voltage trigger (V_{SWITCH}) to $\overline{HSB}$ low	-	-	300	-	25	ns
V_{RESET}	Low voltage reset level	-	-	3.6	Not applicable		V
V_{SWITCH}	Low voltage trigger level	-	4.0	4.5	-	4.4	V
t_{DELAY}	Time allowed to complete SRAM write cycle	-	1,000	-	-	25	ns
V_{HDIS}	$\overline{HSB}$ output disable voltage	-	Not specified		-	1.9	V
t_{LZHSB}	$\overline{HSB}$ to output active time	-	Not specified		-	5	µs
t_{HHHD}	$\overline{HSB}$ high active time	-	Not specified		-	500	ns
Software controlled STORE/RECALL cycle parameters							
t_{HA}	Address hold time	-	20	-	0	-	ns
t_{RECALL}	RECALL duration	-	-	20	-	200	µs
Hardware STORE cycle parameters							
t_{HLBL}	$\overline{HSB}$ LOW to STORE busy	-	-	300	-	25 (t_{DELAY})	ns
t_{DHSB}	$\overline{HSB}$ to output active time when write latch not set	-	Not specified		-	25	ns

3 Critical considerations

The impact of the differences in STK14C88C with respect to STK14C88 in existing applications are discussed in this section. System designers are recommended to review the detailed datasheets when migrating to the new part.

3.1 DC parameters

I_{CC1} (Average current at full speed) is identical in STK14C88C and hence power supply design in applications with STK14C88 would require no changes when replacing the nvSRAM with STK14C88C in spite of the higher values in the lower speed / higher standby current. The critical parameter to consider is the V_{CAP}.

3.1.1 V_{CAP}

While most of the differences do not impact the application, the difference in V_{CAP} is a critical consideration while converting from the older rev parts. V_{CAP} is the capacitor that provides the required charge for AutoStore to complete NV store of the SRAM data during power down. The required capacitor range is different for the two parts.

Table 5 V_{CAP} comparison

Description	STK14C88	STK14C88C
V_{CAP}	68 µF to 220 µF	61 µF to 180 µF

Therefore, any existing application which uses a capacitor value outside the overlapping range (61 µF to 180 µF) the impact of capacitor dimensions needs to be considered while changing to the new capacitor.

Note: The capacitor range is the absolute value of the capacitor, net of tolerence.

3.2 AC switching parameters

There are a few minor differences in switching parameters between STK14C88C and STK14C88 as listed in the **Table 4**. However, these differences do not impact most applications. For replacing 45-ns speed parts, choose the 35-ns speed parts as replacement (since 45-ns speed grade is not available in STK14C88C).

3.2.1 AutoStore / Power-Up RECALL parameters

The power-up RECALL is much different in STK14C88C compared to STK14C88 because of architecture differences.

Table 6 $t_{HRECALL}$ comparison

Description	STK14C88	STK14C88C
$t_{HRECALL}$	550 µs	20 ms

This difference is not likely to affect applications because the initialization of the controller on the board happens at the same time. However, this should be taken into consideration when replacing STK14C88 with STK14C88C.

3.2.2 Software controlled STORE/RECALL cycle parameters

The software cycle parameter t_{RECALL} is different in STK14C88C as described below. The software address sequences are identical to that in the STK14C88 parts.

Software RECALL time (t_{RECALL}) is higher in STK14C88C.

Table 7 t_{RECALL} comparison

Description	STK14C88	STK14C88C
t_{RECALL}	20 µs	200 µs

This difference could require firmware change in the existing application to increase the controller wait state when software RECALL is initiated.

3.3 Software sequence

STK14C88C has been designed to be compatible with STK14C88 in software sequence modes. Therefore, the same Software STORE and RECALL address sequences in STK14C88 works in STK14C88C, requiring no firmware change. However, there is a difference in the required state of $\overline{OE}$ / $\overline{G}$ during the software sequence reads as explained further.

In STK14C88, while software sequence must be clocked with $\overline{CE}$ / $\overline{E}$ controlled reads, it is not necessary that $\overline{OE}$ / $\overline{G}$ be LOW for the sequence to be valid. That is, it is not necessary that the read is a real read with $\overline{OE}$ / $\overline{G}$ held LOW. However, in STK14C88C, the software sequence may be clocked with $\overline{CE}$ controlled reads or $\overline{OE}$ controlled reads. This means that while in STK14C88 parts, the $\overline{OE}$ / $\overline{G}$ state was immaterial, in STK14C88C parts, $\overline{OE}$ needs to be LOW for a valid software sequence read. It does not matter if $\overline{CE}$ goes LOW first or $\overline{OE}$ goes LOW first, but the read is valid for software sequence only when both $\overline{CE}$ and $\overline{OE}$ have gone LOW. In both STK14C88 and STK14C88C parts, $\overline{WE}$ must be kept HIGH for all the six read sequences.

In effect, this difference will affect applications where software sequence reads are done with $\overline{OE}$ / $\overline{G}$ held HIGH. Firmware change will be required to take $\overline{OE}$ LOW when using the new part STK14C88C. Applications where software sequence reads are performed with $\overline{OE}$ / $\overline{G}$ LOW do not require any change.

3.4 Hardware STORE cycle parameters

The Hardware STORE parameters are improved in STK14C88C. The improvements are listed under the **Details of improvement** section. No changes will be required in applications.

3.4.1 AutoStore Inhibit

STK14C88 has the AutoStore Inhibit feature and STK14C88C has AutoStore Disable mode. These two provide the same result of AutoStore disable but are done by different means: hardware in STK14C88 and software in STK14C88C.

To disable AutoStore in STK14C88, the power is to be connected to the V_{CAP} pin and the V_{CC} pin is grounded (or left open). This cannot be done in STK14C88C. For proper operation of the device, in STK14C88C, power is to be connected to the V_{CC} pin only. However, AutoStore disable is more easily done through the software sequence. Therefore, if STK14C88 is to be replaced in an application where AutoStore has been disabled, then the layout has to be modified to connect the power to the V_{CC} pin and a software sequence has to be used to disable AutoStore function followed by a Software STORE, the first time the board is powered up.

3.4.2 Preventing STORE

In STK14C88, the STORE function can be disabled on-the-fly by holding the $\overline{HSB}$ pin HIGH at the onset of STORE with a driver capable of sourcing 30 mA at a V_{OH} of at least 2.2 V. This feature is not available in the 0.13 µ parts. In STK14C88C, a STORE initiated by any means cannot be disabled on-the-fly.

3.5 Data retention

The data retention in STK14C88C is improved from the older technology part. STK14C88C has data retention of 20 years at 85°C against the STK14C88 data retention of 100 years at 55°C. This would translate to over four times improvement in data retention at the same temperatures.

4 Details of improvement

4.1 Hardware STORE-related improvements

$\overline{HSB}$ pin (Hardware STORE Busy Indication/Hardware STORE Initiation)

The $\overline{HSB}$ pin of the nvSRAM is an open-drain I/O pin (internal 100 kΩ weak pull-up resistor) used to indicate or initiate a STORE operation. When a STORE operation is in progress, nvSRAM pulls the $\overline{HSB}$ pin LOW to indicate that the device is busy and cannot be accessed for read/write operation. During normal operation, the $\overline{HSB}$ pin can be pulled LOW to initiate a Hardware STORE operation.

As shown in **Table 4**, several timing parameters related to the $\overline{HSB}$ pin input and output have changed from STK14C88 to STK14C88C. All of these changes are improvements from the original part specification and should be considered as added benefits in your system while migrating to the new part number.

4.1.1 T_{DELAY}

If a write latch is set and the $\overline{HSB}$ pin is pulled LOW, STK14C88 enables 1-µs time for write operations to complete before STORE operation begins and reads and writes are inhibited. This potentially enables inadvertent data to be written to the nvSRAM during the t_{DELAY} duration.

Note: *Write Latch: When a write operation is done, a 'write latch' is set internally. When $\overline{HSB}$ is pulled LOW, nvSRAM checks this write latch before initiating a STORE. This is done to prevent any unnecessary loss of endurance cycles.*

In STK14C88C, the t_{DELAY} parameter enables only one write cycle time for any ongoing write to complete after $\overline{HSB}$ pin is pulled LOW. This improvement provides better security from inadvertent write operations.

Also, if $\overline{HSB}$ pin is pulled LOW externally for a minimum of t_{PHSB} time on STK14C88C, the output driver of $\overline{HSB}$ pin pulls the pin LOW only indicating a STORE operation within 25 ns (t_{DELAY}). This parameter for $\overline{HSB}$ low to STORE busy is not specified in STK14C88. (See **Figure 1** and **Figure 2**).

$\overline{HSB}$ LOW when write latch not set:

If no writes are performed since the last STORE/RECALL operation, STORE operation does not start when $\overline{HSB}$ is pulled LOW. However, the $\overline{HSB}$ pin is still internally pulled LOW for 1 µs (t_{DELAY}) time in STK14C88.

STK14C88C does not pull the $\overline{HSB}$ pin LOW internally if write latch is not set. This improvement prevents the possibility of being in an infinite loop when $\overline{HSB}$ pins of two nvSRAM devices are ganged.

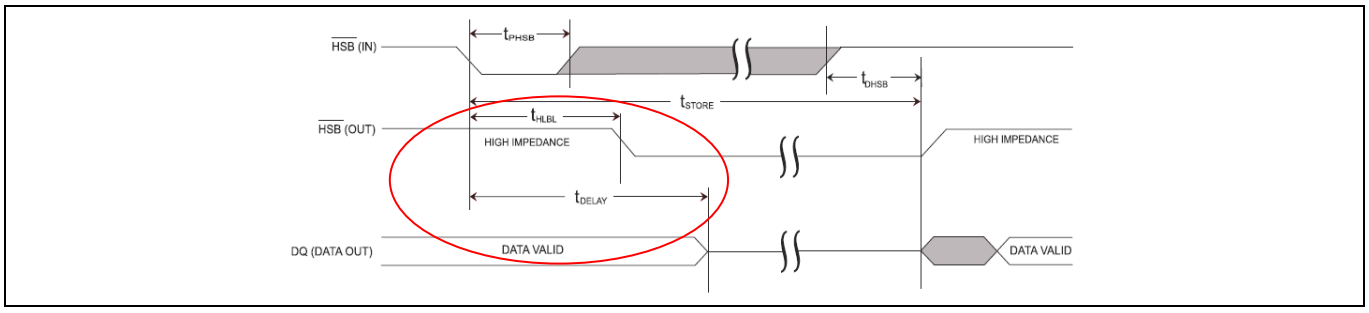

Figure 1 STK14C88: AC parameters related to $\overline{HSB}$

Details of improvement

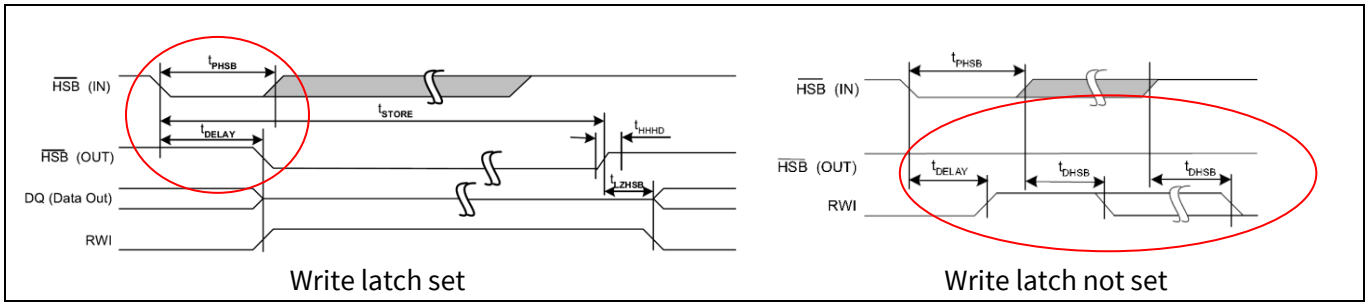

Figure 2 STK14C88C: AC parameters related to $\overline{HSB}$

4.2 Power-up recall related improvements

Additional parameters are specified in STK14C88C such as $\overline{HSB}$ Output Disable Voltage (V_{HDIS}), $\overline{HSB}$ To Output Active Time (t_{LZHSB}), and $\overline{HSB}$ High Active Time (t_{HHHD}), which helps in system design. See **Figure 3** and **Figure 4** for the definition of the additional specs in power-up. Also, note that $\overline{HSB}$ remains LOW until the end of the power-up in the new part. This would guard against the system inadvertently thinking the part has completed the boot up prior to real completion.

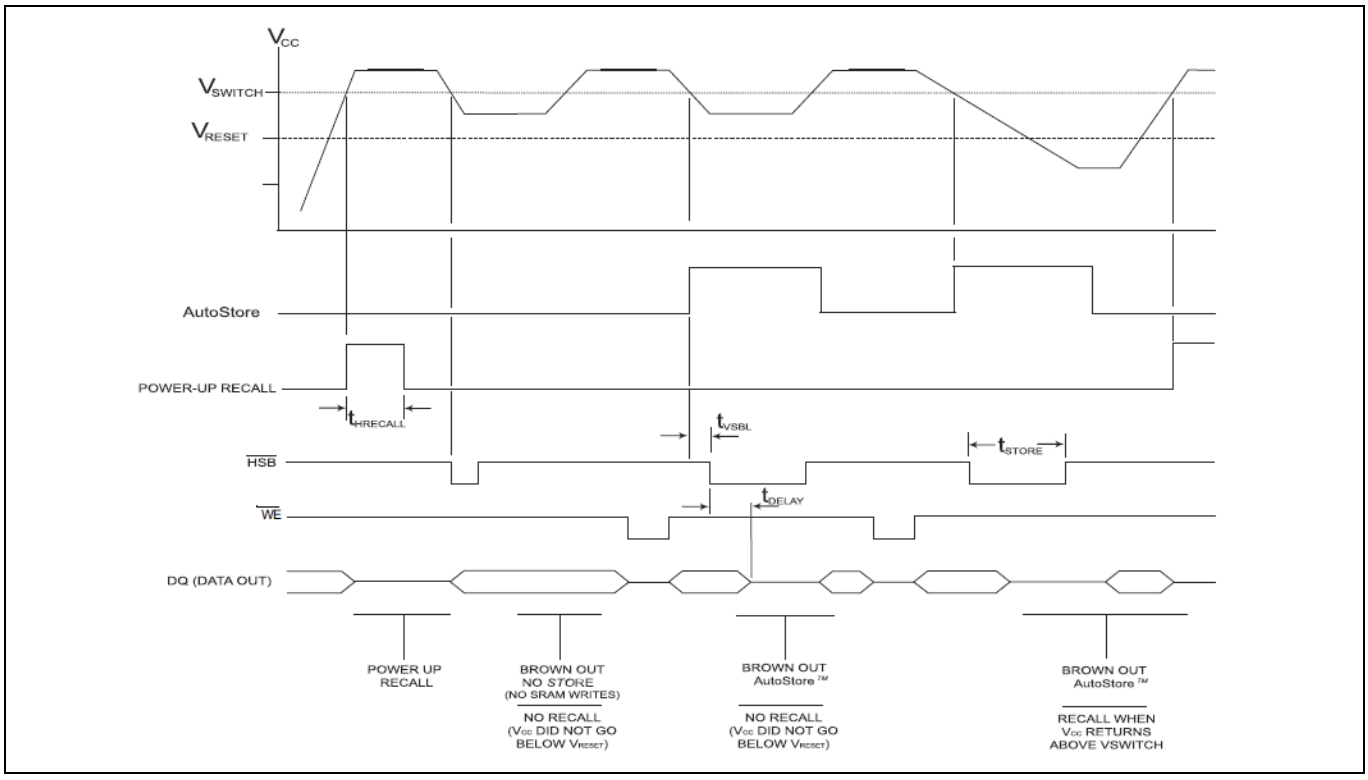

Figure 3 STK14C88: Power-up recall

Details of improvement

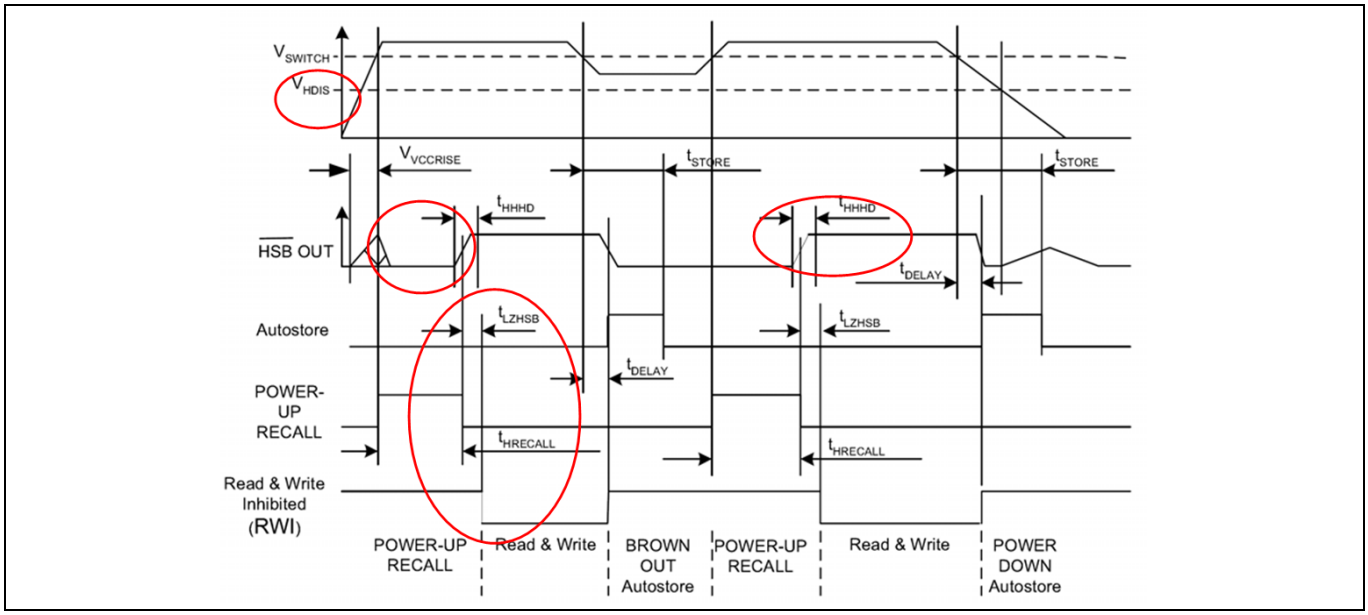

Figure 4 STK14C88C: Power-up recall

5 Summary

The application note discusses the differences between STK14C88C in the latest 0.13-micron technology and STK14C88 in the 0.8-micron technology. Several parameters related to $\overline{HSB}$ and power-up have improved / specified in the new device enabling faster device response, greater data security, and ease of design. STK14C88C is pin compatible with and can replace STK14C88 with minimum changes hardware/firmware in most applications. Applications where STK14C88 is in AutoStore inhibit mode would require layout changes, and also, it is not possible to prevent STORE on the fly in STK14C88C. The value of V_{CAP} in the existing design needs to be considered while replacing the part.

References

[1] Datasheets

- **STK14C88: 256-Kbit (32 K × 8) AutoStore nvSRAM datasheet**
- **STK14C88C: 256-Kbit (32 K × 8) nvSRAM datasheet**

Revision history

Document version	Date of release	Description of changes
**	2018-06-21	Initial release
*A	2022-03-17	Updated to Infineon template

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