Design Guidelines for Power Systems for Traveo Family MCUs with Multiple Power-Supplies

About this document

Scope and purpose

AN223252 explains the important points in designing a power management system using Cypress' Power management IC (PMICs) and Traveo™ family MCUs, and provides examples.

Associated Part Family

S6BP501A, S6BP502A

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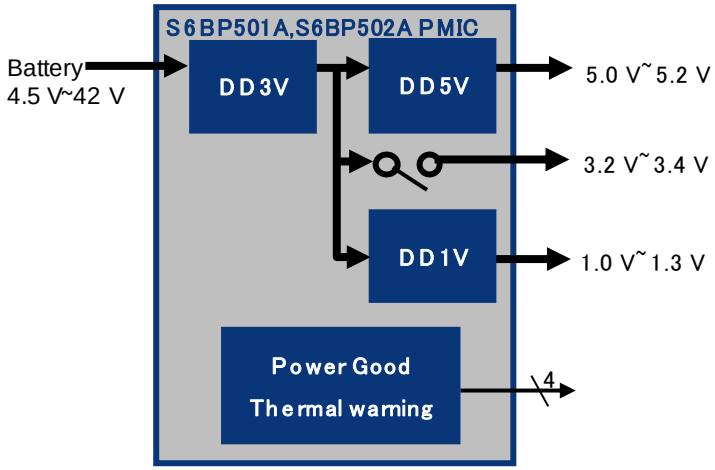
1 Introduction

This application note describes the important points and some examples to design a power management system with S6BP501A or S6BP502A and Traveo MCUs (S6J3200 series, S6J32E, S6J32F, S6J32G series or S6J3310 series, S6J3320, S6J3330, S6J3340 series, S6J3350 series). Traveo MCUs can be used for the automotive cluster, and require multiple power supplies. Cypress' S6BP501A and S6BP502A PMICs are suitable for cluster solutions with Traveo MCUs because they can supply three power lines.

S6BP501A and S6BP502A have three-channel output: one high-voltage buck DC/DC controller (DD3V), one buck DC/DC converter with built-in FETs (DD1V), and one boost DC/DC converter with built-in FETs (DD5V), as shown in **Figure 1**.



*Power good and thermal warning are function names of the PMIC (see the **datasheet**)

Figure 1 Power management system block diagram

Each output voltage can be set by an external resistor. DD3V, which is the primary buck converter, outputs 3.3 V from the 12 V battery voltage. DD5V and DD1V are secondary converters that output 5 V and 1.2 V (or 1.15 V) from 3.3 V. Therefore, in S6BP501A and S6BP502A, the 5-V rail keeps the output voltage level without voltage drop even if the battery voltage becomes 5 V or less. In principle, the levels of 5 V, 3.3 V, and 1.2 V are kept when the power supply voltage from the battery is 3.3 V or higher. To be precise, the minimum required power supply voltage for keeping the 3.3-V output voltage is slightly higher than 3.3 V, because the voltage drops due to the ON resistance of the switching FET of DD3V and the DC resistance of the inductor. For details, see Section 2.3.5. Switching FET (SWFET) of **AN99435**.

2 Traveo MCU and PMIC combinations

Table 1 shows optimized combinations of Traveo MCU and PMIC.

Table 1 Combination of Traveo MCU and Cypress PMIC

Traveo MCU	PMIC
S6J3310 series, S6J3320, S6J3330, S6J3340 series, S6J3350 series (Core voltage: 1.15 V)	S6BP501A 5 V / 1.3 A, 3.3 V / 1.6 A, 1.15 V / 1.4 A
S6J3200 series, S6J32E, S6J32F, S6J32G series (Core voltage: 1.20 V)	S6BP502A 5 V / 1.3 A, 3.3 V / 1.9 A, 1.20 V / 2.0 A

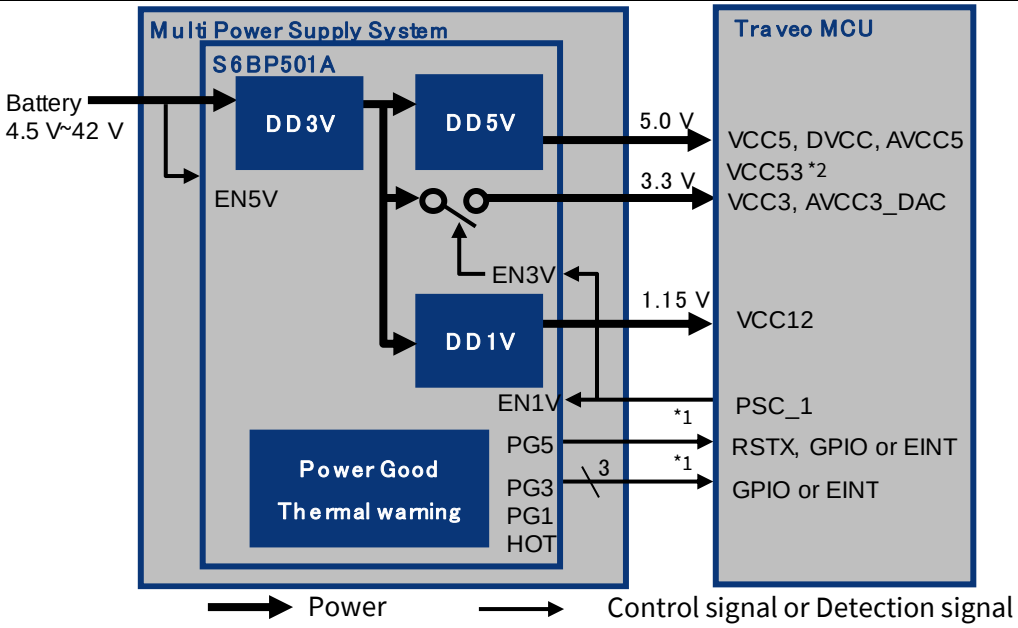
3 Power sequence of Traveo MCU with Cypress PMIC

The power sequence of the Traveo MCU should comply with the power supply sequence: see the “Operation Assurance Condition” or “Recommended Operating Condition” sections in the MCU **datasheet**. The required power sequence is different based on whether it uses Low Voltage Differential Signaling (LVDS).

3.1 Traveo MCU without LVDS

3.1.1 Connection example

Figure 2 and **Figure 3** show the connection between the PMIC and Traveo MCU if the MCU does not use the LVDS function.

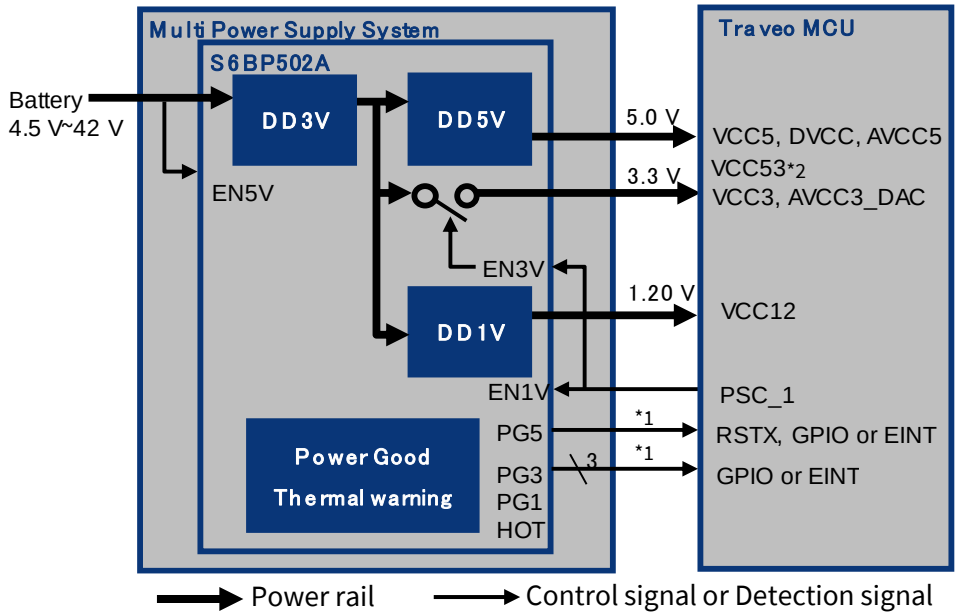


*: EN5V, EN3V, EN1V, PG5, PG3, PG1, and HOT are terminals of the PMIC. See the PMIC **datasheet** for more information. VCC5, DVCC, AVCC5, VCC53, VCC3, AVCC3_DAC, VCC12, PSC_1, RSTX, GPIO, and EINT are terminals of the MCU. See the Traveo MCU **datasheet** for more information.

*1: PG5, PG3, PG1, and HOT are optional connections. These signals can be used as warning detection or reset trigger.

*2: Connect VCC53 to 5.0 V or 3.3 V.

Figure 2 Connection between S6J3310 (or S6J3320, S6J3330, S6J3340, S6J3350) and S6BP501A



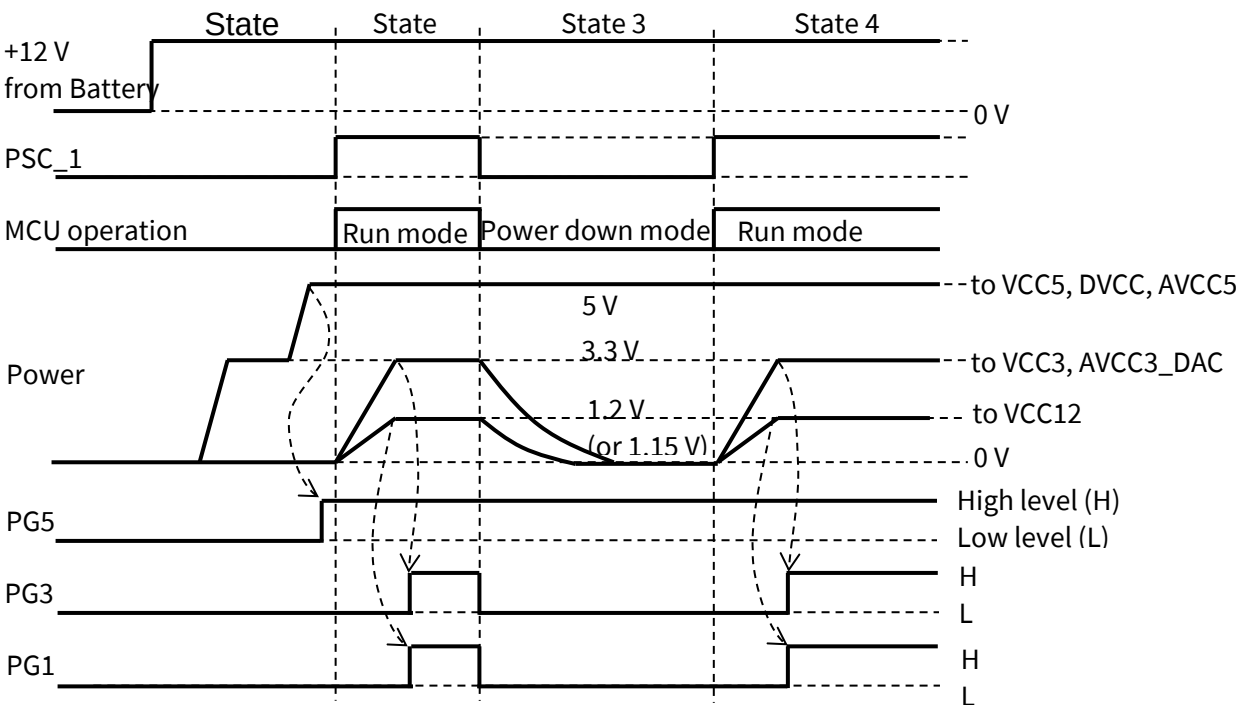
*1: PG5, PG3, PG1, and HOT connections are optional. These signals can be used as warning detection or reset trigger.

*2: Connect VCC53 to 5.0 V or 3.0 V.

Figure 3 Connection example between S6J3200 (or S6J32E, S6J32F, S6J32G) without LVDS and S6BP502A

3.1.2 Power sequence example

Figure 4 shows the startup sequence of an MCU which wakes up after being powered by a battery.



"Run mode" and "Power down mode" is Traveo MCU's function. Please refer **AN220338** for more information.

Figure 4 Instrument cluster system

State 1: Power on sequence with battery. The PMIC starts supplying 5 V. The 5-V rail rises with a rising slope controlled by the DD3V and DD5V soft start function. PG5 outputs H when the 5-V rail becomes higher than the PG5 release voltage.

State 2: The MCU starts the control logic and sets the PSC_1 pin to H. The 3.3-V and 1.2-V (or 1.15-V) rails rise with the rising slope controlled respectively by VOUT3V and DD1V soft start functions. PG3 and PG1 output H when the 3.3-V and 1.2-V (or 1.15-V) rails become higher than PG3 and PG1 release voltages respectively. The MCU starts the run mode.

State 3: The MCU starts the power down mode and sets the PSC_1 pin to L. The 3.3-V and 1.2-V (1.15-V) rails stop, and the PMIC sets PG3 and PG1 to L. In addition, the 3.3-V and 1.2-V (or 1.15-V) rails are discharged with the built-in 400 Ω (typ.) discharge resistor.

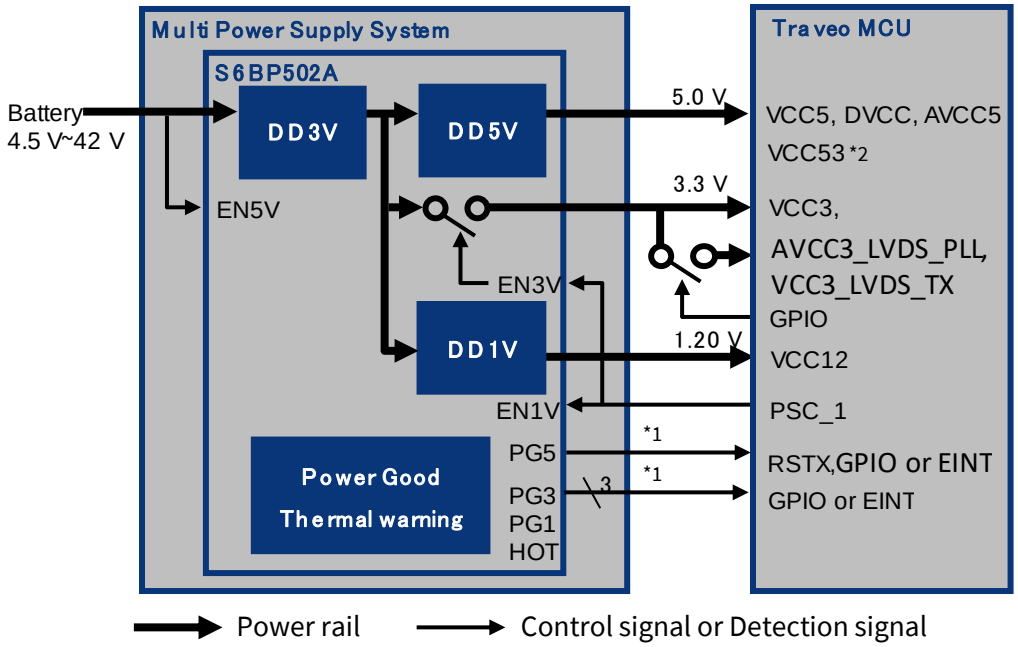
State 4: The MCU starts run mode and sets the PSC_1 pin to H. The 3.3-V and 1.2-V (or 1.15-V) rails rise again with the rising slope controlled by the soft start functions of VOUT3V and DD1V respectively. PG3 and PG1 output H, when the 3.3-V and 1.2-V (or 1.15-V) rails become higher than PG3 and PG1 release voltages respectively.

See **AN220338** for detailed notes on the transition to the power down mode of the MCU. Contact Cypress **Technical Support** if your design does not meet this requirement.

3.2 Traveo MCU with LVDS function

3.2.1 Connection example

Figure 5 shows the connection between PMIC and Traveo MCU if the MCU uses the LVDS function.



*AVCC3_LVDS_PLL and VCC3_LVDS_TX are terminals of MCU. See Traveo MCU **datasheet** for more information.

*1: PG5, PG3, PG1, and HOT connections are optional. These signals can be used as warning detection or reset trigger.

*2: Connect VCC53 to 5.0 V or 3.0 V.

Figure 5 Connection example between Traveo MCU with LVDS and S6BP502A

3.2.2 Power sequence example

Figure 6 shows the startup sequence of an MCU which wakes up after powered by a battery.

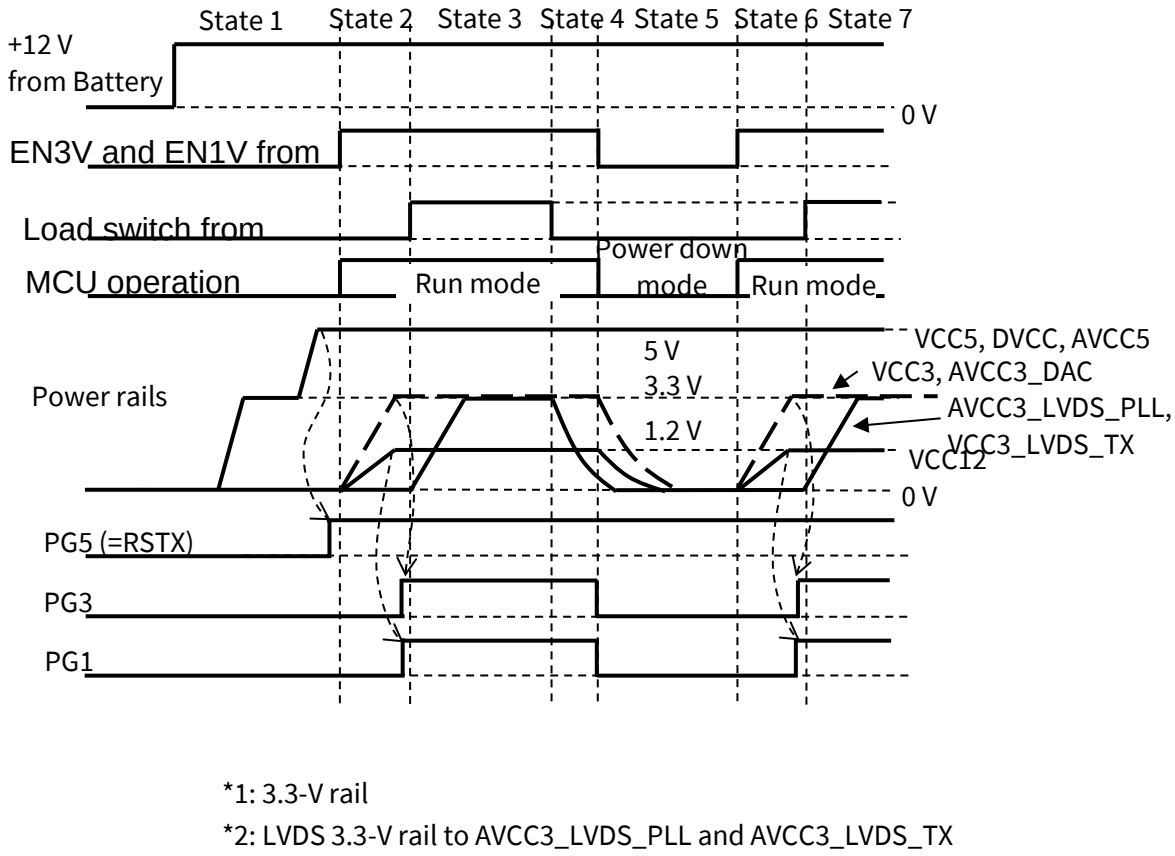


Figure 6 Timing chart of startup

State 1: Power on sequence with battery. The PMIC starts supplying 5 V. The 5-V rail rises with the rising slope controlled by the DD3V and DD5V soft start functions. PG5 outputs H when the 5-V rail becomes higher than the PG5 release voltage.

State 2: The MCU starts the control logic and sets the PSC_1 pin to H. The 3.3-V and 1.2-V rails rise with the rising slope controlled respectively by the VOUT3V and DD1V soft start functions. PG3 and PG1 output H when the 3.3-V and 1.2-V rails become higher than PG3 and PG1 release voltages respectively. The MCU starts run mode.

State 3: The MCU sets the load switch to the ON state to supply the LVDS 3.3-V rail either when the MCU detects that PG1 has changed to H, or after the DD1V soft start.

State 4: The MCU sets the load switch to the OFF state to stop the LVDS 3.3-V rail.

State 5: The MCU starts the power down mode and sets the PSC_1 pin to L. The 3.3-V and 1.2-V rails stop; PG3 and PG1 changes from H to L. The 3.3-V rail and 1.2-V rails are discharged due to the built-in 400 Ω (typ.) discharge resistor.

State 6: The MCU starts run mode and sets the PSC_1 pin to H. The 3.3-V and 1.2-V rails rise again with the rising slope controlled respectively by the VOUT3V and DD1V soft start functions. PG3 and PG1 output H when the 3.3-V and 1.2-V rails become higher than PG3 and PG1 release voltages respectively. The MCU starts run mode again.

State 7: The MCU sets the load switch to the ON state to supply the LVDS 3.3-V rail again either when MCU detects that PG1 has changed to H, or after the DD1V soft start.

See **AN220338** for detailed notes on the transition to the power down mode of the MCU. Contact Cypress **Technical Support** if your design does not meet this requirement.

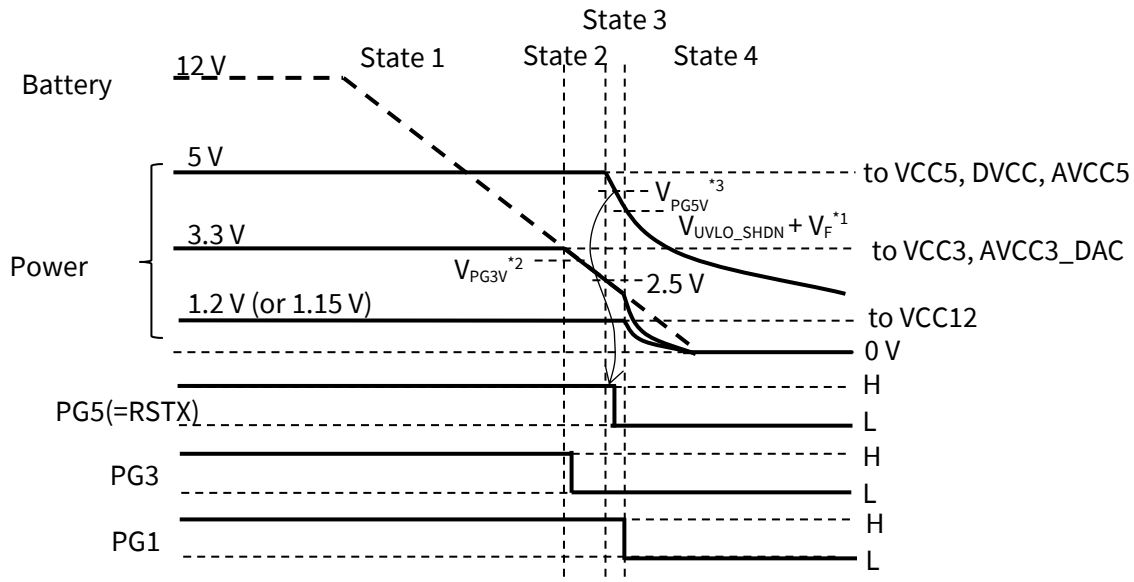
4 Shutdown sequence while battery voltage is dropping

In S6BP501A and S6BP502A, DD3V, which is the primary buck converter, outputs 3.3 V from the 12 V battery voltage; DD5V and DD1V, which are secondary converters, output 5 V and 1.2 V (or 1.15 V) from 3.3 V. For this reason, the 3.3 V rail drops when the battery voltage falls below 3.3 V in principle.

Note that the voltage drops from the 3.3-V rail first in S6BP501A and S6BP502A, in contrast to the voltage dropping from the 5-V rail first in a normal power supply configuration that outputs 5 V from 12 V and outputs 1.2 V or 3.3 V from the 5-V rail.

4.1 Shutdown sequence example

Figure 7 shows the timing chart when the power supply voltage drops from 12 V to less than 3.3 V.



*1: V_{UVLO_SHDN} is the UVLO detection voltage of the PMIC. V_F is the forward voltage of the regenerative Schottky barrier diode (SBD) that is connected between the VOUT5 terminal and the VB terminal of the PMIC.
*2: V_{PG3V} is the undervoltage detection (UVD) voltage, V_{UVDF_PG3V}, of PG3V pin.
*3: V_{PG5V} is converted UVD voltage, V_{UVDF_PG5V}, of PG5V pin from FB5V to VOUT5V.
See the PMIC **datasheet** and **AN99435** for more information.

Figure 7 Timing chart of drop battery power sequence in Run mode

State 1: 5 V, 3.3 V, and 1.2 V (or 1.15 V) power rails keep the output voltage level until the battery voltage drops below 3.3 V.

State 2: When the battery voltage falls below 3.3 V, the voltage of the 3.3-V rail decreases. When the PMIC detects UVD of the 3.3-V output, PG 3 is set to L.

State 3: Because the Max Duty of DD 5 V is 50%, when the DD 3 V output becomes 2.5 V or less, the 5 V rail also decreases. When the PMIC detects UVD of 5 V, PG 5 is set to L.

State 4: The VB voltage of the PMIC also drops with the 5-V rail drop and detects UVLO. The PMIC stops the power supply of the 3-ch power rail, sets all Power Goods to L. In addition, the 3.3-V and 1.2-V rails are discharged by the built-in 400-Ω (typ.) discharge resistor. The 5-V rail does not have the discharge function, so the bypass capacitor of the 5-V rail (including the DD5V output capacitor) is discharged by the load current.

*UVD is the detection function of the PMIC. See the PMIC **datasheet** for more information.

In the battery power drop sequence, in which such a 5-V power rail decreases, the following requirement of the Traveo MCU must be satisfied.

- “Power and reset Sequence” requirements in the **datasheet** of S6J3310, S6J3320, S6J3330, S6J3340 series, and S6J3350 series
- “LVDH1” requirements in the **datasheet** of S6J3200, series, and S6J32E, S6J32F, S6J32G series

See the Traveo MCU **datasheet** for more information.

4.2 Shutdown routine example

If your design does not satisfy the Traveo MCU requirements, consider the following sequence with the connection of PG3 and EINT/GPIO in **Figure 2**, **Figure 3**, or **Figure 5**.

1. PMIC detects UVD of the 3.3-V rail and PG3 drops to L.
2. MCU detects the PG3 drop through EINT/GPIO and starts the shutdown routine, which sets PSC_1 from H to L.

The sequence should be finished within the following $t_{5V\_sustain}$ time for safe recovery of the MCU.

Equation 1

$$t_{5V\_sustain} = \frac{(V_{UVDF\_PG3V} - 2.5) \times C_{IN}}{I_{IN}}$$

Where:

$t_{5V\_sustain}$: Time interval from PG3 going L to LVDH1 detection of the 5-V rail (s)

V_{UVDF_PG3V}: UVD voltage (3.004 V min)

C_{IN}: 12-V rail bypass capacitor (F). This should be inserted between the PMIC and reverse current protection diode if it exists.

I_{IN}: Input current from the battery when the PMIC input voltage drops below 3.3 V (A)

Shutdown sequence while battery voltage is dropping

See the following example calculation:

Conditions:

C_{IN}: 1 mF (Including pi-filter after the rectifier to prevent backflow to the battery)

I_{IN}: 50 mA (e.g., MCU is the run mode but backlight/illumination/gauges turn off because the cluster transits from full-function mode to limited function mode when the battery voltage drops below 6 V)

$$t_{5V\_sustain} = \frac{(3.004\,V - 2.5) \times 1\,mF}{50\,mA} = 10\,ms$$

In this example, the MCU must complete the shutdown sequence within 10 ms. Contact Cypress **Technical Support** if your design does not meet these requirements.

5 Related documents

5.1 Application notes

5.1.1 For Traveo MCU

- AN220338 – Traveo Family MCUs: Scenarios of Intended Power Cycles
- AN220401 – Power Supply Drop Above VCC min and Supply Monitor Detection Level
- AN220402 – Traveo Family MCUs: Power Supply Drop Below Min Supply Voltage but above Vreset
- AN220973 – Traveo Family MCUs: System Safe Recovery when Power Supply Drops below Vreset

5.1.2 For PMIC

- AN99435 – Designing a Power Management System with S6BP501A and S6BP502A

5.2 Datasheets

5.2.1 For Traveo MCU

- S6J3310 Series/S6J3320 Series/S6J3330 Series/S6J3340 Series, 32-bit Microcontroller Traveo™ Family
- S6J3350 Series, 32-bit Microcontroller Traveo™ Family
- S6J3200 Series, 32-bit Microcontroller Traveo™ Family
- S6J32E/S6J32F/S6J32G Series, 32-Bit Microcontroller Traveo™

5.2.2 For PMIC

- S6BP501A/S6BP502A, 3ch DC/DC Converter IC for Automotive Cluster

Revision history

Document version	Date of release	Description of changes
**	2018-07-23	New application note.
*A	2021-06-15	Updated to Infineon template. Completing Sunset Review.

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