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EZ-USB HX3PD Hardware Design Guidelines and Checklist

Authors: Hena Thampy, Vetrivel Prakasam

Associated Part Family: CYUSB4347, CYUSB4357

This application note provides the hardware design and PCB layout guidelines for EZ-USB® HX3PD, a high-performance USB 3.1 Gen 2 (10 Gbps) Type-C Hub with Power Delivery capability. These guidelines help to ensure best performance with respect to signal integrity and full electrical compliance with the USB 3.1 Gen 2 Specification. A schematics and layout review checklist is provided in the end, which consolidates all the important points to be considered while designing with HX3PD.

Contents

1 Introduction

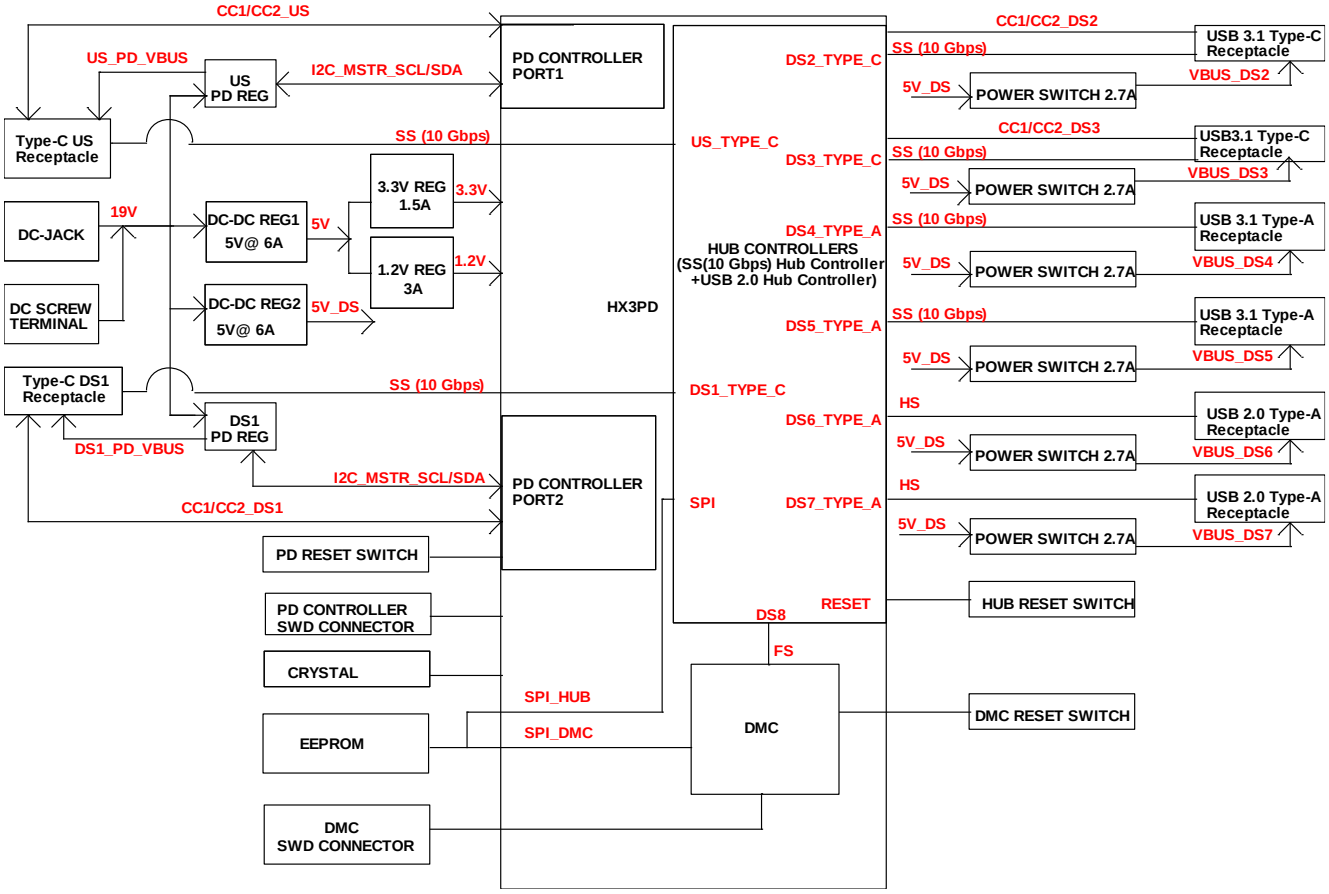
EZ-USB HX3PD is a 7-port USB 3.1 Gen 2 (10 Gbps) Type-C Hub with Power Delivery (PD) capability, recommended for applications such as standalone PD Hub, notebook PC docks, monitor docks, and dongle applications. It is a one-chip solution, integrating a USB 3.1 Gen 2 (10 Gbps) Hub, two-port PD Controller, and a Dock Management Controller (DMC). HX3PD expands a single upstream (US) Type-C PD port into multiple downstream (DS) ports. It supports SuperSpeed (SS) USB 10 Gbps, SuperSpeed USB, Hi-Speed (HS), Full Speed (FS), and Low-Speed (LS) functionality. In addition, it provides a complete Type-C and USB PD Port Controller solution in the US and one DS port. HX3PD consists of SPI interface, Serial communication block, and GPIOs.

Figure 1 shows an HX3PD reference design block diagram. Significant features of HX3PD are:

- **Upstream**: Type-C, PD, and SuperSpeed USB 10 Gbps port
- **Downstream**:
  - DS1: Type-C, PD, and SuperSpeed USB 10 Gbps port
  - DS2 and DS3: Type-C, non-PD, SuperSpeed USB 10 Gbps ports
  - DS4 and DS5: Type-A SuperSpeed USB 10 Gbps ports
  - DS6 and DS7: Type-A USB 2.0 ports
- **Hub Controllers:** HX3PD consists of two Hub Controllers: a SuperSpeed USB 10 Gbps Hub Controller and a USB 2.0 Hub Controller. The former supports SuperSpeed USB 10 Gbps Hub functionalities such as full-duplex data transmission and link power management (U0, U1, U2, and U3 states). The USB 2.0 Hub Controller supports LS, FS, and HS functionalities such as multiple transaction translators (TTs) and USB 2.0 link power management (L0, L1, L2, and L3 states).

- **PD Controller:** HX3PD has a two-port PD Controller for controlling two PD ports. The two PD ports can be US and a DS port, or two DS ports. The PD Controller integrates the termination resistors required to identify the role of Type-C PD ports. Cypress reference design supports PD on US and DS1 port. To configure the PD support for other ports, the hardware needs to be changed and a customized firmware should be used. Contact Cypress Technical Support for more details.
- **Dock Management Controller:** The Dock Management Controller (DMC) includes a USB Billboard Controller and it manages signed/unsigned firmware download over USB to programmable peripherals interfaced to HX3PD.
- **Charging Standard support:** USB Power Delivery 3.0 (PD 3.0) is supported on US and DS1 ports; Battery Charging v1.2 (BC v1.2), and Apple Charging standards are supported on DS1 to DS7 ports. By default, Apple Charging is disabled on DS1 port. Contact Cypress Technical Support to get the firmware that supports BC v.12 and Apple Charging on DS1.
- **Ghost Charge™:** Enables charging of devices connected to DS ports when no Host is connected on the US port

Figure 1. EZ-USB HX3PD Reference Design Block Diagram



HX3PD is available in two part numbers, CYUSB4347 and CYUSB4357 in 192-BGA packages: CYUSB4357 supports signed firmware upgrade whereas CYUSB4347 does not. Cypress DMC on CYUSB4357 uses RSA-2048/SHA-256 signing to qualify firmware update to individual controllers in the dock system. Both parts have the same hardware blocks and power domains, and therefore the hardware design guidelines and checklist provided in this document are applicable for both. For more information on the product options, see the EZ-USB HX3PD datasheet or contact your local sales representative.

2 Schematic Design Requirements

This section explains the schematic design requirements and considerations for an HX3PD based system. See the reference design that is used as the base for the recommendations on the EZ-USB HX3PD USB 3.1 Gen 2 Hub webpage.

2.1 Power System

HX3PD operates with two power supplies: 3.3 V and 1.2 V. In addition, a 1-V supply is generated internally from the 1.2-V supply. In the reference design, two DC/DC converters are used to generate 5-V output from a 19-V input. One of the 5-V outputs is provided to six DS ports (DS2 to DS7 ports). The other 5-V supply is used to generate the 3.3-V and 1.2-V power supplies. It is also provided to the V5P0_P0, V5P0_P1, and V5P0 pins. The V5P0_P0 and V5P0_P1 pins are used by the US and DS1 ports respectively, which are designed as Type-C PD ports in the reference design. The V5P0 pin is used by DS2 and DS3 ports, which are designed as Type-C only ports in the reference design. If US and DS1 are designed as Type-A ports, the 5-V supply is not required to be provided to the V5P0_P0/P1 pins. However, if DS2 and DS3 ports are designed as Type-A ports, 5 V should still be supplied to the V5P0 pin.

In the HX3PD reference design, US and DS1 ports are PD ports, designed to support Power Delivery Objects (PDOs) of 5 V, 9 V, 15 V, and 20 V at 3 A maximum. Switching regulators are used to configure the various output voltages from the 19-V input. DS2 to DS7 ports are non-PD ports, which operate at 5 V. Figure 2 shows the power system design in the HX3PD reference design.

Figure 2. HX3PD Power System Design

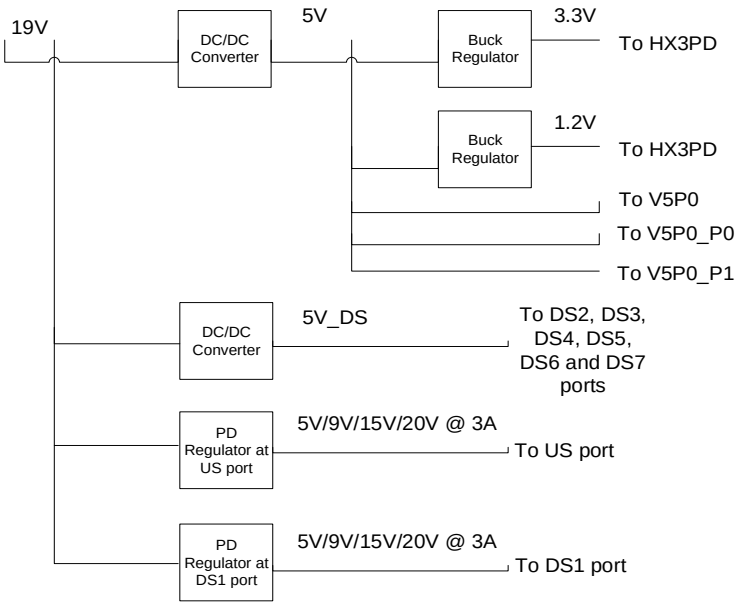


Table 1 lists the different power domains of HX3PD.

Table 1. HX3PD Power Domains

Power Domain	Description	Min	Typical	Max
V1P2	1.2-V supply to Hub	1.14 V	1.2 V	1.26 V
VDD10 (AVDD10/ DVDD10)	1.0-V core supply	0.95 V	1.0 V	1.05 V
V1P0_Px	1.0-V input for Port x	0.95 V	1.0 V	1.05 V
V1P0_PHY	1.0-V for USB 3.1 PHY	0.95 V	1.0 V	1.05 V
V1P0_MEM_A	1.0-V regulator output for internal memory A	–	1.0 V	–
V1P0_MEM_B	1.0-V regulator output for internal memory B	–	1.0 V	–

Power Domain	Description	Min	Typical	Max
V3P3	3.3-V supply for USB 2.0 PHY	3.0 V	3.3 V	3.6 V
V3P3_REG	3.3-V input to internal LDO	3.0 V	3.3 V	3.6 V
VDDIO	3.3-V I/O supply	3.0 V	3.3 V	3.6 V
VDDIO_DMC	3.3-V supply for DMC	3.0 V	3.3 V	3.6 V
VDDIO_PD	3.3-V supply for PD Controller	3.0 V	3.3 V	3.6 V
V5P0	5.0-V input supply	4.5 V	5.0 V	5.5 V
VCCD_DMC	1.8-V regulator output (DMC)	–	1.8 V	–
VCCD_PD	1.8-V regulator output (PD Controller)	–	1.8 V	–

Figure 3 shows the recommended power supply decoupling scheme.

Figure 3. Recommended Power Supply Decoupling Scheme

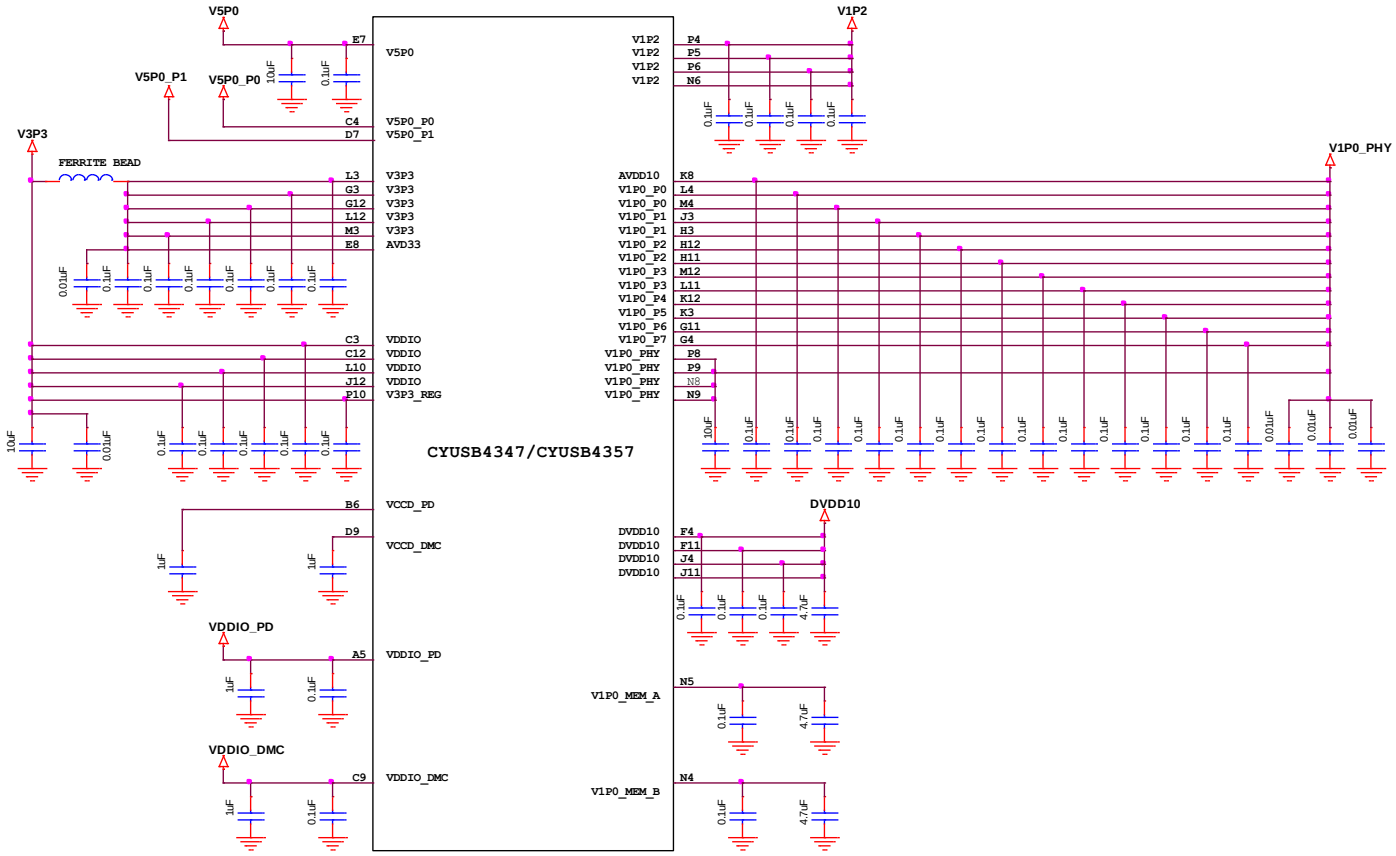


Table 2 lists the bulk capacitors that need to be connected for a group of power pins along with the decoupling capacitors.

Table 2. Decoupling and Bulk Capacitor Requirements

Power Domain (Pin Numbers)	Description	Bulk Capacitors	Decoupling Capacitors	Remarks
V1P2 (P4, P5, P6, N6)	1.2-V input supply for Hub	–	0.1 µF (4 decoupling capacitors used)	One decoupling capacitor per pin is required.
V1P0_Px (L4, M4, J3, H3, H12, H11, M12, L11, K12, K3, G11, G4)	1.0-V input for USB 3.1/USB 2.0 PHY for port x.	–	0.1 µF (12 decoupling capacitors used) and 0.01 µF (3 decoupling capacitors used)	One decoupling capacitor per pin is required. This domain should be connected to V1P0_PHY. The 0.01-µF capacitor helps to filter the high-frequency noise from the V1P0_PHY.
V1P0_PHY (P8, P9, N8, N9)	1.0-V regulator output for USB 3.1 PHY	10 µF	–	This is the regulator output pin and requires 10-µF bulk capacitor. Decoupling capacitors not required because the 0.1-µF capacitors connected on L11 and M12 pins (V1P0_P3) are close to V1P0_PHY. This helps to filter the high-frequency noise on this domain.
AVDD10 (K8)	1.0-V input for analog circuits	–	0.1 µF	One decoupling capacitor per pin is required. This domain should be connected to V1P0_PHY.
DVDD10 (F4, F11, J4, J11)	1.0-V regulator output for digital logic.	4.7 µF	0.1 µF (3 decoupling capacitors used)	Place the 4.7-µF capacitor very close to this domain's power plane. Place 0.1-µF decoupling capacitors close to any of the three pins.
V1P0_MEM_A (N5)	1.0-V regulator output for memory bank-A	4.7 µF	0.1 µF	Both bulk and decoupling capacitors must be placed very close to the pin.
V1P0_MEM_B (N4)	1.0-V regulator output for memory bank-B	4.7 µF	0.1 µF	Both capacitors must be placed close to the pin.
VDDIO_DMC (C9)	3.3-V input to DMC	1 µF	0.1 µF	Both capacitors must be placed close to the pin.
VDDIO_PD (A5)	3.3-V input to PD Controller	1 µF	0.1 µF	Both capacitors must be placed close to the pin.
VCCD_DMC (D9)	1.8-V regulator output (DMC)	1 µF	–	This is an internal regulator output pin and requires a 1-µF bulk capacitor. Place it close to the pin.
VCCD_PD (B6)	1.8-V regulator output (PD controller)	1 µF	–	This is an internal regulator output pin and requires a 1-µF bulk capacitor. Place it close to the pin.
VDDIO (C3, C12, L10, J12)	3.3-V input I/O supply to Hub	10 µF	0.1 µF (5 decoupling capacitors used), 0.01 µF	One decoupling capacitor per pin is required. The 10-µF bulk capacitor is for sourcing the current to these pins. This helps to filter the high-frequency noise from the V3P3_REG.
V3P3_REG (P10)	3.3-V input for internal LDO			
AVDD33 (E8)	3.3-V input supply for analog circuit in hub		0.1 µF (6 decoupling capacitors used), 0.01 µF	One decoupling capacitor per pin is required. The 10-µF bulk capacitor is for sourcing the current to these pins. helps to filter the high-frequency noise from the USB 2.0_PHY.
V3P3 (L3, G3, G12, L12, M3)	3.3-V input supply for USB 2.0			
V5P0 (E7)	5.0-V input supply for Type-C ports	10 µF	0.1 µF	Both capacitors must be placed very close to the pin.
V5P0_P0 (C4)	5.0-V input supply for Type-C ports	–	–	No decoupling capacitors required
V5P0_P1 (D7)	5.0-V input supply for Type-C ports	–	–	No decoupling capacitors required

Note: A ferrite bead is required to isolate VDDIO (3.3 V for GPIOs) from AVDD33 (3.3-V supply for the analog section) and V3P3 (3.3 V for USB 2.0 PHY), as shown in Figure 3. In the HX3PD reference design, a Bourns Inc. MH2029-100Y ferrite bead is used.

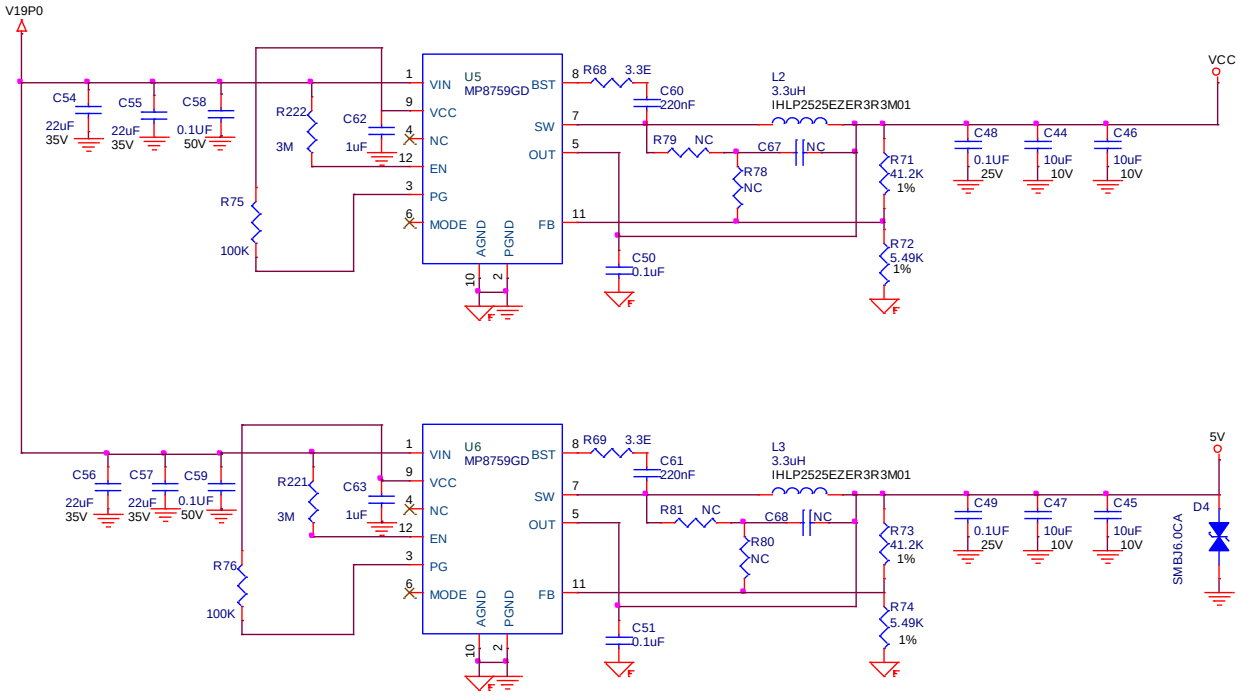
2.2 Power Regulators

2.2.1 5-V DC/DC Converters

For optimal functionality of an HX3PD based system, it is recommended to use an input power supply of 19 V with enough current capacity based on the charging requirements of all US and DS ports. For a 7-port HX3PD Hub design, two 5-V DC/DC converters are used for powering the 3.3-V and 1.2-V regulators and six DS ports. The reason for using two 5-V DC/DC converters in this design is to share the load on the 5-V rail. The first DC/DC converter sources power to the 3.3-V and 1.2-V regulators. The second DC/DC converter sources power to six DS ports. The US and DS1 ports are PD ports and are sourced from separate PD regulators which is explained later in this document.

Follow the DC/DC converter design and layout guidelines as per the respective manufacturer's datasheet especially on FB (Feedback), AGND (Analog Ground) and PGND (Power Ground). This is very important to have stable 5-V supply to generate the 3.3-V and 1.2-V supplies. Cypress uses MP8759GD 5-V DC/DC converters by Monolithic Power Systems, Inc. (MPS) in the HX3PD reference design. Follow the exact design recommendations from MPS as shown in Figure 4. For more information, refer to the MP8759GD datasheet. For a 4 DS port design, a single 5-V DC/DC converter is enough to power the 3.3-V and 1.2-V regulators and four DS ports.

Figure 4. 5-V DC/DC Converters



2.2.2 3.3-V and 1.2-V Regulators

HX3PD requires less than 30 mV of ripple on the 3.3-V and 1.2-V power rails. It is recommended to use a 1.2-V regulator that can support up to 3 A, and a 3.3-V regulator that can support up to 1.5 A.

Follow the regulator design and layout guidelines as per the respective manufacturer's datasheet especially on FB, AGND and PGND to ensure stable 3.3-V and 1.2-V supplies for HX3PD. Cypress uses the MP2162AGQH 3.3-V regulator and MP2130DG-LF-P 1.2-V regulator by Monolithic Power System (MPS) in the HX3PD reference design. Follow the exact design recommendations from MPS as in Figure 5 and Figure 6. For more information, refer to the corresponding datasheets.

Figure 5. 3.3-V Regulator

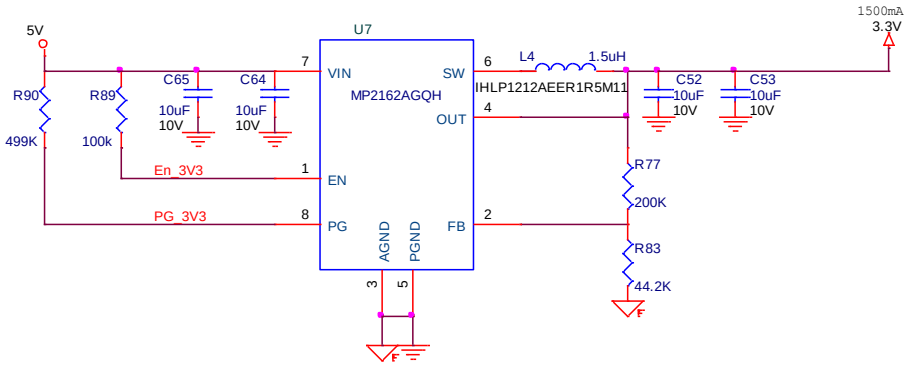
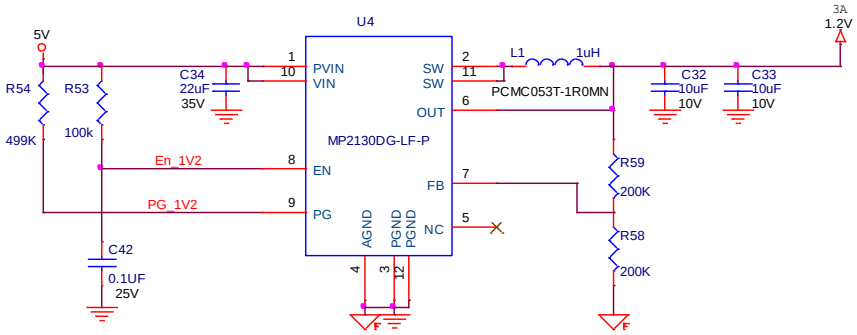


Figure 6. 1.2-V Regulator

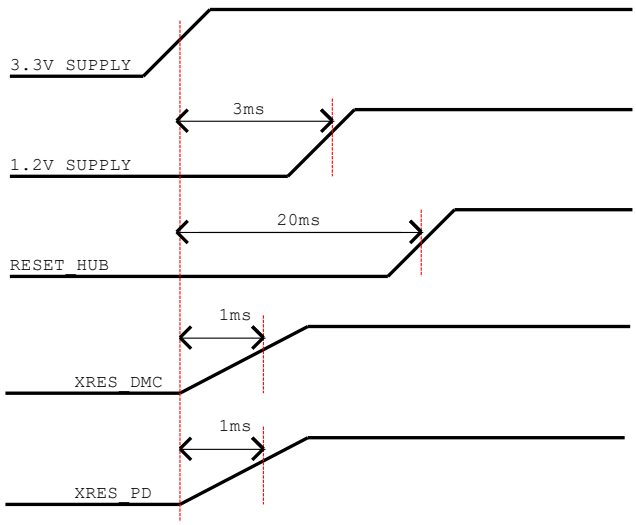


2.3 Power Sequencing

HX3PD operates with two power supplies: 3.3 V and 1.2 V. The power sequencing requirement between these voltage supplies must be strictly followed as shown in Figure 7. The 3.3-V supply must come up first, followed by the 1.2-V supply. Cypress recommends a time difference of 3 ms to 5 ms to take care of the supply voltage ramp-up time due to external circuits. To ensure this delay, the EN (Enable) pin of the 1.2-V regulator (Figure 6) is delayed with an RC circuit (R53 and C42); note that there is an internal pull up resistor in MP2130 (U4), delaying the 1.2-V regulator by 3-ms, together with R53 and C42.

Power sequencing of the reset signals is also shown in Figure 7. This is explained in detail in the Reset Circuit section.

Figure 7. Power and Reset Sequencing in HX3PD

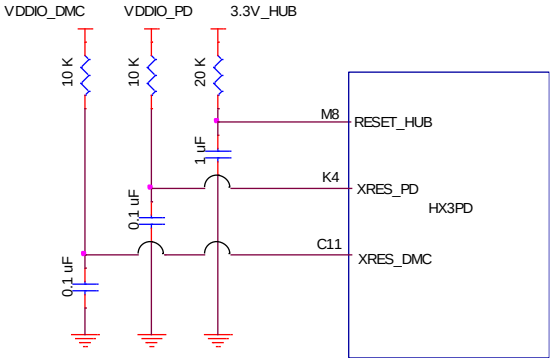


2.4 Reset Circuit

The RESET pin of the Hub Controller (RESET_HUB) should be kept asserted until the two power supplies i.e., 3.3 V and 1.2 V become stable. Also, the RESET pins of the DMC (XRES_DMC) and PD Controller (XRES_PD) should be held LOW until 3.3 V is stable. The time constants of the RESET pins are controlled through RC circuits, as can be seen in Figure 8.

Reset circuits of the Hub and that of the PD Controller and DMC work independently with different time constants. The reset circuit of the Hub is designed such that it provides a time delay of 20 ms (RC=20 kΩ × 1 µF) from when the 3.3-V supply becomes stable. This ensures that the Hub reset will be held LOW until both 3.3-V and 1.2-V power supplies are stable. For the PD Controller and DMC, reset circuits ensure that they are kept asserted for 1 ms (RC= 10 kΩ × 0.1 µF) after the 3.3-V supply is stable. A timing diagram of the reset signals is shown in Figure 7.

Figure 8. Reset Circuit of HX3PD



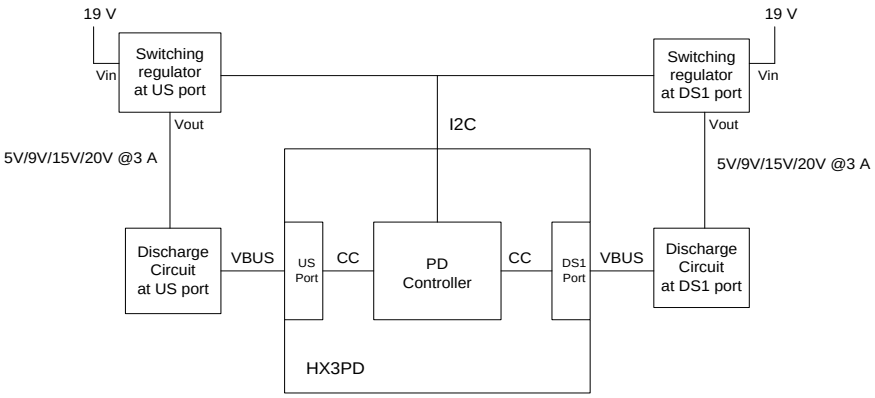
Note: The RC values used on the RESET pins ensure that sufficient time is provided for the supplies to ramp up and stabilize before the device is taken out of reset. In a system where the supply ramp up is slow, it is advisable and recommended to increase the value of capacitance to meet the timing specifications.

2.5 PD Regulators for US and DS1 Ports

The US and DS1 ports of HX3PD are PD ports i.e., they can establish power contract at voltages higher than 5 V. In the Cypress reference design, PD ports can support different Power Delivery Objects (PDOs) such as 5 V, 9 V, 15 V, and 20 V at 3 A maximum. Therefore, switching regulators are required to configure various output voltages from a single input voltage for these two PD ports.

A block diagram illustrating the working of PD regulator circuits for the US and DS1 ports is shown in Figure 9. The PD Controller monitors the Configuration Channel (CC) lines from the Type-C connector (US/DS1) to determine the voltage at which the power contract is to be made. It then communicates the required PDO to the corresponding regulator circuit through an I²C interface. The PD Controller acts as the I²C Master and the switching regulators at the US and DS1 ports are the I²C Slaves. Because it is a single-Master, two-Slave I²C interface, the switching regulators must have different Slave addresses. The Cypress reference design uses ON Semiconductor's NCP81239MNTXG (Slave address = 0x74) and NCP81239AMNTXG (Slave address = 0x75) as the switching regulators for the US and DS1 ports respectively.

Figure 9. PD Regulator Circuits for US and DS1 Ports



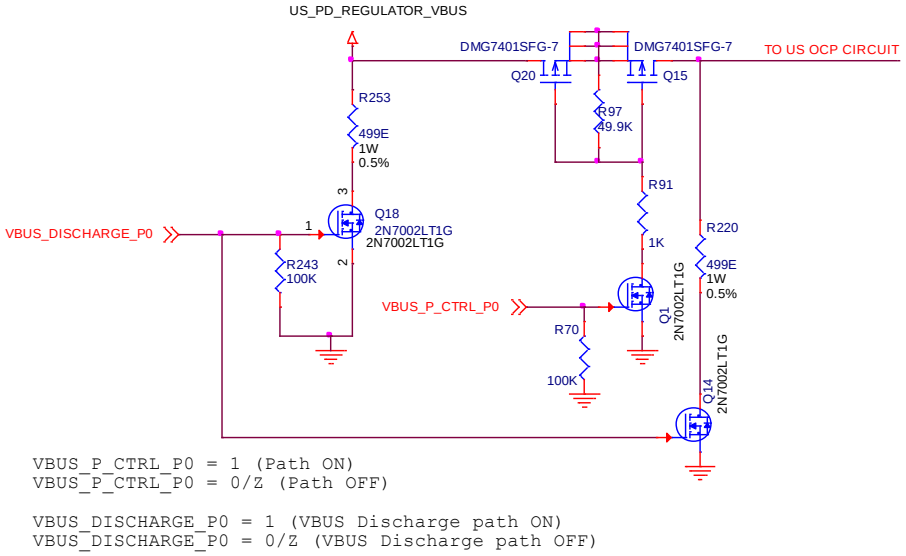
2.5.1 Discharge Circuit

If a power contract must be established at a voltage lower than the existing VBUS value, the existing VBUS would be discharged to the new VBUS value. Figure 10 shows the discharge circuit at the US port. VBUS_DISCHARGE_P0 is the GPIO controlling the discharge switch. When VBUS_DISCHARGE_P0 is HIGH, the n-MOSFETs provide discharging paths for VBUS. You must use power resistors (R220 and R253 in Figure 10) on the discharge paths to withstand and dissipate the large amounts of power, and to discharge VBUS within a very short time. Thus, the resistor value depends on the highest voltage that can be present on the capacitor at the output of the PD regulator circuit and the discharge time.

In the Cypress reference design, the discharge time is chosen as 75 ms, which is well within the USB PD spec requirement. The discharge time of 75 ms is derived from the RC circuit, where R (499 Ω) is the power resistor in the discharge path and C (150 µF) is the capacitor at the output of the PD regulator circuit. The voltage value at the output of the PD regulator can go up to 20 V. Therefore, the highest discharge current would be I = V/R = 20/499 = 0.04 A.

Now, the maximum power that needs to be dissipated is $P = I^2*R = 0.04^2*499 = 0.8$ W. In the HX3PD reference design, resistor with 1-W rating is chosen. Thus, 499-Ω, 1-W resistors are used in the discharge paths.

Figure 10. Discharge Circuit at US Port



VBUS_P_CTRL_P0 is the GPIO used for controlling the power switch of the US port. In Figure 10, Q1 represents the power switch for the US port. When VBUS_P_CTRL_P0 is HIGH, the power switch is ON, and thus VBUS is made available on the US port. If an overcurrent or a disconnection event happens, the PD Controller section of HX3PD drives VBUS_P_CTRL_P0 LOW, cutting off the VBUS supply path to the US port.

Note: A similar discharge circuit is implemented for the DS1 port.

2.6 Overcurrent Protection

The USB specification requires overcurrent protection (OCP) on all ports of the HX3PD Hub. Overcurrent protection on ports can be implemented in two modes: individual power switching mode or ganged power switching mode. In the individual power switching mode, each DS port power is controlled by independent power switches. The Hub turns OFF power to a specific DS port if the current drawn by that particular port exceeds the preset current limit. In the ganged power-switching mode, the power to all DS ports is controlled through a single power switch. In this mode, the Hub turns OFF power to all DS ports if the total current drawn by the DS ports exceeds the preset current limit. This is the case for non-PD DS ports. For a PD DS port, OCP is not implemented using power switches, but using separate overcurrent protection circuits. In the HX3PD reference design, the PGANG pin is pulled down by a 100-kΩ resistor to operate the non-PD DS ports in individual power switching mode.

The following sections explain the overcurrent protection implementation with respect to PD and non-PD ports.

2.6.1 OCP Implementation on Non-PD Ports (DS2 to DS7)

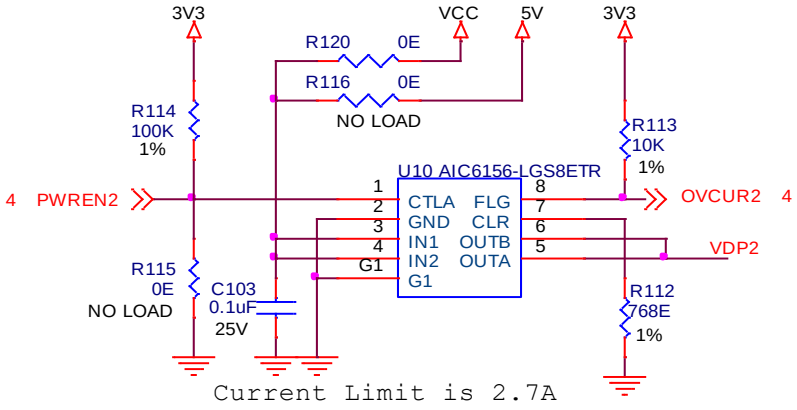
OCP is implemented on the non-PD ports (DS2 to DS7) using power switches. For the power switch, the current limit must be set based on the port configuration. For example, if a DS port is configured to support Battery Charging specification v1.2 only, the current limit of the power switch should be set as 1.5 A. If the port supports 2.4-A Apple charging, the power switch should be able to source up to 2.4 A. In HX3PD, DS ports 2 to 7 support both BC v1.2 and Apple charging standards. Therefore, to support both these charging standards, a current limit of 2.7 A is set for the power switches. In the Cypress reference design, AIC6156 power switch by Analog Integrations Corporation is used as shown in Figure 11.

The PWRENx (x=2 to 7 for DS2 to DS7 ports respectively) pins are used to control the external power switches and OVCURx is the overcurrent indicator input from the external power switches to the Hub Controller in the individual power switching mode.

Power switch schematic considerations:

- Since the power switches have open drain configuration, place a pull-up resistor on the overcurrent (OVCURx) output pins (FLG). The recommended value of the pull up resistor is 10 kΩ, as shown in Figure 11.
- A 100-kΩ pull-up resistor is required on the power enable (PWRENx) pin of the external power switch (CTLA). Because the CTLA pin is active LOW, a pull-up resistor is used.
- PWRENx can be configured as active HIGH or active LOW. For an active HIGH configuration, place a pull-down resistor on the pin. Use the 'EZ-USB HX3PD Configuration Utility' to configure the pin to either active HIGH or LOW. This utility will in turn launch another utility to open the hub configuration options; you can edit and save the configurations.

Figure 11. Power Switch Connection to HX3PD for DS2 Port



Note: OCP implementation on all non-PD ports i.e., DS2 to DS7 ports use a similar power switch implementation as shown in the above figure.

2.6.2 OCP Implementation on PD Ports (US and DS1)

In the HX3PD reference design, US and DS1 ports are PD ports i.e., they can establish power contract at voltages higher than 5 V. Cypress' reference design supports PDOs of 5 V, 9 V, 15 V, and 20 V with 3-A current capability. The input voltage to the power switches used at DS2 to DS7 ports cannot exceed 5.5 V. Therefore, separate overcurrent protection circuits are required at the PD ports. In the Cypress reference design, the current limit is set at 3.4 A at the US port because some PD enabled laptops sink up to 3.4 A of current. In order to keep the design uniform, a current limit of 3.4 A is set for the DS1 port also.

Figure 12 shows the overcurrent protection circuit implemented for the US port. Whenever the VBUS current goes above the predefined limit (3.4 A), the OCP circuit cuts off VBUS to the US port. A current-sensing circuit is implemented on the VBUS line. An opamp comparator is used at the final stage of the circuit to inform HX3PD whenever an overcurrent event happens. The power supplies to the opamp are 3.3 V and 0 V.

In the Cypress reference design, ZXCT1110 (U18 in Figure 12) by Diodes Incorporated is used as the high-side current-sensing monitor; this IC requires two external resistors R_{SENSE} and R_{GAIN}. Resistor value selection of R_{SENSE} is highly critical because it often involves a compromise between power efficiency and accuracy for the given temperature range. This resistor must be small enough to avoid excessive voltage drop between the power supply and the load. However, the resistor must be large enough to avoid excessive current measurement error, particularly random errors. In the reference design, a 25 mΩ current-sensing precision resistor R_{SENSE} (R247) is chosen to sense the current on the VBUS line.

In the event of a load short circuit or overload, a large proportion of the VBUS voltage may appear between the sense terminals. The ZXCT1100 current monitor is rated for a maximum sense voltage of +0.8 V. The resistor R249 protects the current monitor against load short circuit, the value of which is recommended by the manufacturer. This resistor, along with capacitor C168, makes up a low-pass filter to provide significant attenuation in the VHF and UHF regions. The value of C168 is recommended to be in the range of 10 pF to 47 pF.

The resistor R_{GAIN} (R246) converts the device (U18) output current to a voltage for convenient processing by the comparator (U16) as shown in this reference design. For U18, the output current I_{OUT} is defined through the nominal transconductance of 4 mA/V and is given by,

$I_{OUT} = 0.004 * V_{SENSE}$ (V_{SENSE} is the voltage across R_{SENSE})

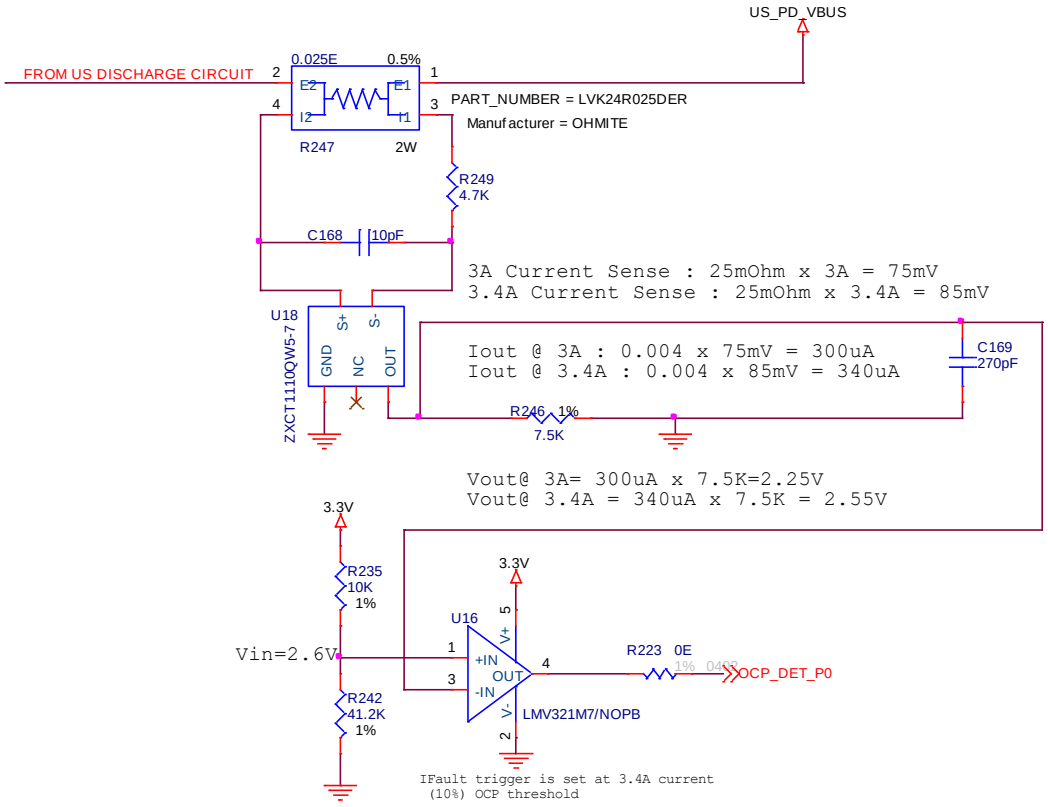
For the predefined current of 3.4 A on VBUS, the voltage at the inverting input terminal of the comparator (U16) would be,

$V_{(-IN)} = I_{OUT} * R_{GAIN} = (0.004* 25\ m\Omega * 3.4\ A) * 7.5\ k\Omega = 2.55\ V$

Accounting for comparator accuracy, charging device behavior, and other component tolerances, the reference voltage at the non-inverting input terminal of the opamp (+IN of U16) is set to 2.6 V to detect any current higher than 3.4 A. Whenever the VBUS current exceeds the set limit of 3.4 A, the voltage at the inverting terminal of the opamp goes higher than that of the non-inverting terminal. In this case, the opamp output goes to zero, i.e., the overcurrent protection input OCP_DET_P0 to HX3PD goes LOW indicating an overcurrent event. Now, the PD Controller section of HX3PD drives the VBUS_P_CTRL_P0 pin LOW to switch OFF the VBUS supply path (See Figure 10). This is already discussed in detail in the PD Regulator section.

A similar OCP circuit is implemented for DS1 port. For the DS1 port, the OCP_DET_P1 pin is used to indicate the overcurrent event to the PD Controller section of HX3PD. This signal is also connected to the OVCUR1 pin. The OVCUR1 pin provides overcurrent indication to the Hub Controller section. Therefore, an overcurrent event at the DS1 port is communicated to the PD Controller section and the Hub Controller section independently unlike other non-PD DS ports where an overcurrent event is communicated only to the Hub Controller section of HX3PD. Now, the Hub Controller indicates the OCP event to the host through the USB interface; the PD controller cuts off VBUS to the DS1 port. Later, when the host wants to re-power DS1 port, it notifies the Hub Controller, which in turn notifies the PD Controller. To enable communication between the Hub Controller and PD Controller, the PWREN1 pin (Power Enable pin of DS1 port) is connected to the PD Controller GPIO VCONN_MON_P1/PD_P27. Once the PD Controller receives the information, it turns ON the VBUS supply back.

Figure 12. Overcurrent Protection Circuit used at the US Port



Note: OCP implementation for DS1 port uses a similar circuit as shown in Figure 12.

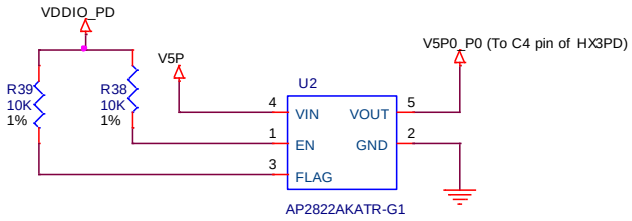
2.7 VCONN Implementation and OCP

VCONN is the 5-V supply that is used to power the integrated circuits within electronically marked Type-C cables (EMCA). These embedded electronics are required to process PD communication protocols.

VCONN implementation for the US port of HX3PD is shown in Figure 13. The reference design uses the power switch AP2822AKATR-G1 from Diodes Incorporated to source 5 V @ 500 mA. The output of the power switch, V5P0_P0, provides the VCONN supply to the CC lines of the US Type-C connector through the C4 pin of HX3PD. The enable pin (EN) of the power switch is active HIGH.

For the US port, an overcurrent event occurs when the EMCA sinks more than 500-mA on the VCONN line. Then, VOUT of the power switch is cut off. Due to this, there will be a voltage drop on the V5P0_P0 pin; an internal comparator is used to detect this drop. After sensing the voltage drop on this pin, the PD Controller section turns OFF the internal FET that is sourcing VCONN to the EMCA cable.

Figure 13. Power Switch Used for VCONN Implementation and OCP at US Port



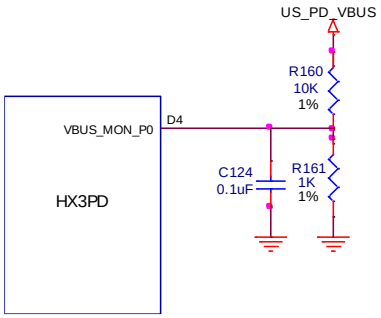
Note: The VCONN implementation and VCONN OCP circuit at the DS1 port is exactly like the one at the US port as shown in Figure 13.

For other Type-C ports (DS2 and DS3), VCONN and its OCP implementation are integrated inside the HX3PD device and therefore do not require external power switches for VCONN implementation at those ports. For these ports, an overcurrent event occurs when the EMCA sinks more than 200 mA current on the VCONN line.

2.8 VBUS Monitor for US and DS1 Ports

Since the US and DS1 ports of HX3PD support multiple PDOs, the VBUS of these PD ports must be monitored. VBUS_MON_P0 and VBUS_MON_P1 pins are used to monitor VBUS at the US and DS1 ports respectively. Figure 14 shows how a potential divider is used to scale down the VBUS value by a factor of 11. The scale down factor is chosen as 11 because the highest VBUS value is 20 V and the maximum input voltage that can be fed to the internal ADC is 2 V. It is mandatory to use resistors with 1% tolerance for the potential divider. A 0.1-µF decoupling capacitor is also used to filter out any high-frequency noise.

Figure 14. VBUS Monitor for US Port



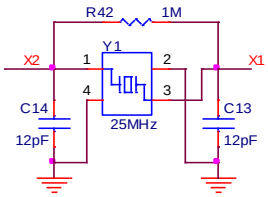
Note: The VBUS monitor circuit at the DS1 port is exactly like the one at the US port.

2.9 Crystal Requirements

HX3PD requires an external crystal with the following parameters:

- 25 MHz ± 50 ppm
- Parallel resonant, fundamental mode
- 100-µW maximum drive level

Figure 15. Crystal Circuit



Note: R42 is a damping resistor.

2.9.1 Crystal Power Dissipation

The power dissipation of the crystal depends on the following:

- The voltage level at the output pin (X2 in Figure 15)
- The operating frequency, f
- The equivalent series resistance (ESR) of the crystal, R

Equation 1. Power Dissipation of the Crystal

$$P = I^2_{RMS} R = \left(\frac{V_{RMS}}{|Z|}\right)^2 R = \left(\frac{1}{2}\right) * \left[\pi f \left(C_{TOT}\right) V_{pp}\right]^2 R$$

where:

f is the crystal frequency

C_{TOT}=C_{L1} + (C_s/2)

C_{L1} is the external load capacitance at the amplifier input (C_{13} in Figure 15)

C_s is the stray capacitance

R is the crystal ESR obtained from the data sheet of the crystal

V_{pp} is the maximum voltage on the output pin – 1.32 V

The parameters of the crystal (ABM8G-25.000MHZ-B4Y-T by Abracon LLC as shown in Figure 15) used in HX3PD's reference design are: f = 25 MHz, R = 60 Ω.

2.9.2 Calculating Load Capacitance Values

The capacitors C_{13} and C_{14} (as shown in Figure 15) must be chosen carefully based on the load capacitance value of the crystal.

Equation 2. Load Capacitance of a Crystal

$$C_L = \frac{C_{13} * C_{14}}{C_{13} + C_{14}} + C_s$$

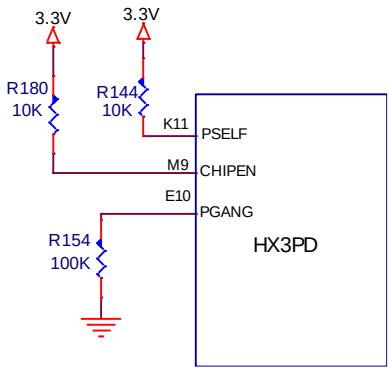
C_s is the stray capacitance of the XOUT and XIN traces on the PCB. Typically, C_s ranges between 2 pF and 5 pF. For the crystal used in the HX3PD reference design, C_L = 10 pF. Also, considering the worst case scenario, PCB C_s = 5 pF. From Equation 2, C_{13} = C_{14} = 10 pF. The HX3PD reference design uses C_{13} = C_{14} = 12 pF.

Now, using Equation 1, the power dissipation for this crystal is found as 67.7 µW. This is less than the 100-µW crystal drive level. If the power dissipation of the crystal is higher than the maximum drive level, it will cause accelerated aging or even burnout of the crystal. Therefore, always use a crystal with a rated drive level higher than the crystal's power dissipation.

2.10 Other Configuration Options

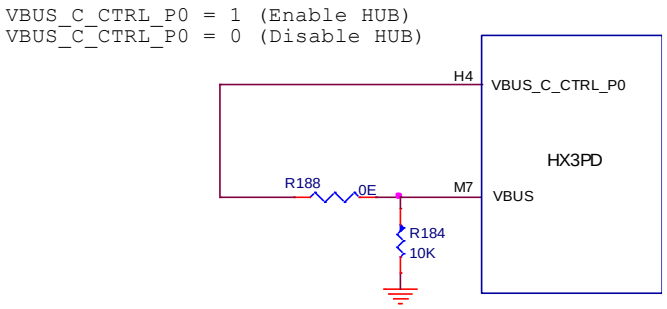
The CHIPEN pin (active HIGH) is pulled up to 3.3 V through a 10-kΩ resistor so that the chip is always enabled. In the Cypress reference design, the PSELF pin is pulled up through a 10-kΩ resistor to keep HX3PD in self-powered mode. The PGANG pin of HX3PD is pulled down by a 100-kΩ resistor to operate it in individual power switching mode as discussed previously.

Figure 16. CHIP ENABLE, PSELF and PGANG



HX3PD also has a provision to enable/disable the Hub Controller depending on whether the US port is connected or not. A connection at the US port is detected by monitoring the CC lines. The Hub Controller Enable pin (VBUS) is pulled down through a 10-kΩ resistor. When a connection is detected at the US port, the PD Controller makes VBUS_C_CTRL_P0 HIGH, which enables the Hub Controller.

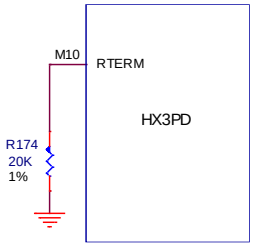
Figure 17. Hub Enable



2.11 USB Precision Resistor

RTERM: This pin should be connected to a precision resistor (20 kΩ ±1%) for SuperSpeed PHY termination impedance calibration (as shown in Figure 18). The resistor should be placed close to HX3PD and one end should be connected to GND with the shortest possible trace length.

Figure 18. USB Precision Resistor

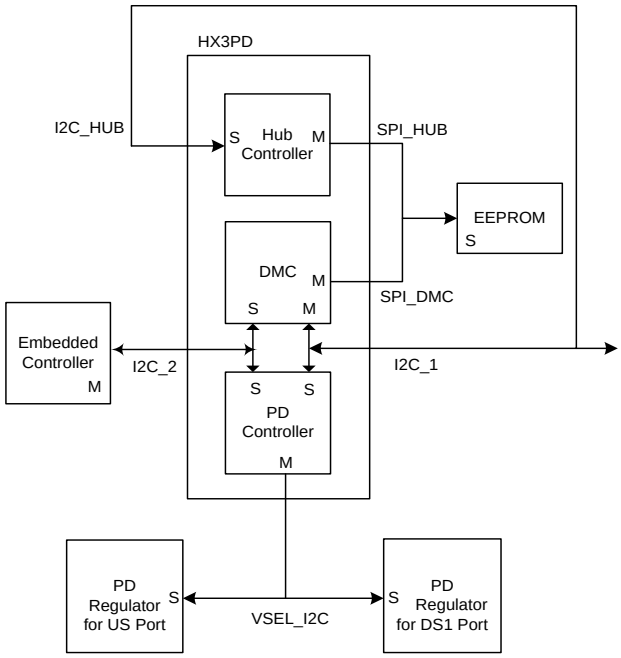


2.12 Communication Interfaces

HX3PD supports SPI and I²C interfaces for communication with individual blocks like EEPROM and Embedded Controller (EC). Firmware and configuration image for the Hub Controller is stored in the external SPI EEPROM while the PD Controller and DMC images are stored in the respective device flash. HX3PD has two SPI and four I²C interfaces (See Figure 19).

- **SPI_HUB:** This interface connects the Hub Controller section of HX3PD to a SPI EEPROM. At the time of boot up, firmware stored in the EEPROM is accessed by the Hub Controller section of HX3PD through SPI_HUB interface. The SPI_HUB interface signal connections are shown in detail in Figure 20.
- **SPI_DMC:** The DMC also has access to the SPI EEPROM using the SPI_DMC interface. This interface is used by DMC to write the Hub Controller firmware onto the EEPROM. DMC receives the firmware from a PC through USB 2.0 interface. The SPI_DMC interface signal connections are shown in detail in Figure 20.
- **I2C_1:** This interface connects the DMC and PD Controller. The DMC acts as the I²C Master and the PD Controller acts as the I²C Slave. The I2C_SCL1 and I2C_SDA1 pins of HX3PD are the pins of this interface, each provided with external pull-up resistors of 2.2 kΩ.
- **I2C_2:** The I²C interface I2C_2 is connected to the DMC and PD controllers – DMC I²C is a slave; and PD I²C is unused in the default firmware. An external I2C master, such as Embedded Controller (EC), shall use this interface to communicate to the DMC and PD controllers.
- **I2C_HUB:** The I²C interface I2C_HUB is connected to the Hub Controller – the Hub Controller acting as the I²C Slave. The DMC accesses I2C_HUB by connecting externally using I2C_1 to read the Hub status and write the Hub configuration. Thus, in Cypress reference design, DMC acts as the Master and Hub Controller acts as the Slave for this I²C interface. The I2C_CLK_HUB and I2C_DAT_HUB pins of HX3PD are used for this interface.
- **VSEL_I2C:** This is the I²C interface between the PD Controller section of HX3PD and the two external PD regulators. It is used to select the VBUS voltage of the PD-enabled ports. The VSEL_GPIO1 and VSEL_GPIO2 pins are used as I2C_MASTER_SDA and I2C_MASTER_SCL respectively. These pins must be connected to the external NCP's I²C interface to configure voltage levels for PD ports.

Figure 19. SPI/I²C Interfaces

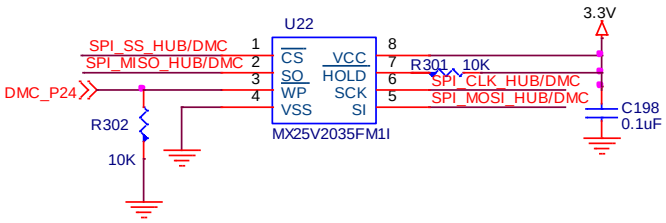


Note: 'M' and 'S' inside the blocks denote 'Master' and 'Slave' respectively.

The EEPROM connection is shown in Figure 20. HX3PD firmware image size is 32 KB (maximum); Cypress recommends provision to support dual images in the EEPROM. Therefore, the recommended EEPROM size is 64 KB or higher. During the firmware upgrade process, in case the primary image of the Hub Controller is corrupted, HX3PD recovers the primary image using the secondary image to ensure that the system continues to function normally. In the case of DMC and PD Controller images, HX3PD falls back to the secondary image if the primary image is corrupted. The Cypress reference design uses MX25V2035FM1I EEPROM by Macronix. Cypress also recommends the following part numbers:

1. S25FL064 by Cypress
2. W25Q80JV by Winbond

Figure 20. EEPROM Connection



Do the following to configure the EEPROM:

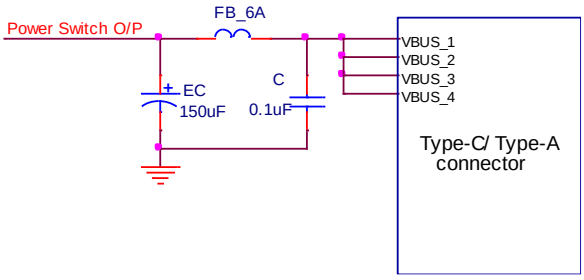
1. Connect the CS (Chip Select) pin of the EEPROM to the SPI_SS_HUB/SPI_SS_DMC pins of HX3PD.
2. Keep the HOLD pin HIGH to make the hold function inactive. The function of the HOLD pin (active LOW) is to pause the device without deselecting the device.
3. The WP (Write Protect) pin is an active LOW pin and is controlled by the DMC. In general, this pin is kept LOW to protect the EEPROM contents from external spurious signals during normal operation; whenever the firmware needs to be updated, DMC drives this pin HIGH.
4. Connect the SCK pin of the EEPROM to the SPI clock pins of the Hub Controller (SPI_CLK_HUB) and DMC (SPI_CLK_DMC) sections.

5. Connect the SI pin of the EEPROM to the MOSI lines of the Hub Controller (SPI_MOSI_HUB) and DMC (SPI_MOSI_DMC) sections.
6. Connect the SO pin of the EEPROM to the MISO lines of the Hub Controller (SPI_MISO_HUB) and DMC (SPI_MISO_DMC) sections.

2.13 VBUS Capacitance, Filtering, and Shield Termination

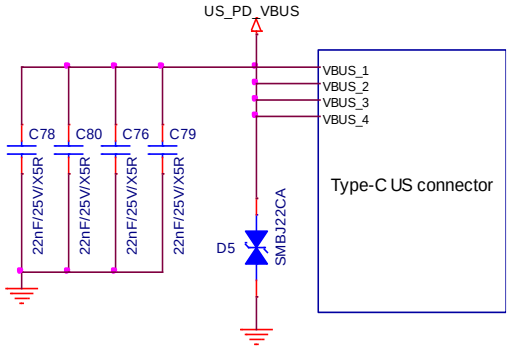
According to the USB specification, every Downstream Facing Port (DFP) must have a minimum capacitance of 120 µF on the VBUS pin to maintain a stable voltage under the maximum load condition. The Upstream Facing Port (UFP) requires only less than 10 µF on the VBUS pin. The Cypress reference design uses up to 150 µF on the VBUS pins of DS ports as shown in Figure 21. The US port of HX3PD is a dual-role port and therefore can take the role of a DFP or UFP. The US port takes the role of a DFP when the Hub charges a device connected at the US port. In this condition, the capacitance at the output of the PD regulator is enough to serve the purpose of maintaining a stable VBUS voltage.

Figure 21. VBUS Filtering for DS2 to DS7 Ports



The US and DS1 ports of HX3PD have PD regulators to support the PD feature. Since the PD regulator circuits provide regulated VBUS at these ports, it is enough to have 22-nF capacitance on the VBUS pins of the Type-C connectors to further filter out any high-frequency noise. Additionally, a TVS diode SMBJ24CA-E3/52 by Vishay Semiconductors is used to clamp out any high-voltage transients as shown in Figure 22. Figure 21 shows the filtering circuit used for DS2 to DS7 ports.

Figure 22. VBUS Filtering for US Port

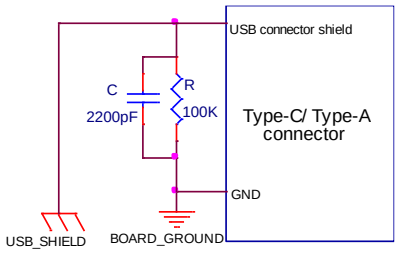


Note: i) The VBUS filtering circuit used at the DS1 port is the same as shown in Figure 22.

ii) VBUS_1, VBUS_2, VBUS_3, and VBUS_4 are the VBUS pins of the Type-C connector.

The USB connector shield should be terminated to BOARD_GROUND (GND) with a parallel RC circuit to reduce EMI as shown in Figure 23.

Figure 23. Shield Termination for US and DS Ports



3 Layout Design Considerations

Take special care in component selection, location of power supply decoupling capacitors, signal line impedance, and noise when designing a board for USB 3.1 Gen 2 application. This section explains PCB design guidelines for routing power and USB signal lines.

Refer to Appendix A for general information on PCB layout techniques.

3.1 Power System Design

Power supply to the HX3PD chip must be clean and stable for reliable Hub operation. Improper layouts lead to poor signal quality, especially on the USB signaling, resulting in higher error rates and increased error-correction retries. These symptoms can lead to Hub enumeration failure. Consider the following points while designing power system network.

- Placement of bulk and decoupling capacitors
- Power domain routing
- Placement of power and ground planes

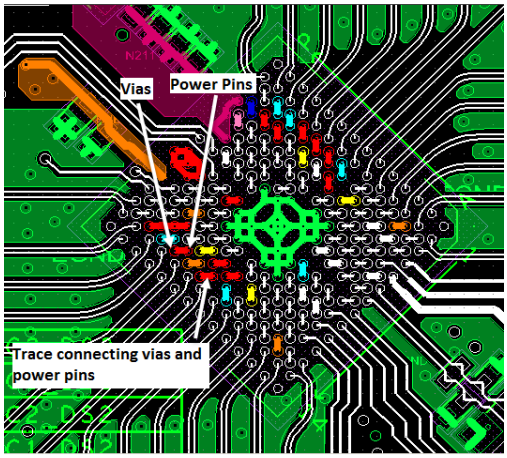
3.1.1 Placement of Bulk and Decoupling Capacitors

Place decoupling capacitors close to the power pins for high-frequency noise filtering. It is recommended to place them on the opposite side of the PCB directly under the HX3PD to reduce planar inductance.

Place the bulk capacitor, which acts as a local power supply to the power pin, near the decoupling capacitors. Minimize the trace length between the bulk capacitor and the decoupling capacitors.

Make the power trace width the same as the power pad size. To connect power pins to the power plane, keep vias very close to the power pads as shown in Figure 24. This helps in minimizing stray inductance and IR drop on the line.

Figure 24. Power Delivery Network



3.1.2 Power Domain Routing

HX3PD has several power domains. Use split planes on the power layer, top layer, and bottom layer for the power domains as shown in Figure 25 to Figure 27. The following guidelines are recommended for power traces:

- Keep power traces away from SuperSpeed USB 10 Gbps, SuperSpeed USB, and HS data and clock lines.
- Power trace widths should be ≥ 25 mils to reduce inductance.
- Keep power traces short. Use larger vias on power traces.

Figure 25. Split Planes on the Power Layer

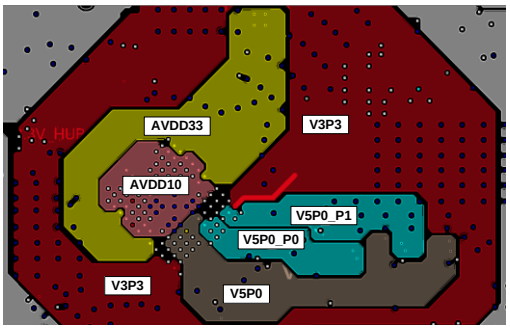


Figure 26. Split Planes on the Top Layer

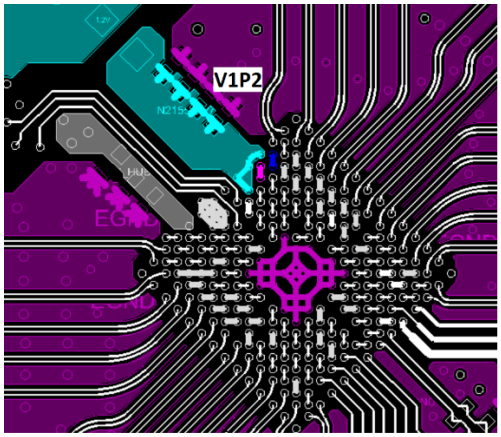
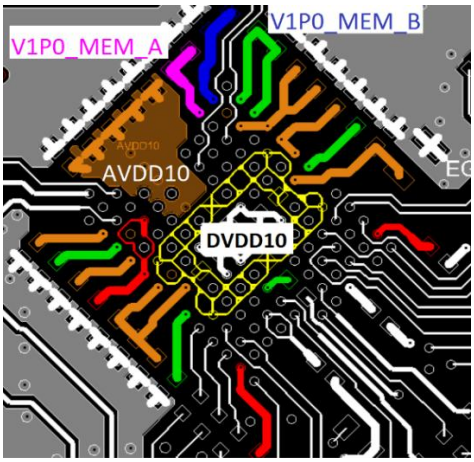


Figure 27. Split Planes on Bottom Layer



3.1.3 Placement of Power and Ground Planes

Place the power plane near the ground plane for good planar capacitance. Planar capacitance that exists between the planes acts as a distributed decoupling capacitor for high-frequency noise filtering, thereby reducing electromagnetic radiation.

3.2 Routing of USB Data Lines

Pay attention while routing USB signal lines to achieve good signal quality and reduced emission. Pay attention to the following key factors while routing USB signal lines during the PCB design phase.

3.2.1 Controlled Differential Impedance

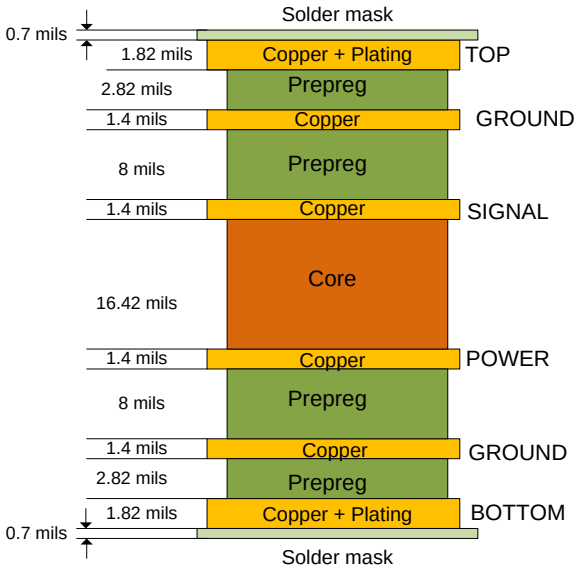
The differential impedance of USB signal lines (SuperSpeed USB 10 Gbps/ SuperSpeed USB/HS) should be 90 Ω ±7%. Otherwise, it affects the signal eye pattern, jitter, and crossover voltage measurements.

Refer to Appendix B to learn about the underlying theory of differential impedance.

3.2.2 Typical 46.4-Mil, 6-Layer PCB Example

The recommended stack-up for a standard 48.7 mil (1.24 mm) thick PCB is shown in Figure 28.

Figure 28. Stackup Details



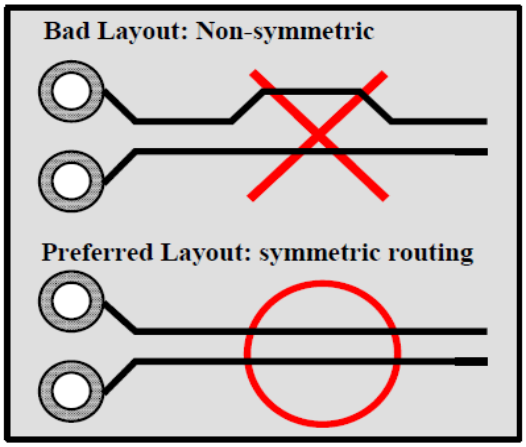
3.2.3 Impedance Matching

A layout which demonstrates the placement of a differential pair is shown in Figure 29. 'W' is the trace width, 'S' is the spacing between a differential pair and 'g' is the minimum gap between the trace and other planes. The value of the spacing 'S' should be chosen higher than the trace width 'W'. In the Cypress reference design, W=4.5 mils, S=5 mils and g=9 mils. In this case, the calculated differential impedance, Z_{diff}, is 90-Ω.

Figure 29. Differential Pairs Placements

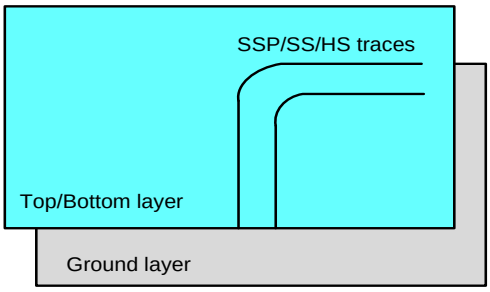
The trace widths and the spacing between the differential pairs must be maintained constant for symmetric routing, as shown in Figure 30.

Figure 30. Symmetric Routing of Differential Pairs



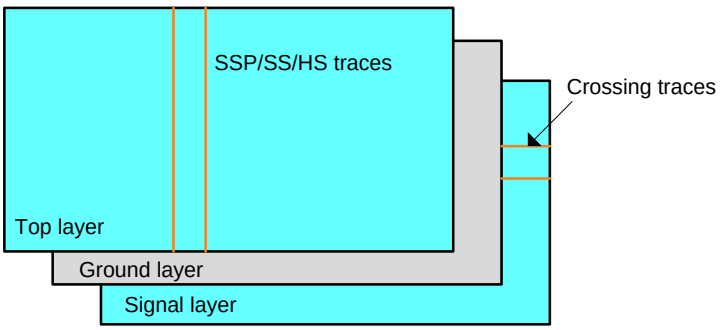
All differential pair signals should be routed over an adjacent ground plane layer to provide a good return current path. Splitting the ground plane underneath the signals introduces impedance mismatch, thereby increasing the loop inductance and electrical emissions. Figure 31 shows a solid ground plane under the differential pair signal layer.

Figure 31. Solid Ground Plane Under Differential Pair Signal Layer



Whenever two pairs of USB traces cross each other in different layers, a ground layer should run between the two USB signal layers, as Figure 32 shows.

Figure 32. Ground Insertion



3.2.4 Trace Length

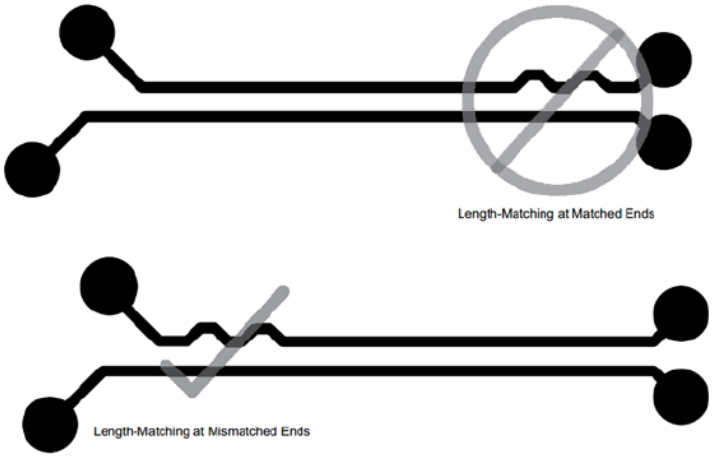
The USB signal trace length should be as short as possible. Long traces increase insertion loss and emission, and introduces Inter-Symbol Interference (ISI) to the far-end receiver. Trace lengths of differential pairs must be matched to maintain uniform impedance all along the trace.

Note: In the HX3PD reference design, SuperSpeed USB 10 Gbps/ SuperSpeed USB lines are characterized for a trace length of up to three inches. It is recommended that the length of these traces be kept under three inches.

During PCB layout design, prioritize the routing of USB signal lines. Ensure that the following recommendations are met:

- The difference in trace lengths of the HS (D+ and D–) signals should be matched within 1.25 mm (50 mils) for impedance matching.
- The difference in trace lengths of the SuperSpeed USB 10 Gbps differential pairs (Rx± /Tx±) must be matched within 0.12 mm (5 mils). This is to be followed for SuperSpeed USB differential pairs also.
- Always make adjustments (by putting loops as shown in Figure 33) for SuperSpeed USB 10 Gbps/ SuperSpeed USB/HS signal trace lengths near the USB receptacle and not near the device. The figure shows the matched and mismatched ends near the receptacle. Always adjust the length at the mismatched ends.

Figure 33. Length Matching



There are different routing methods for length matching. Figure 34 and Figure 35 show single arc routing and serpentine routing methods respectively.

Figure 34. Single Arc Routing

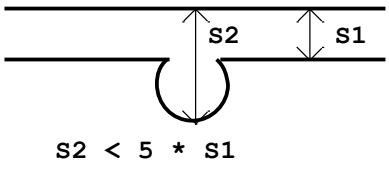
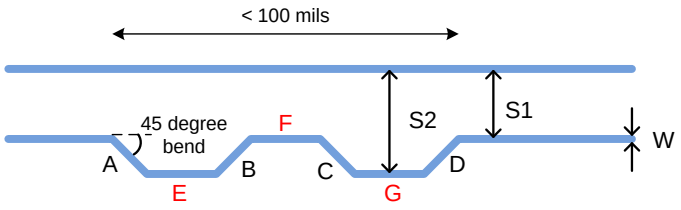


Figure 35. Serpentine Routing



A=B=C=D
E=F=G=3W (W=trace width)
Length < 100 mils
S2 < 2* S1

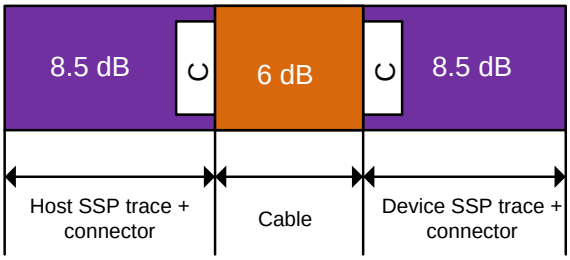
In order to meet the SuperSpeed USB 10 Gbps channel insertion loss budget as documented in USB-IF's white paper 'USB 3.1 Channel Loss Budgets', follow the guidelines given below:

- Select proper FR4 material for 10-Gbps operation by choosing the material properties as follows:
  - Dielectric constant (D_k) ≤ 3.9
  - Loss tangent (D_f) ≤ 0.025
  - Glass transition temperature (T_g) = 180^0

  Low values of D_k and D_f are suitable for high-speed transmission of signals.

  Cypress reference design uses the FR4 material 370HR with properties D_k = 3.0, D_f = 0.025 and T_g = 180^0.
- Maintain channel insertion loss for SuperSpeed USB 10Gbps at less than 23 dB (which includes the loss budgets for host trace, connectors, cable, and device trace).
- Maintain the insertion loss of the SuperSpeed USB 10 Gbps trace + connector at less than 8.5 dB.

Figure 36. Channel Insertion Loss Budget for SuperSpeed USB 10 Gbps

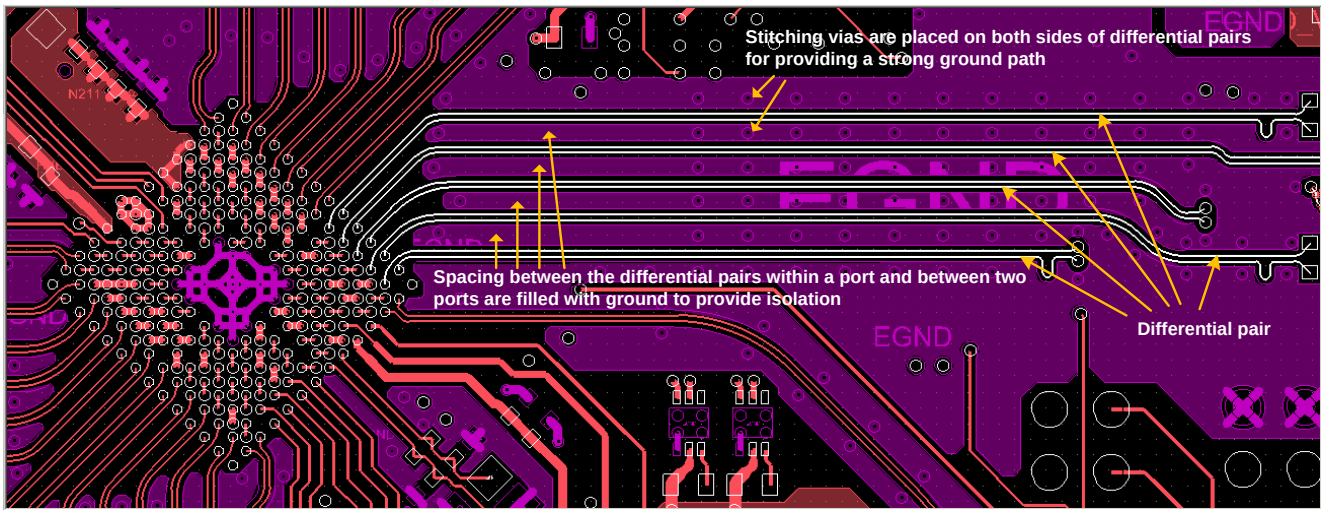


3.2.5 Port Isolation

Port-to-port isolation is required to minimize cross talk between Tx lines of one port and the Rx lines of another port. Isolation is also required to minimize cross talk between Tx lines and Rx lines within a port. In order to provide these isolations, the spacing between the differential pairs (Rx± /Tx±) within a port and between two ports must be filled with ground. Maintain a minimum of 2W space, where W = trace width.

Provide stitching vias on both sides of the SuperSpeed USB 10 Gbps, SuperSpeed USB, and HS traces to ensure proper isolation between ports. These stitching vias are connected to the ground plane. Figure 37 shows the routing of ground traces on both sides of the USB data line pairs using stitching vias.

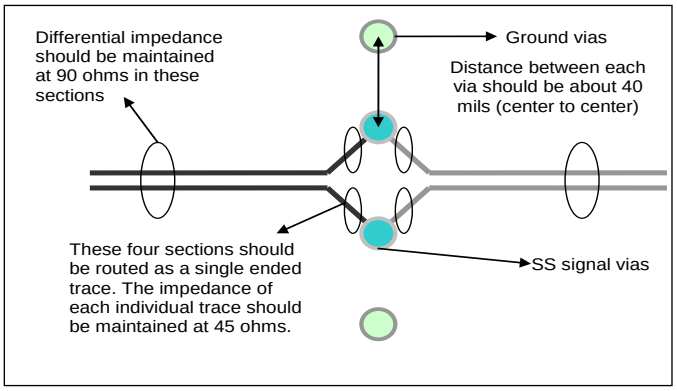
Figure 37. Port Isolation



3.2.6 Signal Via Routing

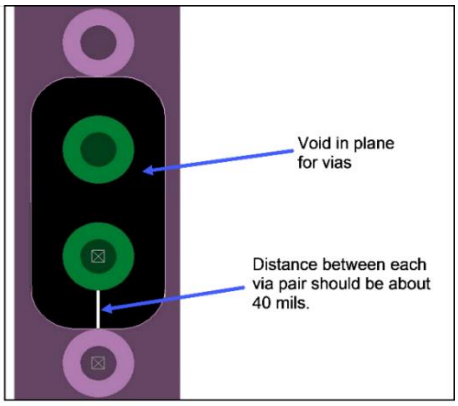
It is recommended that SuperSpeed USB 10 Gbps/SuperSpeed USB signals be routed in a single layer. Vias introduce discontinuities in the signal line and affect the SuperSpeed USB 10 Gbps/SuperSpeed USB signal quality. However, if vias are not avoidable and you need to route the signals to another layer, maintain continuous grounding to ensure uniform impedance throughout. To do so, place ground vias next to signal vias as shown in Figure 38. The distance between a pair of signal and ground vias can be at most 40 mils. A maximum of two pairs of vias are allowed on the SuperSpeed USB 10 Gbps/SuperSpeed USB lines.

Figure 38. Ground Vias



Voids for vias on signal traces should be common for the differential pair. Common void, as shown in Figure 39, helps in matching the impedance compared to separate voids.

Figure 39. Void Placement for Signal Trace Vias



3.2.7 Other Recommendations

- Place the capacitor used in the RC reset circuitry as close as possible to the reset pins of HX3PD.
- Place the crystal less than 1 cm from HX3PD. Make sure that there is a solid ground plane under the crystal trace.
- When using a Type-C receptacle, it is highly recommended that USB signal lines are connected to the receptacle pins on the opposite layer as the receptacle, as shown in Figure 40. For example, if the Type-C receptacle is placed on the top layer, the signal lines should be connected to the receptacle pins on the bottom layer. This is to avoid pin stubs (antennas).

Figure 40. Type-C Receptacle Placement

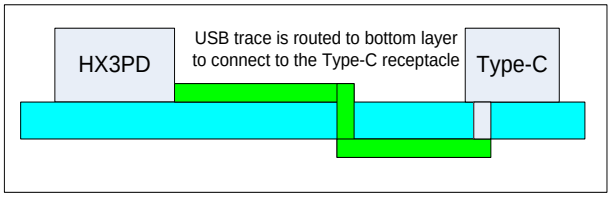


Figure 41. Type-C Receptacle Layout – Top Layer

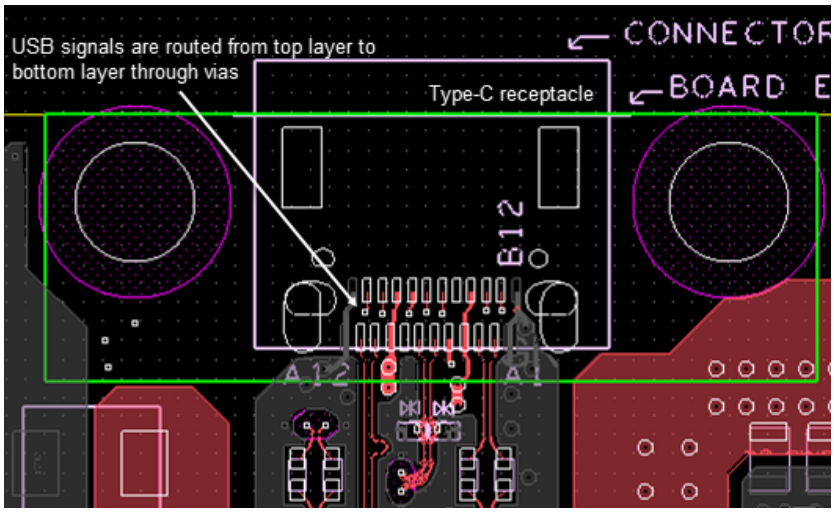


Figure 42. Type-C Receptacle Layout – Bottom Layer

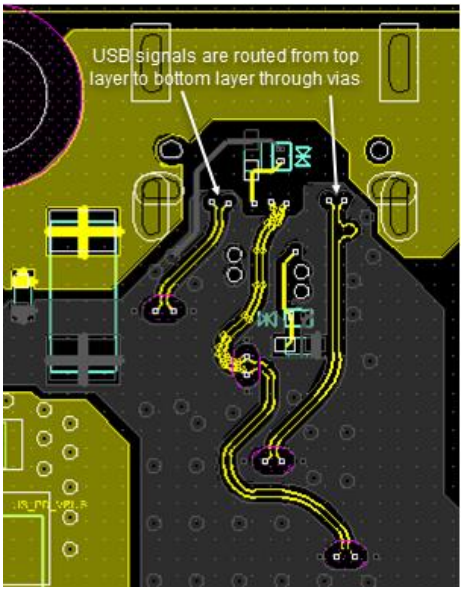
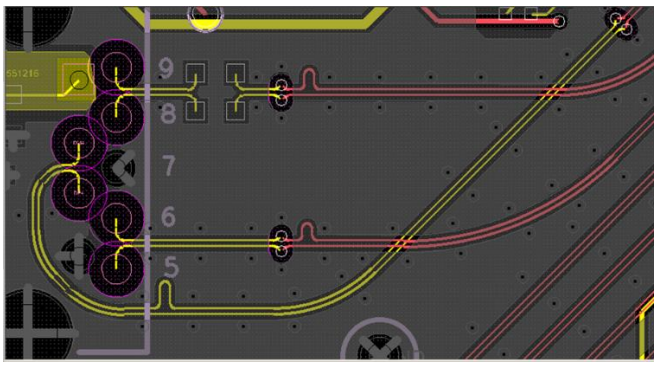


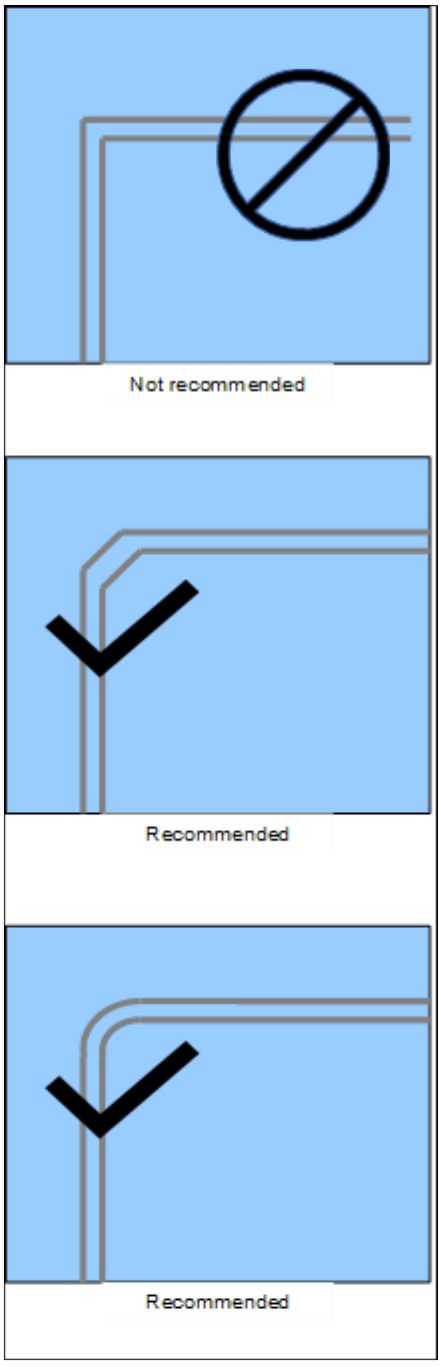
Figure 43 illustrates the recommended layout for a Type-A receptacle.

Figure 43. USB Signals Connected on Opposite Side of Standard-A USB Receptacle to Avoid Stub on Line



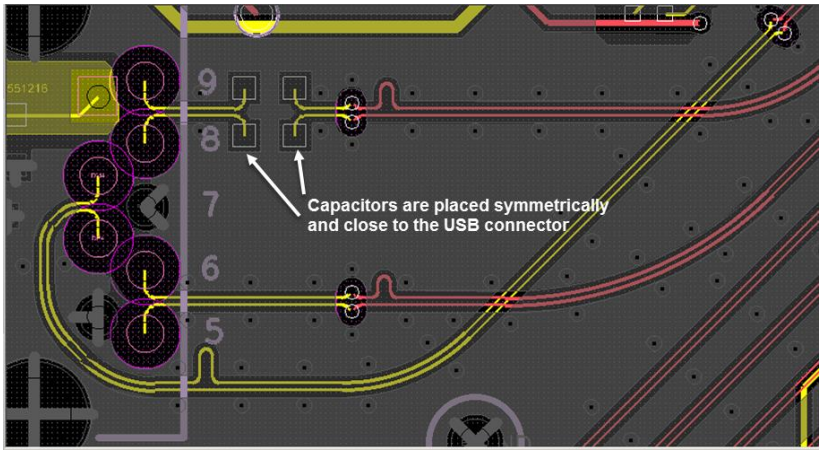
- The polarity of the SuperSpeed USB 10 Gbps/SuperSpeed USB differential pairs can be swapped. Polarity detection is done automatically by the SuperSpeed PHY during link training. The polarity inversion mechanism can be utilized to ensure that USB traces do not cross each other.
- On the USB signal lines, use as few bends as possible. Do not use 90-degree bends. Use 45-degree or rounded (curved) bends if necessary, as illustrated in Figure 44.

Figure 44. USB Signal Bends



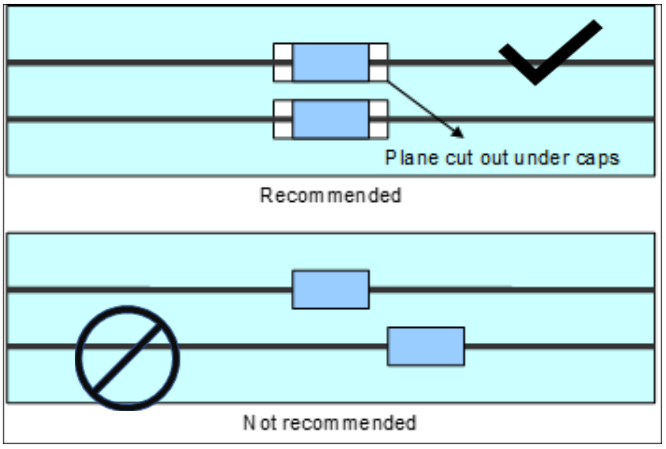
- SuperSpeed USB 10 Gbps/SuperSpeed USB traces require additional AC coupling capacitors (0.1 µF) on the Tx lines (on US and DS ports as shown in Figure 45). For US and DS ports, place these capacitors symmetrically and near to the connector.

Figure 45. SuperSpeed USB 10 Gbps Tx Line AC Coupling Capacitors



Two immediate planes underneath the AC coupling capacitors should have a cutout in the shape of these capacitors to avoid extra capacitance on the lines created by the capacitor pads. Figure 46 shows the proper layout of the decoupling capacitors.

Figure 46. SuperSpeed USB 10 Gbps/SuperSpeed USB Tx AC Coupling Capacitors Layout



4 Schematics and Layout Review Checklist

Table 3 is a checklist for all the important guidelines. Provide an answer to each checklist item to find out the extent to which your hardware design meets these guidelines.

Table 3. Schematics and Layout Review Checklist

No.	Schematic checklist	Answer (Yes/No/NA)
1	Are the decoupling capacitors and bulk capacitors connected as per Figure 3?	
2	Do you have isolation between VDDIO and V3P3 using the ferrite bead as shown in Figure 3?	
3	Does the 1.2-V supply come up after 3.3-V with a delay of 3 ms?	
3	Does the crystal meet the maximum power drive level as specified in this application note?	
4	Are all DS ports provided with 150-µF bulk capacitors?	
5	Do the Power-on-Reset RC components meet the required reset times?	
6	Does the USB precision resistor have 1% tolerance?	
7	Are the I^2C lines provided with pull-up resistors to the 3.3-V domain?	
8	Is the WP pin of the EEPROM pulled down through a 10-k resistor?	
9	Are the CHIPEN and PSELF pins pulled up to 3.3 V?	
10	Is the PGANG properly enabled for individual mode or ganged mode?	
11	Are all USB connector shields terminated properly?	
12	Are the VBUS_MON_Px pins provided with correct potential divider (to scale down to 11)?	
13	Are the VBUS discharge resistors rated for 2-W of power dissipation?	
	Layout Checklist	
1	Is the crystal placed close to the chip (less than 1 cm)?	
2	Are the decoupling capacitors and bulk capacitors placed close to the HX3PD power pins?	
3	Are the power vias placed close to the HX3PD power pins?	
4	Are the power traces routed away from the SuperSpeed USB 10 Gbps/SuperSpeed USB/HS data lines and the clock lines?	
5	Is the capacitor in the RC reset circuitry placed close to the reset pin of HX3PD?	
6	Is the 150-µF capacitor placed close to the DS port connector?	
7	Are the SuperSpeed USB 10 Gbps, SuperSpeed USB and HS signal lines matched in length?	
8	Are the USB data lines provided with solid ground plane underneath?	
9	Are the SuperSpeed USB 10 Gbps/SuperSpeed USB/HS traces provided with stitching ground vias?	
10	Are the SuperSpeed USB 10 Gbps/SuperSpeed USB traces provided with the AC decoupling capacitors (0.1 µF) on the TX lines?	
11	Are the SuperSpeed USB 10 Gbps/SuperSpeed USB traces lengths less than three inches?	
12	Is it ensured that there are no stubs on all the USB traces?	
13	Is it ensured that there are only two pairs of vias on the SuperSpeed USB 10 Gbps/SuperSpeed USB traces?	
14	Are the USB differential pair signals (SuperSpeed USB 10 Gbps, SuperSpeed USB, HS) routed without 90-degree bends?	

5 Summary

HX3PD is a USB 3.1 Gen 2 (10 Gbps) Type-C Hub with Power Delivery capability. Its SuperSpeed USB 10 Gbps operation demands careful hardware design to preserve signal integrity. By following the guidelines in this application note, your HX3PD-based design has a good chance of first-pass success.

6 Acronyms

Acronym	Description
BC	Battery Charging
CC	Configuration Channel
DFP	Downstream Facing Port
DS	Downstream
EC	Embedded Controller
EEPROM	Electrically Erasable Programmable Read-Only Memory
FS	Full Speed
GND	Ground
GPIO	General-Purpose Input Output
HS	High Speed
I/O	Input/Output
ISI	Inter-Symbol Interference
LED	Light-Emitting Diode

Acronym	Description
LS	Low-Speed
NC	No Connect
PCB	Printed Circuit Board
PD	Power Delivery
POR	Power-On Reset
ROM	Read Only Memory
SCL	Serial Clock
SDA	Serial Data
TT	Transaction Translator
UFP	Upstream Facing Port
US	Upstream
USB	Universal Serial Bus

About the Authors

Name: Hena Thampy

Title: Senior Applications Engineer

Name: Vetrivel Prakasam

Title: Principal Systems Engineer

Appendix A. PCB Layout Tips

There are many classic techniques for designing PCBs for low noise and EMC. Some of these techniques include the following:

- **Multiple layers:** Although they are more expensive, it is best to use a multilayer PCB with separate layers dedicated to the V_{SS} and V_{DD} supplies. This provides good decoupling and shielding effects. It is recommended to use at least a six-layer PCB for HX3PD.
- **Component position:** You should separate the different circuits on the PCB according to their EMI contribution. This will help reduce cross-coupling on the PCB. For example, separate noisy high-current circuits, low-voltage circuits, and digital components.
- **Ground and power supply:** There should be a single point for gathering all ground returns. Avoid ground loops, or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding.

  The power supply should be close to the ground line to minimize the area of the supply loop. The supply loop can act as an antenna and can be a major emitter or receiver of EMI.
- **Decoupling:** The decoupling capacitors should be placed as close as possible to the V_{SS} and V_{DD} pins of the device to reduce high-frequency power supply ripple.

  Generally, decouple all sensitive or noisy signals to improve EMC performance. Decoupling can be both capacitive and inductive.
- **Signal routing:** When designing an application, analyze the following areas to improve EMC performance:
  - Noisy signals, for example, signals with fast edge times
  - Sensitive signals, like reset and crystal oscillator signals
  - Signals that capture events, such as interrupts and strobe signals

To improve the EMC performance, keep the signal trace lengths as short as possible and isolate the traces with V_{SS} traces. To avoid crosstalk, do not route them near to or parallel to other noisy and sensitive traces.

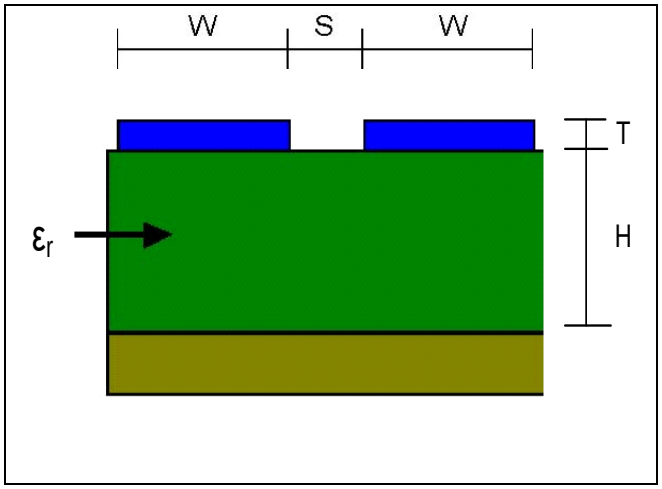
Appendix B. Differential Impedance of USB Traces

The copper traces on the outer layers of a PCB are called microstrips. A microstrip has an impedance, Z_0, which is determined by its width (W), height (T), distance to the nearest copper plane (H), and the relative permittivity (ε_r) of the material (commonly FR-4) between the microstrip and the nearest plane.

When two microstrips run parallel to each other, cross-coupling occurs. The space between microstrips (S) as related to their height above a plane (H) affects the amount of cross-coupling that occurs. The amount of cross-coupling increases as the space between the microstrips is reduced. As cross-coupling increases, the microstrips' impedances decrease. Differential impedance, Z_{diff}, is calculated by measuring the impedance of both the microstrips and summing them.

Figure 47 illustrates a cross-sectional representation of a PCB, showing (from top to bottom) the differential traces, the substrate, and the ground plane.

Figure 47. Microstrip Model of Differential Impedance



Equation 3 and Equation 4 provide the formulas necessary to estimate differential impedance using a 2D parallel microstrip model. Table 4 provides the definition of the variables. These formulas are valid for the ratios $0.1 < W/H < 2.0$ and $0.2 < S/H < 3.0$. Commercial utilities can obtain more accurate results using empirical or 3D modeling algorithms.

Equation 3. Differential Impedance Formula

$$Z_{diff} = 2 \times Z_0(1 - 0.48e^{-0.96S/H})$$

Equation 4. Impedance of One Microstrip

$$Z_0 = (87/(\varepsilon_r + 1.41)^{0.5}) \ln(5.98H/0.8W + T)$$

Table 4. Definition of Differential Impedance Variables

Variable	Description
Z_{diff}	Differential impedance of two parallel microstrips over a plane
Z_0	Impedance of one microstrip over a plane
W	Width of the traces
H	Distance from the ground plane to the traces
T	Trace thickness
S	Space between differential traces (air gap)
ε_r	Relative permittivity of substrate (FR-4)

Document History

Document Title: AN222944 – EZ-USB HX3PD Hardware Design Guidelines and Checklist

Document Number: 002-22944

Revision	ECN	Date	Description of Change
**	6052228	02/01/2018	New Application Note
*A	6521941	04/17/2019	Updated the application note based on the latest revision of the reference design
*B	6892110	06/11/2020	Updated Figure 1, Figure 2 and Figure 7. Changed pin names of VCONN_MON_P0 and VCONN_MON_P1 to VCONN_MON_P0/PD_24 and VCONN_MON_P1/PD_P27 respectively. Modified Section 2.6.2 to include the hardware changes to connect PWREN1 (Power Enable of DS1) to PD controllers VCONN_MON_P1/PD_P27. Updated Section 2.12 based on the latest HX3PD datasheet. Updated sections 2.1, 2.6, 2.6.1 and 2.7 to include the latest hardware changes.

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