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AN221699

Migration Guide for S25FL128L from S25FL128P or S25FL129P Quad SPI Flash

Author: Zhi Feng

Associated Part Family: S25FL128L, S25FL128P, S25FL129P

AN221699 provides guidelines for migration from Cypress' S25FL128P/S25FL129P to S25FL128L Quad SPI Flash Memory products. It describes the similarities and differences in specifications to facilitate this migration.

Contents

1 Introduction

The S25FL128P and S25FL129P families are 3.0-V Flash memory device based on the 90-nm MirrorBit® process technology. The S25FL128L family is a 3.0-V, single-supply (no V_{IO} power supply), 4-KB uniform sector Flash memory device based on the 65-nm Floating Gate process technology. The FL128P and FL129P families are no longer recommended for new designs. Use this document as a guideline to complete such migration. This document provides comparisons on features and functions to support the migration efforts.

2 Features Comparison

The S25FL128L family is command-set-compatible and footprint-compatible with the S25FL128P and S25FL129P families. Table 1 summarizes the feature similarities and differences among them.

Table 1. Features Comparison

Feature/Parameter	S25FL128L	S25FL128P	S25FL129P
Technology Node	65-nm NOR Flash	90-nm NOR Flash	90-nm NOR Flash
Architecture	Floating Gate	MirrorBit®	MirrorBit®
Density	128 Mb	128 Mb	128 Mb
Bus Width	x1, x2, x4	x1	x1, x2, x4
Supply Voltage	2.7 V – 3.6 V	2.7 V – 3.6 V	2.7 V – 3.6 V
Normal Read Speed (SIO)	6.25 MB/s (50MHz)	5 MB/s (40 MHz)	5 MB/s (40 MHz)
Fast Read Speed (SIO)	16.6 MB/s (133 MHz)	13 MB/s (104 MHz)	13 MB/s (104 MHz)
Dual Read Speed (DIO)	33.3 MB/s (133 MHz)	n/a	20 MB/s (80 MHz)
Quad Read Speed (QIO)	66.6 MB/s (133 MHz)	n/a	40 MB/s (80 MHz)
Quad Read Speed (QIO - DDR)	66 MB/s (66 MHz)	n/a	n/a
Program Buffer Size	256B	256B	256B
Erase Sector Size	4 KB / 32 KB / 64 KB	256 KB or 64 KB	256 KB or 64 KB
Parameter Sector Size	–	4 KB	4 KB
Security Region / OTP	1024B	n/a	506B
Data Protection	Legacy Block Protection Individual and Region Protection	Legacy Block Protection	Legacy Block Protection
Suspend / Resume	Erase / Program	Not supported	Not supported
Addressing	3 / 4 Byte	3-Byte	3-Byte
Hardware Reset	Yes	No	No
Operating Temperature	–40°C to +85°C –40°C to +105°C –40°C to +125°C	–40°C to +85°C	–40°C to +85°C –40°C to +105°C
Deep Power Down	Yes – 2 µA (typical)	Yes – 3 µA (typical)	Yes – 3 µA (typical)
ID and CFI	No	Read_ID only	yes
ID and SFDP	Yes	RDID only	RDID only
Packages	8-pin SOIC (208 mils) 16-pin SOIC (300 mils) 8-Contact WSON (5 × 6 mm) 24-Ball FBGA (6 × 8 mm) 5x5 24-Ball FBGA (6 × 8 mm) 6x4	16-pin SOIC (300 mils) 8-Contact WSON (6 × 8 mm)	16-pin SOIC (300 mils) 8-Contact WSON (6 × 8 mm) 24-Ball FBGA (6 × 8 mm) 5x5 24-Ball FBGA (6 × 8 mm) 6x4

3 Sector Architecture

The S25FL128L family has a uniform sector architecture with 4-KB sectors, 32-KB half blocks, and 64-KB blocks. S25FL128P has two ordering options: one with uniform 64-KB sectors and the other with uniform 256-KB sectors. Similarly, S25FL129P family also has these two options: 64-KB or 256-KB sectors. With the 64-KB sector option, the device will have 32 4-KB parameter sectors either at the bottom or top depending on the configuration register setting.

Since the sector architectures are different, S25FL128L and S25FL128P, S25FL129P families offer different sector address maps. Table 2 and Table 3 show the sector address map comparison for S25FL128L and S25FL128P, S25FL129P.

Table 2. Sector Address Map Comparison – Uniform 64-KB or 256-KB sectors (Bottom 256-KB range)

Address Range	S25FL128L			S25FL128P / S25FL129P	
				Uniform 64 KB	Uniform 256 KB
0000000h – 0000FFFh	Sector 0	Half Block 0	Block 0	Sector 0	Sector 0
…	…				
0007000h – 0007FFFh	Sector 7				
0008000h – 0008FFFh	Sector 8	Half Block 1			
…	…				
000F000h – 000FFFFh	Sector 15				
0010000h – 0010FFFh	Sector 16	Half Block 2	Block 1	Sector 1	
…	…				
0017000h – 0017FFFh	Sector 23				
0018000h – 0018FFFh	Sector 24	Half Block 3			
…	…				
001F000h – 001FFFFh	Sector 31				
0020000h – 0020FFFh	Sector 32	Half Block 4	Block 2	Sector 2	
…	…				
0027000h – 0027FFFh	Sector 39				
0028000h – 0028FFFh	Sector 40	Half Block 5			
…	…				
002F000h – 002FFFFh	Sector 47				
0030000h – 0030FFFh	Sector 48	Half Block 6	Block 3	Sector 3	
…	…				
0037000h – 0037FFFh	Sector 39				
0038000h – 0038FFFh	Sector 40	Half Block 7			
…	…				
003F000h – 003FFFFh	Sector 63				

Table 3. Sector Address Map Comparison – Uniform 64-KB Sectors with 4-KB Parameter Sectors at Bottom

Address Range	S25FL128L			S25FL129P
				Uniform 64 KB with 32 4KB parameter sectors
0000000h – 0000FFFh	Sector 0	Half Block 0	Block 0	Sector 0
…	…			…
0007000h – 0007FFFh	Sector 7			Sector 7
0008000h – 0008FFFh	Sector 8	Half Block 1		Sector 8
…	…			…
000F000h – 000FFFFh	Sector 15			Sector 15
0010000h – 0010FFFh	Sector 16	Half Block 2	Block 1	Sector 16
…	…			…
0017000h – 0017FFFh	Sector 23			Sector 23
0018000h – 0018FFFh	Sector 24	Half Block 3		Sector 24
…	…			…
001F000h – 001FFFFh	Sector 31			Sector 31
0020000h – 0020FFFh	Sector 32	Half Block 4	Block 2	Sector 32
…	…			
0027000h – 0027FFFh	Sector 39			
0028000h – 0028FFFh	Sector 40	Half Block 5		
…	…			
002F000h – 002FFFFh	Sector 47			
0030000h – 0030FFFh	Sector 48	Half Block 6	Block 3	Sector 33
…	…			
0037000h – 0037FFFh	Sector 39			
0038000h – 0038FFFh	Sector 40	Half Block 7		
…	…			
003F000h – 003FFFFh	Sector 63			

4 Command Set Comparison

Table 4 summarizes the commands supported for each device family. Subsequent sections discuss pertinent differences between the families.

Table 4. Command Set Comparison

Function	Command	Description	S25FL128L	S25FL128P S25FL129P
Read Device ID	RDID	Read ID (JEDEC Manufacturer ID)	9Fh	9Fh
	RSFDP	Read JEDEC Serial Flash Discoverable Parameters	5Ah	–
	RDQID	Read Quad ID	AFh	–
	RUID	Read Unique ID	4Bh	–[1]
	READ_ID	Read Manufacturer and Device Identification	–	90h
	RES	Read Electronic Signature		ABh
Register Access	RDSR1	Read Status Register 1	05h	05h
	RDSR2	Read Status Register 2	07h	–
	RDCR1	Read Configuration Register 1	35h	35h[2]
	RDCR2	Read Configuration Register 2	15h	–
	RDCR3	Read Configuration Register 3	33h	–
	RDAR	Read Any Register	65h	–
	WRR	Write Register (Status-1 and Configuration-1,2,3)	01h	–
	WRR	Write Register (Status-1 and Configuration-1)	–	01h
	WRDI	Write Disable	04h	04h
	WREN	Write Enable for Non-volatile data change	06h	06h
	WRENV	Write Enable for Volatile Status and Configuration Registers	50h	–
	WRAR	Write Any Register	71h	–
	CLSR	Clear Status Register	30h	30h[2]
	4BEN	Enter 4 Byte Address Mode	B7h	–
	4BEX	Exit 4 Byte Address Mode	E9h	–
	SBL	Set Burst Length	77h	–
	QPIEN	Enter QPI (Quad SPI 4-4-4)	38h	–
	QPIEX	Exit QPI (Quad SPI 4-4-4)	F5h	–
	DLPRD	Data Learning Pattern Read	41h	–
	PDLRNV	Program NV Data Learning Register	43h	–
	WDLRV	Write Volatile Data Learning Register	4Ah	–
Read Flash Array	READ	Read	03h	03h
	4READ	Read (4-Byte Address)	13h	–
	FAST_READ	Fast Read	0Bh	0Bh
	4FAST_READ	Fast Read (4-Byte Address)	0Ch	–
	DOR	Dual Output Read	3Bh	3Bh

[1] 4Bh is used as OTP Read in FL129P

[2] Only in FL129P

Function	Command	Description	S25FL128L	S25FL128P S25FL129P
	4DOR	Dual Output Read (4-Byte Address)	3Ch	–
	QOR	Quad Output Read	6Bh	6Bh[1]
	4QOR	Quad Output Read (4-Byte Address)	6Ch	–
	DIOR	Dual I/O Read	BBh	BBh
	4DIOR	Dual I/O Read (4-Byte Address)	BCh	–
	QIOR	Quad I/O Read	EBh	EBh
	4QIOR	Quad I/O Read (4-Byte Address)	ECh	–
	DDRQIOR	DDR Quad I/O Read	EDh	–
	4DDRQIOR	DDR Quad I/O Read (4-Byte Address)	EEh	–
Program Flash Array	PP	Page Program	02h	02h
	4PP	Page Program (4-Byte Address)	12h	–
	QPP	Quad Page Program	32h	32h[1]
	4QPP	Quad Page Program (4-Byte Address)	34h	–
Erase Flash Array	SE	Sector Erase	20h	20h[2]
	4SE	Sector Erase (4-Byte Address)	21h	–
	HBE	Half Block Erase	52h	–
	4HBE	Half Block Erase (4-Byte Address)	53h	–
	BE	Block Erase	D8h	D8h
	4BE	Block Erase (4-Byte Address)	DCh	–
	SE	64-KB or 256-KB Sector Erase	–	D8h
	CE	Chip Erase / Bulk Erase	60h	60h
	CE	Chip Erase / Bulk Erase (alternate instruction)	C7h	C7h
Erase / Program Suspend / Resume	EPS	Erase / Program Suspend	75h	–
	EPR	Erase / Program Resume	7Ah	–
Security Region Array	SECRE	Security Region Erase	44h	–
	SECRP	Security Region Program	42h	–
	SECRR	Security Region Read	48h	–
	OTPP	Programs one byte of data in OTP memory space	–	42h[1]
	OTPR	Read data in the OTP memory space	–	4Bh[1]
Array Protection	IBLRD	IBL Read	3Dh	–
	4IBLRD	IBL Read (4-Byte Address)	E0h	–
	IBL	IBL Lock	36h	–
	4IBL	IBL Lock (4-Byte Address)	E1h	–
	IBUL	IBL Unlock	39h	–
	4IBUL	IBL Unlock (4-Byte Address)	E2h	–
	GBL	Global IBL Lock	7Eh	–

[1] FL129P only

[2] P4E command in FL129P only

Function	Command	Description	S25FL128L	S25FL128P S25FL129P
	GBUL	Global IBL Unlock	98h	–
	SPRP	Set Pointer Region Protection	FBh	–
	4SPRP	Set Pointer Region Protection (4-Byte Address)	E3h	–
Individual and Region Protection	IRPRD	IRP Register Read	2Bh	–
	IRPP	IRP Register Program	2Fh	–
	PRRD	Protection Register Read	A7h	–
	PRL	Protection Register Lock (NVLOCK Bit Write)	A6h	–
	PASSRD	Password Read	E7h	–
	PASSP	Password Program	E8h	–
	PASSU	Password Unlock	EAh	–
Reset	RSTEN	Software Reset Enable	66h	–
	RST/RESET	Software Reset	99h	–
	MBR	Mode Bit Reset	FFh	–
Deep Power Down	DPD	Deep Power Down	B9h	B9h
	RES	Release from Deep Power Down / Device ID	ABh	ABh

4.1 Identification Commands

4.1.1 Read Identification (RDID 9Fh)

The S25FL128L, and the S25FL128P, S25FL129P families all support the RDID (9Fh) command, which outputs manufacturer identification and device identification. The S25FL129P family also outputs the JEDEC Common Flash Interface (CFI) after three bytes of identification. Table 5 provides the comparison of the ID field definitions. The S25FL128L family does not output CFI data.

Table 5. Read Identification (RDID 9Fh) Field Definitions

Byte #	Description	S25FL128L	S25FL128P / S25FL129P
0	Manufacturer ID for Cypress	01h	01h
1	Device ID – Memory Interface Type	60h	20h
2	Device ID – Density and Features	18h	18h
3	Extended ID	Undefined	03h/4Dh
4			00h[1] or 01h[2]

4.1.2 Read Quad Identification (RDQID AFh)

The S25FL128L family supports the RDQID (AFh) command, which provides the same information as the RDID (9Fh) command in QPI mode. The S25FL128P and S25FL129P families do not support the RDQID command.

4.1.3 Read Serial Flash Discoverable Parameters (RSFDP 5Ah)

The S25FL128L family supports the RSFDP (5Ah) command, which outputs the Serial Flash Discoverable Parameters (SFDP), defined by JEDEC (JEDEC-216B). The S25FL128P and S25FL129P families do not support SFDP. For details regarding the SFDP byte contents, refer to the S25FL128L datasheets.

[1] Uniform 256KB Sector

[2] Uniform 64KB Sector

4.1.4 Unique Identification (RUID 4Bh)

The S25FL128L family provides a 64-bit unique number for each device via the RUID (4Bh) command. This can be an alternative feature to the Cypress Programmed Random Number supported by the S25FL129P family.

4.2 Status and Configuration Registers

The S25FL128L family and the S25FL129P family both have Status and Configuration registers to report the status of device operations and to configure how the device operates. S25FL128P has only the Status Register. Table 6 summarizes the Status and Configuration Register Set comparison. The S25FL128L family has a nonvolatile and volatile version of each register. During Power-On Reset (POR), hardware reset, or software reset, the device copies the nonvolatile version of a register to the volatile version to provide the default state of the volatile register. For details regarding the nonvolatile and the volatile register functionalities, refer to the S25FL128L family datasheet.

Table 6. Register Set Comparison

Register Name	Register Features	FL128L	FL128P	FL129P
Status Register 1	Reports ready/busy status and controls block protection functions	✓	✓	✓
Status Register 2	Reports erase/program suspend status	✓		
Configuration Register 1	Controls certain interface and block protection functions	✓		✓
Configuration Register 2	Controls certain interface functions	✓		
Configuration Register 3	Controls read commands burst wrap behavior and read latency	✓		

Although the S25FL128L, S25FL128P and S25FL129P families provide the same command codes for reading Status Register 1 and Configuration Register 1, register bits assignments are different. Table 7 shows the at-a-glance comparison of status and configuration register bits assignments. For details of each status or configuration register bit, refer to the device-specific datasheet.

Table 7. Status Register Bits Comparison

Bits	Status Register 1		Status Register 2		Configuration Register 1	
	S25FL128L	S25FL128P S25FL129P	S25FL128L	S25FL128P S25FL129P	S25FL-L	S25FL129P
7	SRP0	SRWD	RFU	N/A	SUS	Not used
6	SEC	P_ERR	E_ERR		CMP	Not used
5	TBPROT	E_ERR	P_ERR		LB3	TBPROT
4	BP2		RFU		LB2	Do Not Use
3	BP1		RFU		LB1	BPNV
2	BP0		RFU		LB0	TBPARM
1	WEL		ES		QUAD	
0	WIP		PS		SRP1	FREEZE

4.3 Read Latency

Some read commands require a read latency to allow time to access the Flash memory array. The read latency cycles are traditionally called dummy cycles. In the S25FL128L family, the number of dummy cycles is configured in the Configuration Register(CR3[3:0]). In the S25FL128P and S25FL129P families, the number of dummy cycles is defined for a specific command.

In the S25FL128L family, the 4-bit wide latency code bits for CR3[3:0] represents the exact number of dummy cycles (except 0000b, which represents 8 dummy cycles). For details of the latency code bits including maximum clock frequency, refer to the S25FL128L datasheet.

In the S25FL128P and S25FL129P families, only a few read commands are defined with fixed dummy cycles as shown in Table 8.

Table 8. Latency Code Bits Map in FL128P and FL128P

	READ	FAST_READ	DOR	QOR	DIOR	QIOR
S25FL128P		1	-	-	–	–
S25FL129P		1	1	1	0	2

4.4 QPI Mode

Legacy SPI commands always send the instruction one-bit wide (serial I/O) on the SI (IO0) signal. The S25FL128L family also supports the QPI mode in which all transfers between the host system and memory are four bits wide on IO0 to IO3, including all instructions. The S25FL128P and S25FL129P families do not support QPI mode. For details about the QPI mode, refer to the S25FL128L family datasheet.

4.5 Double Data Rate (DDR) Read Commands

The S25FL128L family supports Double Data Rate (DDR) commands. The S25FL128P and S25FL129P families do not support DDR commands. For details of the DDR commands, refer to the S25FL128L family datasheet.

4.6 Suspend and Resume

The S25FL128L family supports Erase and Program Suspend and Resume commands. The S25FL128P and S25FL129P families do not support Erase or Program Suspend functions. For details of the Suspend and Resume functions, refer to the S25FL128L family datasheet.

4.7 Software Reset

The S25FL128L family supports Software Reset command (66h, 99h). The S25FL128P and S25FL129P families do not support Software Reset command. For details of the Software Reset command, refer to the S25FL128L family datasheet.

5 Data Protection

5.1 Security Regions

The S25FL128L family and the S25FL129P family both have a “Secure Silicon Region” or “One Time Programmable (OTP) area” that is separated from the main Flash array. S25FL128P does not have this function. The OTP has 1024 bytes in S25FL128L and 506 bytes in S25FL129P. Table 9 shows the feature/parameter comparison between these two device families. The S25FL128L family does not have a Cypress Programmed Random Number in the Security Region, but it has the RUID (4Bh) command that provides a similar functionality.

Table 9. Security Regions Comparison

Feature/Parameter	S25FL128L	S25FL129P
Array Size	1024 Bytes (256 Byte x 4 Regions)	506 Bytes (8-Byte x 2 Regions 16-Byte x 30 Regions 10-Bytes x 1 Region)
Read Array Command	SECRR (48h)	OTPR (4Bh)
Program Array Command	SECRP (42h)	OTPP (42h)
Erase Array Command	SECRE (44h)	Not Supported
Password Protection	Supported	Not Supported
Lock Method	LB3, LB2, LB1, LB0 (CR1NV[5:2]) NVLOCK (PR[0])	Lock Bytes in specific OTP space
Cypress Programmed Random Number	Not Supported	Programmed in ESN

5.2 Deep Power Down

The S25FL128L family and the S25FL128P, S25FL129P families support the Deep Power Down (DPD) command that offers an alternative means of data protection. During DPD, the device ignores all commands, except for the Release from Deep Power Down (RES ABh) command and hardware reset.

5.3 Status Register Protect

The S25FL128L family and the S25FL128P, S25FL129P families have a legacy status register protection method via bit 7 in the Status Register (SRP0 in the S25FL128L and SRWD in the S25FL128P and S25FL129P). The S25FL128L family has an additional SRP1 bit in the Configuration Register 1. The SRP1 adds more flexible and secure functionality to the status register protection.

5.4 Flash Array Protection

The S25FL128L family and the S25FL128P, S25FL129P families have some Flash array protection methods. Subsequent sections summarize the similarities and differences between the device families.

5.4.1 Legacy Block Protection

The S25FL128L family and the S25FL128P, S25FL129P families have the Legacy Block Protection that can protect an address range of the main Flash array from program and erase operations. The S25FL128L family provides more flexibility for the array protection map by additional Status and Configuration Register bits. Table 10 shows the related Status and Configuration Register bits to the Block Protection method of each device family. Note that in the S25FL128L family, Legacy Block Protection is mutually exclusive with the Individual Block Lock (IBL) protection mechanism. The Write Protect Selection (WPS) bit (CR2V[2]) is used for selecting one of the two protection mechanisms.

Table 10. Block Protection Register Bits

Function	S25FL128L	S25FL128P S25FL129P
Block Protection Bit (BPx)	SR1V[4:2] (S25FL128L)	SR1[4:2]
Top or Bottom Protection (TBPROT)	SR1V[6]	TBPROT (CR1[5])[1]
Complement Protection (CMP)	CR1V[6]	-
Sector / Block Protect (SEC)	SR1V[6]	-
Write Protect Selection (WPS)	CR2V[2]	-

5.4.2 Individual and Region Protection (IRP)

The S25FL128L family provides a set of more advanced protection methods, referred to as the “Individual and Region Protection (IRP)”. The IRP provides volatile and nonvolatile sector, block, or region protection methods. For details of the IRP, refer to the S25FL128L datasheet. The S25FL128P and S25FL129P do not provide individual or region protection aside from the legacy BP bits protection method.

6 Hardware Comparison

6.1 Package Compatibility

Table 11 shows the supported packages in the S25FL128L family and S25FL128P, S25FL129P families. S25FL128L does not support the 8-contact WSON (6 x 8 mm) package, while S25FL128P and S25FL129P support them.

Table 11. Package Compatibility

Package Name	S25FL128L	S25FL128P	S25FL129P
8-pin SOIC (208 mil)	✓		
16-pin SOIC (300 mil)	✓	✓	✓
8-Contact WSON (5 × 6 mm)	✓		
8-Contact WSON (6 × 8 mm)		✓	✓

[1] S25FL129P only

Package Name	S25FL128L	S25FL128P	S25FL129P
5 x 5 ball FBGA (6 × 8 mm)	✓		✓
4 x 6 ball FBGA (6 × 8 mm)	✓		✓

6.2 Hold (HOLD#) / IO3

The S25FL128P and S25FL129P families support serial communications hold (stop) through the HOLD# pin. HOLD# is a multiplexed pin. If the Quad bit is enabled, it becomes the IO3 pin. The S25FL128L family does not support the hold functionality; instead, RESET# replaces HOLD# and acts as a hardware reset when CS# is HIGH. RESET# is also multiplexed with IO3 for Quad mode.

6.3 DC Characteristics

Table 12 shows a comparison of the DC parameters for S25FL128L, and S25FL128P, S25FL129P in the industrial plus (–40 °C to +105 °C) temperature range. For details and parameters at other temperature ranges, refer to the datasheets.

Table 12. DC Parameters Comparison

Symbol	Parameter Operating (–40 °C to +105 °C)	S25FL128L			S25FL128P, S25FL129P			Unit
		Min	Typical	Max	Min	Typical	Max	
V_{DD} (min)	V_{DD} (minimum operation voltage)	2.7	–	–	2.7	–	–	V
V_{DD} (cut-off)	V_{DD} (Cut off where reinitialization is needed)	2.4	–	–	2.4	–	–	V
V_{DD} (low)	V_{DD} (low voltage for initialization to occur)	1.0	–	–	0.2[1] 2.3[2]	–	–	V
V_{IL}	Input Low Voltage	–0.5	–	0.3 x V_{CC}	–0.3	–	0.3 x V_{CC}	V
V_{IH}	Input High Voltage	0.7 x V_{CC}	–	V_{CC} + 0.4	0.7 x V_{CC}	–	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	–	–	0.2		–	0.4	V
V_{OH}	Output High Voltage	V_{CC} – 0.2	–		V_{CC} – 0.6	–		V
I_{LI}	Input Leakage Current	–	–	±2	–	–	±2	µA
I_{LO}	Output Leakage Current	–	–	±4	–	–	±2	µA
I_{CC1}	Active Power Supply Current (READ) – Serial SDR@133 MHz	–	30	35	–	–	25[3]	mA
	Active Power Supply Current (READ) – Quad DDR@66 MHz	–	30	35	–	–	–	mA
I_{CC2}	Active Power Supply Current (Page Program)	–	40	50	–	–	26	mA
I_{CC3}	Active Power Supply Current (WRR or WRAR)	–	40	50	–	–	26	mA
I_{CC4}	Active Power Supply Current (SE)	–	40	50	–	–	26	mA
I_{CC5}	Active Power Supply Current (HBE, BE)	–	40	50	–	–	26	mA
I_{SB}	Standby Current (SPI, DIO, QIO)	–	20	35	–	–	200	µA
	Standby Current (QPI)	–	60	100	–	–	–	µA
I_{DPD}	Deep Power Down Current	–	2	20	–	3	20[4] 10[5]	µA
I_{POR}	Power On Reset Current	–	15	30	–	–	–	mA

[1] Initialization to occur at read/standby

[2] Initialization to occur at embedded

[3] At 104MHz

[4] S25FL128P

[5] S25FL129P

6.4 AC Characteristics

Table 13 shows a comparison of the SDR AC parameters for S25FL128L and S25FL128P, S25FL129P in the industrial plus (–40 °C to +105 °C) temperature range. For details and parameters at other temperature ranges, refer to the datasheets.

Table 13. SDR AC Characteristics Comparison

Symbol	Parameter (–40 °C to +105 °C)	S25FL128L		S25FL128P, S25FL129P		Unit
		Min	Max	Min	Max	
$F_{SCK, R}$	SCK Clock Frequency for READ and 4READ instructions	–	50	–	40	MHz
$F_{SCK, C}$	SCK Clock Frequency for dual and quad commands	–	133	–	80[1]	MHz
P_{SCK}	SCK Clock Period	1/ F_{SCK}	–	1/ F_{SCK}	–	ns
t_{WH}, t_{CH}	Clock HIGH Time	50% P_{SCK} ±5%	–	4.5	–	ns
t_{WL}, t_{CL}	Clock LOW Time	50% P_{SCK} ±5%	–	4.5	–	ns
t_{CRT}, t_{CLCH}	Clock Rise Time (slew rate)	0.1	–	0.1	–	V/ns
t_{CFT}, t_{CHCL}	Clock Fall Time (slew rate)	0.1	–	0.1	–	ns
t_{CS}	CS# HIGH Time (Any Read Instructions)	20	–	10	–	ns
	CS# HIGH Time (All other Non-Read instructions)	50	–	50	–	ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3	–	3	–	ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	5	–	3	3000	ns
t_{SU}	Data in Setup Time	3	–	3	–	ns
t_{HD}	Data in Hold Time	2	–	2	–	ns
t_V	Clock LOW to Output Valid	–	8	–	8	ns
t_{HO}	Output Hold Time	1	–	2	–	ns
t_{DIS}	Output Disable Time	–	8	–	8	ns
t_{WPS}	WP# Setup Time	20	–	20	–	ns
t_{WPH}	WP# Hold Time	100	–	100	–	µs
t_{DP}	CS# HIGH to Deep Power Down Mode	–	3	–	3[2] 10[3]	µs
t_{RES}	CS# HIGH to Release from Deep Power Down Mode	–	5	–	30	µs

[1] S25FL129P only

[2] S25FL128P

[3] S25FL129P

6.5 Embedded Algorithms Performance

Table 14 shows a comparison of the program and erase performance for S25FL128L and S25FL128P, S25FL129P. For details of program and Erase performance, refer to the datasheets.

Table 14. Program and Erase Performance Comparison

Symbol	Parameter	S25FL128L			S25FL128P, S25FL129P			Unit
		Min	Typical	Max	Min	Typical	Max	
t_W	Non-volatile Register Write Time	–	145	750	–	–	100[1] 50[2]	ms
t_{PP}	Page Programming (256 Bytes)	–	300	1200	–	1500	3000	µs
t_{SE}	Sector Erase Time (4-KB sectors)	–	50	250	–	200[3]	800[3]	ms
t_{HBE}	Half Block Erase Time (32-KB sectors)	–	190	363	–	–	–	ms
t_{BE}	Block Erase Time (64-KB sectors)	–	270	725	–	500	2000	ms
t_{SE}	Sector Erase Time (256-KB sectors)	–	–	–	–	2	8	sec
t_{CE}	Chip Erase Time	–	70	180	–	128	256	sec

7 Conclusion

The S25FL128L family is serial and multi-I/O command-set and footprint-compatible with the S25FL128P and S25FL129P families. Migration from the S25FL129P or S25FL129P family to the S25FL128L family requires some modifications to accommodate the sector architecture, register set, and data protection methods offered by the S25FL128L family.

8 Related Documents

Table 15. Cypress SPI NOR Flash Product Specific Datasheets

Product Family	Spec Number	Document Title
FL128P Family	002-00646	S25FL128P 128 Mbit 3.0V SPI Flash Memory
FL129P Family	002-00648	S25FL129PS 128 Mbit 3.0V SPI Flash Memory
FL128L Family	002-00124	S25FL256L 256 Mbit, S25FL128L 128 Mbit SPI Flash Memory

[1] S25FL128P

[2] S25FL129P

[3] S25FL129P only

Document History

Document Title: AN221699 – Migration Guide for S25FL128L from S25FL128P or S25FL129P Quad SPI

Document Number: 002-21699

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5995320	ZHFE	12/15/2017	New application note.

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