Migration guide for 45-nm S25HS01GT SEMPER™ flash with Quad SPI from 65-nm S70FS01GS Quad SPI flash (1.8 V)

About this document

Scope and purpose

AN221450 discusses the new features of the S25HS01GT SEMPER™ flash with Quad SPI device and software considerations when migrating from the 65-nm S70FS01GS MCP Quad SPI 1.8 V flash.

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1 Introduction

SEMPER™ flash device, S25HS01GT is a 1.8-V, single-supply flash memory device based on 45-nm advanced MIRRORBIT® technology. This migration guide discusses features of the S25HS01GT device and software considerations when migrating from the S70FS01GS 1.8 V device. This document helps software developers write low-level drivers, setup software, or application software for the S25HS01GT device.

2 Package architecture

2.1 Block diagrams

The S70FS01GS device is a Multi-Chip Package (MCP) with a dual-die stack of two S25FL512S dies (See **Figure 1**). S25HS01GT is a monolithic die (See **Figure 2**).

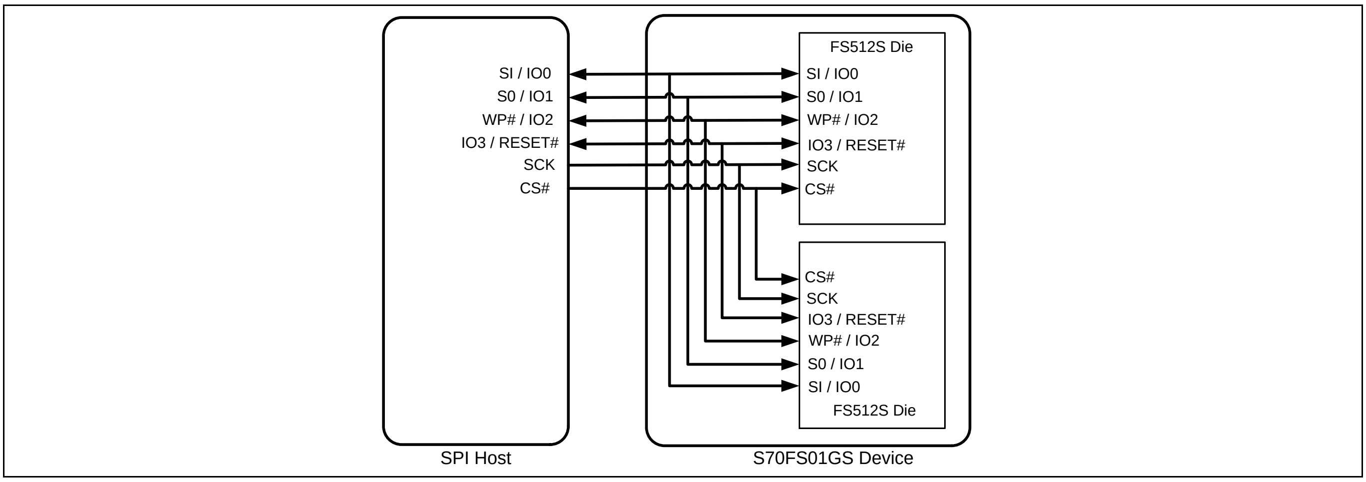

Figure 1 Block diagram S70FS01GS MCP package

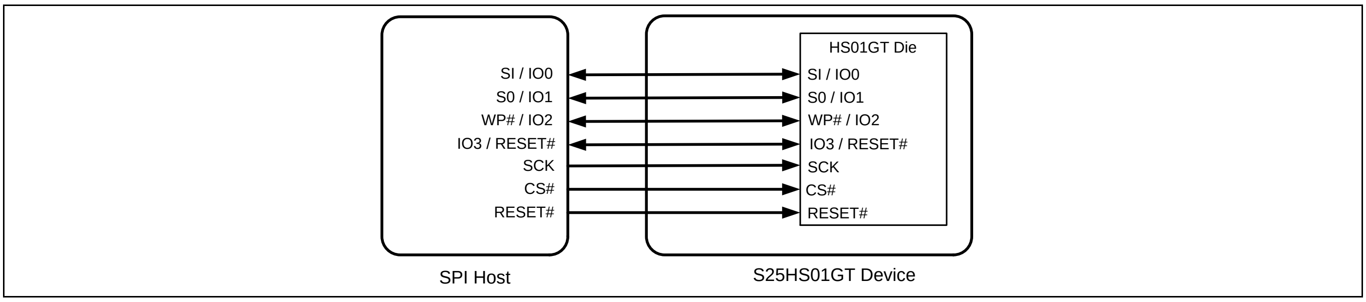

Figure 2 Block diagram S25HS01GT monolithic package

2.2 BGA-24 package

The monolithic S25HS01GT die does not fit into the S70FS01GS' BGA-24 6x8 mm package. The wider BGA-24 8x8 mm package fits the S25HS01GT die with no ball placement or signal assignment changes.

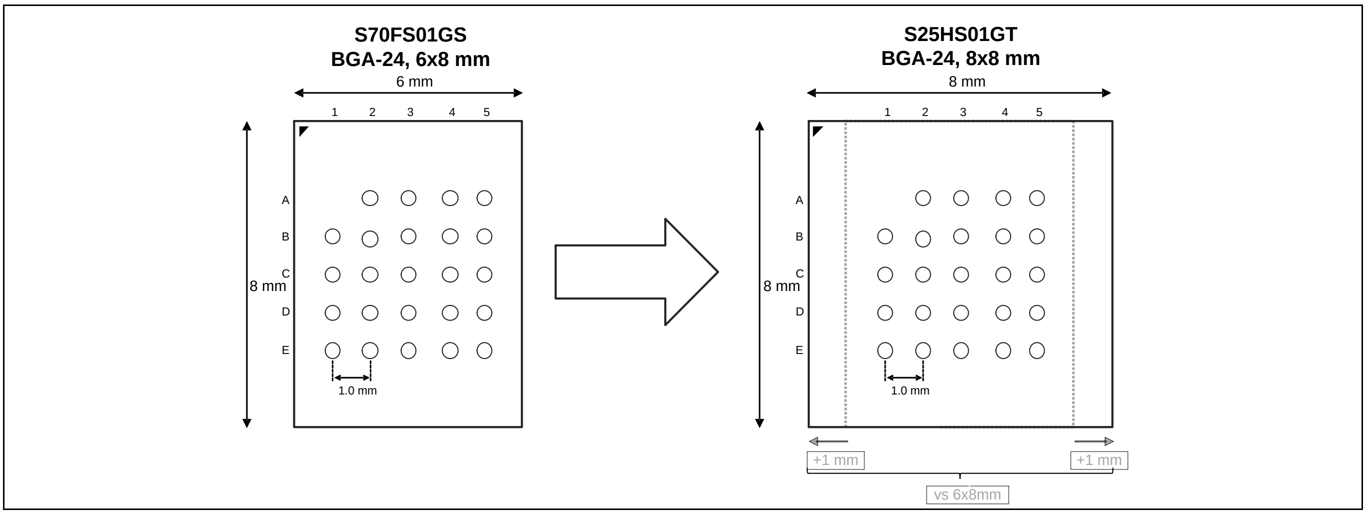

Figure 3 BGA package comparison

3 Sector architecture

The sector architecture in the S25HS01GT device is very flexible. It provides both large "normal" and small "parameter" sectors. Large sectors are 256 KB, and parameter sectors are 4 KB in size. A small set of 32 parameter sectors can be located at the device's lowest (bottom) or highest (top) address or split with 16 parameter sectors, both top and bottom. Parameter sectors can also be removed from the device's address space so that all sectors are uniform in size. The S70FS01GS device provides only eight parameter sectors available at the top or bottom of the memory array.

To erase these two types of sectors (4-KB parameter sectors and 256-KB uniform size sectors), S25HS01GT provides two sets of transactions:

- To erase parameter sectors, use the `ER004_C_0 or ER004_4_0` transaction
- To erase uniform sectors, use the `ER256_C_0 or ER256_4_0` transaction

Configuration Register-1 non-volatile bit 6 (CFR1N[6]) equal to '1' defines the logical location of the parameter sectors; they are split with half at the highest and half at the lowest memory address space. When (CFR1N[6]) is equal to '0', split parameter sectors are disabled, and the logical location of the parameter sectors is selected by CFR1N[2] bit 1.

Configuration Register-1 non-volatile bit 2 (CFR1N[2]) equal to '0' overlays the parameter sectors at the bottom of the lowest address uniform sector. CFR1N[2] equal to '1' overlays parameter sectors at the top of the highest address uniform sector.

There is a configuration option to remove the 4-KB parameter sectors from the address map so that all sectors are a uniform size. Configuration Register-3 non-volatile bit 3 (CFR3N[3]) equal to '0' selects the hybrid sector architecture with 4-KBparameter sectors. TBPRAM bit CFR3N[3]='1' selects the uniform sector architecture without parameter sectors.

The device array configuration needs to be set before any programming of sectors.

Table 1 to **Table 7** show all sector combinations that S25HS010T and S70FL010S devices may have.

Table 1 S25HS01GT sector address map (256-KB uniform sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
256	512	SA00	00000000h-0003FFFFh	Sector starting address — Sector ending address
		:	:	
		SA511	07FC0000h-07FFFFFFh	

Note: Configuration: CFR3N[3]=1.

Table 2 S25HS01GT sector address map (Bottom thirty-two 4-KB sectors and 256-KB uniform sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
4	32	SA00	00000000h-00000FFFh	Sector starting address — Sector ending address
		:	:	
		SA31	0001F000h-0001FFFFh	
128	1	SA32	00020000h-0003FFFFh	
256	511	SA33	00040000h-0007FFFFh	
		:	:	
		SA543	07FC0000h-07FFFFFFh	

Note: Configuration: CFR3N[3]=0, CFR1N[6]=0, CFR1N[2]=0. This is the default configuration.

Table 3 S25HS01GT sector address map (Top thirty-two 4-KB sectors and 256-KB uniform sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
256	511	SA00	0000000h-003FFFFh	Sector starting address — Sector ending address
		:	:	
		SA510	07F80000h-07FBFFFFh	
128	1	SA511	07FC0000h-07FDFFFFh	
4	32	SA512	07FE0000h-07FE0FFFh	
		:	:	
		SA543	07FFF000h-07FFFFFFh	

Note: Configuration: CFR3N[3]=0, CFR1N[6]=0, CFR1N[2]=1.

Table 4 S25HS01GT sector address map (Bottom sixteen and top sixteen 4-KB sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
4	16	SA00	00000000h-0000FFFh	Sector starting address — Sector ending address
		:	:	
		SA15	0000F000h-0000FFFFh	
192	1	SA16	00010000h-0003FFFFh	
256	510	SA17	00040000h-0007FFFFh	
		:	:	
		SA526	07F80000h-07FBFFFFh	
192	1	SA527	07FC0000h-07FEFFFFh	
4	16	SA528	07FF0000h-07FF0FFFh	
		:	:	
		SA543	07FFF000h-07FFFFFFh	

Note: Configuration: CFR3N[3]=0, CFR1N[6]=1.

Table 5 S70FS01GS sector address map (Bottom eight 4-KB sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
4	8	SA00	00000000h-00000FFFh	Sector starting address — Sector ending address
		:	:	
		SA7	00007000h-00007FFFh	
224	1	SA8	00008000h-0003FFFFh	
256	511	SA9	00040000h-0007FFFFh	
		:	:	
		SA519	07FC0000h-07FFFFFFh	

Table 6 S70FS01GS sector address map (Top eight 4-KB sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
256	511	SA00	00000000h-0003FFFFh	Sector starting address — Sector ending address
		:	:	
		SA510	07F80000h-07FBFFFFh	
224	1	SA511	07FC0000h -07FF7FFFh	
4	8	SA512	07FF8000h-07FF8FFFh	
		:	:	
		SA519	07FFF000h-07FFFFFFh	

Table 7 S70FS01GS sector address map (256-KB uniform sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
256	512	SA00	00000000h-0003FFFFh	Sector starting address — Sector ending address
		:	:	
		SA511	07FC0000h-07FFFFFFh	

These tables show the sector architectures of S25HS01GT and S70FS01GS devices. Some of the configurations show a mid-size sector due to memory overlay. You should ensure that the address associated with the Sector Erase command is correct.

Both the S25HS01GT and S70FS01GS devices have an option to enable the blank check feature during an erase. By default, when an erase command is issued, the sector is unconditionally erased. However, suppose the blank check feature is enabled by turning on Bit 5 of Configuration Register 3 (CFR3x[5]). In that case, the device will first check if the last erase was successfully completed on this sector, and the sector is all blank. If so, it returns the successful erase status. This dramatically reduces the erase time. If the blank check finds any '0' values in the array, the erase operation starts immediately.

This blank check feature is handy, especially in the manufacturing environment, where the devices being programmed are often new. However, to ensure that the programming is successful, most manufacturer software will perform an erase regardless. With the blank check feature enabled, the erase time will be improved dramatically while erasing a non-blank sector.

4 Addressing schemes

For devices that are 128 Mb or less, an address length of three bytes is sufficient to address the whole device. For devices that are of higher densities, an address length of four bytes is needed. To accommodate these address length requirements, S25HS01GT and S70FS01GS family devices provide two alternatives:

- A set of transactions that always require a 4-byte address. These transactions can be used to access up to 32 Gb of memory. The transactions include all read transactions, page program transactions, erase transactions, and DYB/PPB protection transactions.
- A 4-byte addressing mode for 3-byte address transactions. This mode is controlled by the AL bit (Bit 7) in Configuration Register 2 (CFR2x[7]). When this bit is set to '1', all standard 3-byte address transactions require 4-byte addressing. The default of this bit is '0', that is, the 3-byte addressing scheme.

Note: When the AL bit is set to 4-byte addressing mode, all standard 3-byte transactions require 4-byte addresses, except RSFDP_3_0 (5Ah). This transaction always uses 3-byte addressing scheme, regardless of the current addressing mode as required by the JEDEC JESD216 (SFDP) standard.

5 Features comparison

S25HS01GT supports a superset of the S70FS01GS feature set.

Table 8 Feature comparison

		S25HS01GT	S70FS01GS
Features	Technology	45-nm MIRRORBIT	65-nm MIRRORBIT
	Density	1 Gb	
	VCC	1.7 V to 2.0 V	
	Temp Range	– 40°C to + 85°C	
		– 40°C to + 105°C	
		– 40°C to + 125°C	
	Data Bus Width	SPI (1-1-1), DIO (1-2-2), QIO (1-4-4), QPI (4-4-4)	
	Erase Sector Size	4 KB/ 256 KB	
	Page Size	256 B / 512 B	
	Burst Read/Wrap	Yes	
	Security Regions	32 x 32 B	
	Cycling endurance	2,560K cycles Endurance flex high endurance	100K Cycles
	Data Retention	25 Years Endurance flex long retention	20 Years
	AutoBoot	Yes	No
	ECC	Yes	
	Data Integrity Check	Yes	No
	Endurance flex	Yes	No
Package	SOIC 8 (208 mil)	No	No
	SOIC 16 (300mil)	Yes	
	BGA (8x6 mm) (5 x 5 Ball)	No	Yes
	BGA (8x8 mm) (5 x 5 Ball)	Yes	No
Options	Reset#	Yes	No
	IO3/Reset#	Yes	
	Legacy Protection BP[x]	Yes	
	Security Protection	ASP	
	Program Suspend / Resume	Yes	
	Erase Suspend / Resume	Yes	
	Parameter Table	SFDP	
	Status Register Protect	Yes	

6 New features S25HS01GT

6.1 Endurance flex architecture (Wear-leveling)

The endurance flex architecture allows partitioning of the main memory array into regions configuring as high-endurance or long-retention. Endurance flex implements wear-leveling in high-endurance regions where program/erase cycles are spread evenly across all sectors, which are part of the wear-leveling pool. This greatly improves the reliability of the device by avoiding premature wear-out of an individual sector.

Architecturally, endurance flex's wear-leveling algorithm is based on the mapping of logical sectors to physical sectors. During the lifetime of the part, this mapping is changed to maintain a uniform distribution of program/erase cycles overall physical sectors. The logical to physical mapping information is stored in a dedicated flash array, which is updated when sectors are swapped. Sector swaps occur when an erase transaction is given.

Endurance flex’s high-endurance region requires a minimum set of 20 sectors. To provide flexibility between configuring long-retention, high-endurance, or both regions, a four-pointer architecture is provided. The factory default setting designates all sectors as high-endurance as part of the wear-leveling pool with all pointers disabled. The four pointers can be used to form a maximum of five regions that can each be configured as either long-retention or high-endurance. These pointers are one-time-programmable and must be configured during the initial device setup.

Data that is frequently updated should be stored in high-endurance partitions to enable the highest number of program/erase cycles and longest device lifespan. Boot code which is infrequently updated should be stored in long-retention partitions to enable highly-reliable 25-year retention.

Note: 4-KB sectors are not part of the endurance flex architecture. Only the main array 256-KB sectors are included.

For detailed definitions of endurance flex, see **Related documents**.

6.2 AutoBoot

SPI devices normally require 32 or more cycles of command and address shifting to initiate a read command. To read the boot code from an SPI device, the host memory controller or processor must supply the read command from a hardwired state machine or from some host processor internal ROM code.

The AutoBoot feature allows the host memory controller to take the boot code from an S25HS01GT family device immediately after the end of reset, without having to send a read command. This saves 32 or more cycles and simplifies the logic needed to initiate the reading of the boot code.

See the S25HS01GT datasheet for a detailed definition of AutoBoot.

6.3 Data Integrity Check

The Data Integrity Check command sequence causes the device to perform a Cyclic Redundancy Check (CRC) calculation over a user-defined address range. The CRC process calculates the check value on the data contained at the starting address through the ending address.

See the S25HS01GT datasheet for a detailed definition of the Data Integrity Check command.

6.4 Sector Erase Count (SEC)

The S25HS01GT device has a new command that allows the software to check the Sector Erase Count. The command outputs the number of erase cycles for the sector with the address specified. Each sector's erase cycle count information is stored in a dedicated flash array on the counters.

See the S25HS01GT datasheet for a detailed definition of the Sector Erase Count command.

6.5 ECC Error Address Trap

A register is provided to capture the data unit address where an ECC error is first encountered while reading the flash array. The Error Lower Address Register and Error Upper Address Register contain the address accessed when the error is detected. The failing bits may not be located at the exact address indicated in the registers but will be located within the aligned 16-byte data unit where the error was detected. Suppose errors are found in multiple data units during a single read operation. In that case, the address of the first failing data unit address is captured in the Error Lower and Upper Address registers.

See the S25HS01GT datasheet for a detailed definition of the ECC Error Address Trap register.

6.6 Error Detection Counter

A counter is provided to keep track of the number of 1-bit or 2-bit errors that occur as data units are read from the flash array. Only errors recognized in the main array will cause the Error Detection counter to increment. The counter will be set to '0' on POR, hardware Reset, or with the ECC Clear command.

See the S25HS01GT datasheet for a detailed definition of the Error Detection Counter.

6.7 SafeBoot

Power-on initialization failure or corrupt registers can render the device unusable. If it is not a catastrophic failure, such as the firmware getting permanently corrupted, it is possible to potentially recover the device. The SafeBoot feature uses the status register polling sequence to detect if there is a Power-on Failure or Register Corruption occurred.

See the S25HS01GT datasheet for a detailed definition of the SafeBoot process.

6.7.1 Power-on detection

During the device initialization process, a failure may occur and make the device unusable. A hardware reset initiated by the master controller (host) can potentially recover the device. S25HS01GT family devices provide a failure signature (0x61) in its status register upon detecting an initialization breakdown. The host must go through a status register polling process to determine if a hardware reset is required to reinitialize the device.

See the S25HS01GT datasheet for a detailed definition of the bootup failure recovery process.

6.7.2 Configuration corruption detection

A WRR or WRAR transaction sequence to non-volatile configuration registers may get interrupted by a brown out or hardware reset; this will corrupt the configuration data. The S25HS01GT family device can detect a corrupted configuration and enter a default mode where the device can be accessed, while providing a configuration corruption signature in its status register. The host can detect this to initiate reprogramming of the non-volatile configuration registers' data.

See the S25HS01GT datasheet for a detailed definition of the configuration corruption detection process.

7 Transaction set comparison

Table 9 summarizes the supported transactions for each device. Pertinent differences will be discussed in subsequent sections. The SEMPER™ flash family has new definitions of transaction names for easier recognition of the transaction operation.

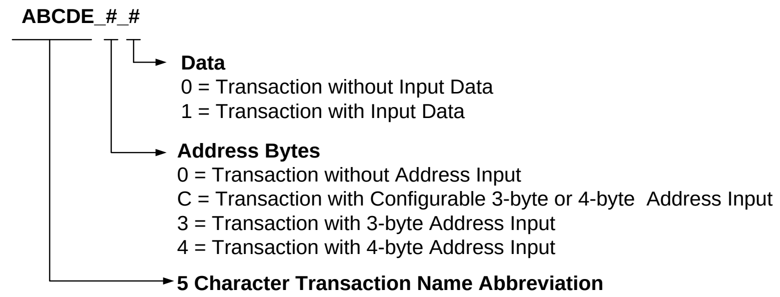

Figure 4 SEMPER™ flash transaction name decoder

Table 9 Transaction set comparison

Function	Transaction name		Description	Command code	
	S25HS01GT	S70FS01GS		S25HS01GT	S70FS01GS
Array Protection	PRASP_0_1	ASPP	Advanced Sector Protection Register Program/Write	2F	N/A
	WRPLB_0_0	PLBWR	PPB Lock Bit Write	A6	
	RDPLB_0_0	PLBRD	PPB Lock Bit Read	A7	
	RDDYB_4_0	4DYBRD	DYB Read (4-Byte)	E0	
	WRDYB_4_1	4DYBWR	DYB Write (4-Byte)	E1	
	RDPPB_4_0	4PPBRD	PPB Read (4-Byte)	E2	
	PRPPB_4_0	4PPBP	PPB Program (4-Byte)	E3	
	ERPPB_0_0	PPBE	PPB Erase / Clear	E4	N/A
	ERPPB_4_0	PPBEA	PPB Erase / Clear Addressed	N/A	EA
	PWDUL_0_1	PASSU1	Password Unlock - 1	E9	
	RDDYB_C_0	DYBRD	DYB Read	FA	
	WRDYB_C_1	DYBWR	DYB Write	FB	
	RDPPB_C_0	PPBRD	PPB Read	FC	
	PRPPB_C_0	PPBP	PPB Program / PPB Write	FD	N/A
	Note[1]	PASSRD	Password Read	N/A	E7
	PGPWD_0_1	PASSP	Password Program / Password Write	E8	
CRC	DICHK_4_1	N/A	Data Integrity Check	5B	N/A
Erase / Program /	SPEPD_0_0	EPCS	Erase / Program / DIC Suspend	75	
	SPEPA_0_0	EPS	Erase / Program Suspend Alternate	85	
				B0	N/A

1 To read the password, use the Read Any Register transaction RDARG_C_0.

Function	Transaction name		Description	Command code	
	S25HS01GT	S70FS01GS		S25HS01GT	S70FS01GS
DIC Suspend / Resume	RSEPD_0_0	EPCR	Erase / Program / DIC Resume	7A	
	RSEPA_0_0	EPR	Erase / Program Resume Alternate	8A	
				30	N/A
Erase Array	ER004_C_0	P4E	Parameter Sector Erase 4 KB	20	
	ER004_4_0	4P4E	Parameter Sector Erase 4 KB (4-Byte)	21	
	SEERC_C_0	N/A	Sector Erase Count	5D	N/A
	ERCHP_0_0	BE	Chip Erase	60	N/A
	ERCHP_0_0	BE	Chip Erase	C7	N/A
	ERCHP_4_0	BE	Chip Erase	N/A	FE
	EVERS_C_0	EES	Evaluate Erase Status	D0	
	ER256_C_0	SE2	Sector Erase 256 KB	D8	
	ER256_4_0	4SE2	Sector Erase 256 KB (4-Byte)	DC	
Identification	RDUID_0_0	N/A	Read Unique Identification Register	4C	N/A
	RSFDP_3_0	RSFDP	Read Memory Discovery Parameters	5A	
	RDIDN_0_0	RDID	Read Identification Register	9F	
	RDQID_0_0	RDQID	Quad Read Identification Register	AF	
Secure Silicon Region	PRSSR_C_1	OTPP	Program Secure Silicon Region	42	
	RDSSR_C_0	OTPR	Read Secure Silicon Region	4B	
Program Array	PRPGE_C_1	PP	Program Page	02	
	PRPGE_4_1	4PP	Program Page (4-Byte)	12	
Read Array	RDAY1_C_0	READ	Read Normal	03	
	RDAY1_4_0	4READ	Read Normal (4-Byte)	13	
	RDAY2_C_0	FAST_READ	Fast Read	0B	
	RDAY2_4_0	4FAST_READ	Fast Read (4-Byte)	0C	
	RDAY3_C_0	DIOR	Read Dual I/O	BB	
	RDAY3_4_0	4DIOR	Read Dual I/O (4-Byte)	BC	
	RDAY4_C_0	N/A	Read Quad Output	6B	N/A
	RDAY4_4_0	N/A	Read Quad Output (4-Byte)	6C	N/A
	RDAY5_C_0	QIOR	Read Quad I/O	EB	
	RDAY5_4_0	4QIOR	Read Quad I/O (4-Byte)	EC	
	RDAY7_C_0	DDRQIOR	Read Double Data Rate Quad I/O	ED	
	RDAY7_4_0	4DDRQIOR	Read Double Data Rate Quad I/O (4-Byte)	EE	

Function	Transaction name		Description	Command code	
	S25HS01GT	S70FS01GS		S25HS01GT	S70FS01GS
Register Access	WRREG_0_1	WRR	Write Register (Status & Configuration)	01	N/A
	WRDIS_0_0	WRDI	Write Disable	04	
	RDSR1_0_0	RDSR1	Read Status Register 1-1	05	N/A
	WRENB_0_0	WREN	Write Enable (Non-volatile)	06	
	RDSR2_0_0	RDSR2	Read Status Register-2	07	N/A
	WRAUB_0_1	N/A	AutoBoot Register Write	15	N/A
	RDECC_4_0	4ECCRD	ECC Read (4-Byte)	18	
	RDECC_C_0	ECCRD	ECC Read	19	
	CLECC_0_0	N/A	Clear ECC Register(s)	1B	N/A
	CLPEF_0_0	CLSR1	Clear Program and Erase Failure Flags	30	
		CLSR2	Clear Program and Erase Failure Flags	82	
	RDCR1_0_0	RDCR1	Read Configuration Register-1	35	
	RDDLP_0_0	DLPRD	Read Data Learning Pattern	41	
	PRDLP_0_1	PNVDLR	Program Data Learning Register	43	N/A
	WRDLP_0_1	WVDLR	Write Data Learning Register	4A	
	WRENV_0_0	N/A	Write Enable (Volatile)	50	N/A
	RDARG_C_0	RDAR	Read Any Register	65	
	WRARG_C_1	WRAR	Write Any Register	71	
	EN4BA_0_0	4BAM	Enter 4-byte Address Mode	B7	
	EX4BA_0_0	N/A	Exit 4-byte Address Mode	B8	N/A
	Note[2]	SWL2	Set Wrap Length	N/A	C0
Reset	SRSTE_0_0	RSTEN	Reset Enable	66	
	SFRST_0_0	RST1	Software Reset	99	
	SFRSL_0_0	RST2	Legacy Software Reset	F0	
DPD	ENDPD_0_0	DPD	Enter Deep Power-Down Mode	B9	
	Note[3]	RES	Release from Deep Power-Down Mode	N/A	AB

2 To Set Wrap Length, use the Write Any Register transaction WRARG_C_1 to write to Configuration Register 4 bits [1:0].
3 To exit Deep Power-Down Mode, toggle CS# LOW.

8 Status and Configuration registers

S25HS01GT and S70FS01GS devices provide many control and customization abilities through a series of Status and Configuration registers. Most of these registers have two versions: non-volatile and volatile. The register value in a non-volatile register will be retained after a power cycle. The register value in a volatile register is reset back to the same value as its non-volatile counterpart upon device power-up, hardware reset, or software reset.

With a volatile version of the registers, you can test settings in the early product development phase before programming the value to the non-volatile registers. Some of the bits in non-volatile registers are One Time Programmable (OTP) bits; thus the changes are not reversible. The volatile version of the registers also allows for overriding the value loaded during reset from the non-volatile register.

This document points out some useful information for software developers. The register in the S25HS01GT device works in the same way as the S70FS01GS device as a monolithic die. On the other hand, there are separate registers for each die in S70FS01GS. See the datasheet for detailed definitions of the Status and Configuration registers.

Table 10 Register set comparison/matching

Register	Type	S25HS01GT	S70FS01GS
Status Register-1	Non-volatile	Yes	Yes
	Volatile	Yes	Yes
Status Register-2	RFU	Yes	Yes
Configuration Register-1	Non-volatile	Yes	Yes
	Volatile	Yes	Yes
Configuration Register-2	Non-volatile	Yes	Yes
	Volatile	Yes	Yes
Configuration Register-3	Non-volatile	Yes	Yes
	Volatile	Yes	Yes
Configuration Register-4	Non-volatile	Yes	Yes
	Volatile	Yes	Yes
Mode Register	Volatile	Yes	No
ECC Status Register	Volatile	Yes	No[4]
ASP Register	RFU	Yes	Yes
Password Register	Non-volatile OTP	Yes	Yes
PPB Lock Register	Volatile	Yes	Yes
PPB Access Register	Non-volatile	Yes	Yes
DYB Access Register	Volatile	Yes	Yes
SPI DDR Data Learning Registers	Non-volatile	Yes	Yes
	Volatile	Yes	Yes
AutoBoot Register	Non-volatile	Yes	No
Data Integrity Check Register	Volatile	Yes	No

4 The ECC Status Register for S25HS01GT has a different function from that of the S70FS01GS Register. S25HS01GT has the ECC Data Unit Status, which has the same function as the S70FS01GS ECC Status Register. See the datasheet for more details.

Register	Type	S25HS01GT	S70FS01GS
SEC Register	Volatile	Yes	No
Address Trap Register	Volatile	Yes	No
Error Detection Counter Register	Volatile	Yes	No
Endurance Flex Pointer Address Registers	OTP	Yes	No

There are two ways to access Status and Configuration registers:

- S70FS01GS and S25HS01GT use Read or Write Any Register commands to access any registers. This allows the address to select the 512-Mb die register to read or write. For S70FS01GS, it is necessary to Read or Write each 512-Mb die registers (see **Table 11**).
  - WRAR (71h) to write to any register
  - RDAR (65h) to read any register
- **S25HS01GT** also uses the traditional method. These commands exist in older SPI devices:
  - Using WRR (01h) to write to SR1NV, and CR1NV
  - Using RDSR1 (05h), RDSR2 (07h), or RDCR (35h) to read SR1V, SR2V, or CR1V

Note: The WRR command writes to the non-volatile version of registers while the read commands read from the volatile version of the registers. When writing to the non-volatile registers, the volatile version will be updated automatically.

Table 11 Register address map

Function	Register type	S25HS01GT		S70FS01GS	
		Volatile component address (Hex)	Non-volatile component address (Hex)	Volatile component address (Hex)	Non-volatile component address (Hex)
Device status	Status Register 1	00800000	00000000	00800000	00000000
	Status Register 2	00800001	N/A	00800001	N/A
Device Configuration	Configuration Register 1	00800002	00000002	00800002	00000002
	Configuration Register 2	00800003	00000003	00800003	00000003
	Configuration Register 3	00800004	00000004	00800004	00000004
	Configuration Register 4	00800005	00000005	00800005	00000005
Endurance Flex Architecture	Endurance Flex Arch. Selection Register 0 [7:0]	N/A	00000050	N/A	N/A
	Endurance Flex Arch. Selection Register 1 [7:0]	N/A	00000052	N/A	N/A
	Endurance Flex Arch. Selection Register 1 [15:8]	N/A	00000053	N/A	N/A

Function	Register type	S25HS01GT		S70FS01GS	
		Volatile component address (Hex)	Non-volatile component address (Hex)	Volatile component address (Hex)	Non-volatile component address (Hex)
	Endurance Flex Arch. Selection Register 2 [7:0]	N/A	00000054	N/A	N/A
	Endurance Flex Arch. Selection Register 2 [15:8]	N/A	00000055	N/A	N/A
	Endurance Flex Arch. Selection Register 3 [7:0]	N/A	00000056	N/A	N/A
	Endurance Flex Arch. Selection Register 3 [15:8]	N/A	00000057	N/A	N/A
	Endurance Flex Arch. Selection Register 4 [7:0]	N/A	00000058	N/A	N/A
	Endurance Flex Arch. Selection Register 4 [15:8]	N/A	00000059	N/A	N/A
Error Correction	ECC Status Register	00800089	N/A	N/A	N/A
	ECC Count Register [7:0]	0080008A	N/A	N/A	N/A
	ECC Count Register [15:8]	0080008B	N/A	N/A	N/A
	ECC Address Trap Register [7:0]	0080008E	N/A	N/A	N/A
	ECC Address Trap Register [15:8]	0080008F	N/A	N/A	N/A
	ECC Address Trap Register [23:16]	00800040	N/A	N/A	N/A
	ECC Address Trap Register [31:24]	00800041	N/A	N/A	N/A
AutoBoot	AutoBoot Register [7:0]	00800042	00000042	N/A	N/A
	AutoBoot Register [15:8]	00800043	00000043	N/A	N/A
	AutoBoot Register [23:16]	00800044	00000044	N/A	N/A
	AutoBoot Register [31:24]	00800045	00000045	N/A	N/A
Data Learning	Data Learning Register [7:0]	00800010	00000010	00800010	00000010

Function	Register type	S25HS01GT		S70FS01GS	
		Volatile component address (Hex)	Non-volatile component address (Hex)	Volatile component address (Hex)	Non-volatile component address (Hex)
	Data Learning Register [15:8]	00800011	00000011	N/A	N/A
Erase Count	Sector Erase Count [7:0]	00800091	N/A	N/A	N/A
	Sector Erase Count [15:8]	00800092	N/A	N/A	N/A
	Sector Erase Count [23:16]	00800093	N/A	N/A	N/A
Data Integrity Check	DIC Register [7:0]	00800095	N/A	N/A	N/A
	DIC Register [15:8]	00800096	N/A	N/A	N/A
	DIC Register [23:16]	00800097	N/A	N/A	N/A
	DIC Register [31:24]	00800098	N/A	N/A	N/A
Protection & Security	Advanced Sector Protection Register [7:0]	N/A	00000030	N/A	00000030
	Advanced Sector Protection Register [15:8]	N/A	00000031	N/A	00000031
	ASP PPB Lock Register (Persistent Protection Block)	0080009B	N/A	00800040	N/A
	ASP Password Register [7:0]	N/A	00000020	N/A	00000020
	ASP Password Register [15:8]	N/A	00000021	N/A	00000021
	ASP Password Register [23:16]	N/A	00000022	N/A	00000022
	ASP Password Register [31:24]	N/A	00000023	N/A	00000023
	ASP Password Register [39:32]	N/A	00000024	N/A	00000024
	ASP Password Register [47:40]	N/A	00000025	N/A	00000025
	ASP Password Register [55:48]	N/A	00000026	N/A	00000026
	ASP Password Register [63:56]	N/A	00000027	N/A	00000027

9 Order of execution

Some bits in the Configuration Register are important to the sector architecture of the device. Ensure that these register bits are set before any program or erase is done to the device. These bits are:

- TB4KBS (Bit 2) in CFR1N[2]: This bit determines where parameter sectors are – bottom or top.
- SP4KBS (Bit 6) in CFR1N[6]: This bit determines whether parameter sectors are split between the bottom and top overrides (Bit2) if set. New feature for S25HS01GT.
- UNHYSA (Bit 3) in CFR3N[3]: This bit determines whether parameter sectors exist in user memory.
- D8h_NV (Bit 1) in CFR3N[3]: This bit is RFU in the S25HS01GT SEMPER™ flash family because it has only 256-KB sectors. On the S70FS01GS device, this bit determines the size of uniform sectors – 64 KB or 256 KB.

If you modify any of these bits after a program operation to the main array, the array's contents are not guaranteed to be present. Therefore, as a best practice, you should configure these bits before accessing the flash array.

Some Status and Configuration register bits can be modified with the same transaction, but some bits have protection interactions with each other. For example, the WRREG_0_1 transaction can write both STR1x and CFRx in one transaction. LBPROT bits are in STR1x[4:2] and the TLPROT bit is in CFR1x[0]. It is recommended that you should first set LBPROT bits in software, then use a separate WRREG_0_1 transaction to set the TLPROT bit to protect LBPROT bits. However, if you issue the new LBPROT bit values and TLPROT bit value in the same transaction, it will still work because the device will act upon the current TLPROT value.

After choosing a device protection mode – Persistent Protection or Password Protection (protection modes are discussed later in this document), CFR1N (except TLPROT and QUADIT), CFR2N, CFR3N, and CFR4N are protected. It is important to note that any modification in these registers must be done before choosing the protection mode.

10 Protection

10.1 Legacy Bit Protection

The Legacy Bit Protection in the S25HS01GT device works the same way as in the S70FS01GS device except there is separate bit protection for each die in S70FS01GS. LBPROT bits protect part or all the flash memory depending on the values.

There are two versions of LBPROT bits. The non-volatile version is in STR1N. The volatile version is in STR1V. When using the `RDSR1_0_0 (05h)` transaction to read, it always reads the STR1V value. If you want to read the non-volatile version of LBPROT bits, use the `RDARG_C_0 (65h)` transaction. The STR1NV value will be returned.

When using the `WRREG_0_1 (01h)` or `WRARG_0_1 (71h)` transaction to write LBPROT bits, depending on the LBPROT non-volatile value (in CFR1V), the transaction writes to LBPROT bits in STR1N or STR1V.

10.2 Advanced Sector Protection (ASP)

There are two ASP modes in the S25HS01GT SEMPER™ flash family: Persistent Protection and Password Protection. You can select one by programing Bit 1 or Bit 2 of the ASP register. Note that these two bits are mutually exclusive. If you try to program both bits to ‘0’, the program transaction will result in an error and the previous setting will be retained.

After one of the modes is selected, most of the bits in Configuration Registers are protected, as mentioned earlier in this document. So, it is important to program all Configuration Registers first before choosing the protection mode.

If the protection mode has not been selected, the device will function as if in Persistent Protection mode. Strongly recommends that you explicitly select the desired mode so that malicious code cannot later change the protection behavior of the device.

11 Quad Peripheral Interface (QPI) operations

S70FS01GS and S25HS01GT support QPI mode in which all information, including the instruction code, is transferred in 4-bit width. In the datasheet, this is referenced as 4-4-4 transaction protocol, as the instruction, address, and data are all transferred in 4-bit width.

To operate in QPI mode, write to the QPI-IT (Bit 6) bit in CFR2x[6].

To try out the QPI mode, use the QPI-IT volatile bit in the CFR2V register. This is the volatile version of the QPI-IT bit; the device will go back to normal mode after reset. Note that once QPI-IT volatile bit is set, the QUADIT bit (Bit 1) in CFR1V[1] will be set automatically. That indicates that all I/O signals are used for information transfer, and the WP# and HOLD# functions are disabled.

When the QPI-IT volatile bit is reset back to ‘0’, the QUADIT bit in CFR1V[1] will remain ‘1’. You must reset it back to ‘0’ if necessary. After the QPI mode has been tested thoroughly, you can set the QPI-IT bit to permanently run the device in QPI mode if required.

Although with the QPI-IT non-volatile bit set, you can still set QPI-IT volatile bit to ‘0 ‘so the device reverts to normal mode; this is not a recommended operation because the device would always revert to QPI after reset.

12 Secured Silicon Region (SSR)

The Secured Silicon Region in S25HS01GT works the same way as in S70FS01GS except that there are separate SSRs for each die in S70FS01GS. The S25HS01GT SEMPER™ flash family provides 1024 bytes of SSR area separated from the main flash array. The area is divided into 32 individually lockable, 32-byte aligned regions. (32 x 32 bytes = 1024 bytes) as a monolithic die, whereas there is separate bit protection for each die in S70FS01GS.

SSR is protected by the TLPROT bit in CFR1V[0]. If TLPROT is set, the SSR program transaction will be ignored. No error is reported.

Region 0 of the SSR (first 32 bytes) is a special region. The first 16 bytes of Region 0 are reserved to program in a Random Number that can be used as a unique device identification; for example, a serial number. The next four bytes are the lock bits. Each lock bit controls the corresponding 32 SSR regions, from Region 0 to Region 31. Any attempt to program to the Random Number area will result in a program error. If an SSR region is locked by its lock bit, any attempt to program into the region will result in a program error.

13 Deep Power-Down mode

S25HS01GT and S70FS01GS both support Deep Power-Down modes. The S25HS01GT device does not use the Release from Deep Power-Down command. Driving CS# LOW will release the S25HS01GT device from the Deep Power-Down mode. Release from Deep Power-Down will take the time duration of t_{RES}.

14 Capacitance characteristics

Symbol	Parameter	S25HS01GT		S70FS01GS		Units
		Min	Max	Min	Max	
C_{IN}	Input Capacitance	–	6.5	–	16	pF
C_{OUT}	Output Capacitance	–	7.5	–	16	pF

15 DC parameters

Table 12 compares the DC parameters of S25HS01GT and S70FS01GS. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all the parameter differences for any potential impact.

Table 12 DC parameter comparison

Symbol	Parameter operating temperature range –40°C to +85°C	S25HS01GT			S70FS01GS			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	1.7	1.8	2.0	1.7	1.8	2.0	V
V_{CC} (min)	V_{CC} (minimum operation voltage)	1.7			1.7			V
V_{CC} (cutoff)	V_{CC} (cutoff where reinitialization is needed)	1.55			1.5			V
V_{CC} (low)	V_{DD} (low voltage for initialization to occur)	0.7			0.7			V
V_{IL}	Input LOW Voltage	V_{CC} x -0.15		V_{CC} x 0.35	–0.5		0.3 x V_{CC}	V
V_{IH}	Input HIGH Voltage	V_{CC} x 0.65		V_{CC} x 1.15	V_{CC} x 0.7		V_{CC} +0.4	V
V_{OL}	Output LOW Voltage			0.2			0.2	V
V_{OH}	Output HIGH Voltage	V_{CC} – 0.2			V_{CC} – 0.2			V
I_{LI}	Input Leakage Current			±2			±4	µA
I_{LO}	Output Leakage Current			±2			±4	µA
I_{CC1}	Active Power Supply Current (READ) – Serial SDR 50 MHz		10	18		18	25	mA
	Active Power Supply Current (READ) – QPI SDR 133 MHz					60	65	mA
	Active Power Supply Current (READ) – QPI SDR 166 MHz		53	69				mA
	Active Power Supply Current (READ) – QPI DDR 80 MHz					70	90	mA
	Active Power Supply Current (READ) – QPI DDR 102 MHz		50	68				mA
I_{CC2}	Active Power Supply Current (Page Program)		50	58		60	100	mA
I_{CC3}	Active Power Supply Current (WRR or WRAR)		50	55		60	100	mA
I_{CC4}	Active Power Supply Current (SE)		50	55		60	100	mA

Symbol	Parameter operating temperature range –40°C to +85°C	S25HS01GT			S70FS01GS			Units
		Min	Typ	Max	Min	Typ	Max	
I_{CC5}	Active Power Supply Current (HBE, BE)		50	55		60	100	mA
I_{SB}	Standby Current		11	113		140	200	µA
I_{DPD}	Deep Power-Down Current		1.3	18		16	120	µA
I_{POR}	Power-On Reset Current			80			160	mA

16 AC parameters

Table 13 and **Table 14** compare the AC parameters of S25HS01GT and S70FS01GS. While most parameter differences should not cause performance issues when migrating, it is recommended that you carefully review all the parameter differences for any potential impact.

Table 13 Single Data Rate (SDR) AC parameter comparison

Symbol	Parameter operating temperature range –40°C to +85°C	S25HS01GT		S70FS01GS		Units
		Min	Max	Min	Max	
f_{SCK} - 1	SCK Clock Frequency for dual and quad commands		166		133	MHz
f_{SCK} - 2	SCK Clock Frequency for READ and 4READ instructions		50		50	MHz
P_{SCK}	SCK Clock Period	1/ f_{SCK}		1/ f_{SCK}		
t_{WH}, t_{CH}	Clock HIGH Time	45% P_{SCK}	55% P_{SCK}	45% P_{SCK}	55% P_{SCK}	ns
t_{WL}, t_{CL}	Clock LOW Time	45% P_{SCK}	55% P_{SCK}	45% P_{SCK}	55% P_{SCK}	ns
t_{CS}	CS# HIGH Time (any Read instructions)	20		10		ns
	CS# HIGH Time (all other non-Read instructions)	50		50		ns
t_{CSS}	CS# Active Setup Time relative to CK ($f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz)	5 / 4		2 / 2		ns
t_{CSH0}	CS# Active Hold Time Mode 0 (relative to CK)	4		3		ns
t_{CSH3}	CS# Active Hold Time Mode 3 (relative to CK)	6		3		ns
t_{SU}	Data in Setup Time ($f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz)	5 / 2		2 / 2		ns
t_{HD}	Data in Hold Time ($f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz))	5 / 2		3 / 3		ns
t_V	Clock LOW to Output Valid (30-pF Loading)	2	8		8	ns
	Clock LOW to Output Valid (15-pF Loading)	2	6		6	ns
t_{HO}	Output Hold Time	1.5		1		ns
t_{DIS}	CS# Inactive to Output Disable Time		8		8	ns
	CS# Inactive to Output Disable Time (When Reset and Quad mode Enabled)		20			ns
t_{DP}	CS# HIGH to Deep Power-Down Mode	10			3	µs
t_{RES}	Release from Deep Power-Down Mode to wakeup		430		30	µs
t_{PU} /t_{RPH}	Reset Time		500		35	µs

Table 14 Double Data Rate (DDR) AC parameter comparison

Symbol	Parameter operating temperature range –40°C to +85°C	S25HS01GT		S70FS01GS		Units
		Min	Max	Min	Max	
f_{SCK} - 1	SCK Clock Frequency		102		80	MHz
P_{SCK}	SCK Clock Period	1/ f_{SCK}		1/ f_{SCK}		
t_{WH}, t_{CH}	Clock HIGH Time	45% P_{SCK}	55% P_{SCK}	45% P_{SCK}	55% P_{SCK}	ns
t_{WL}, t_{CL}	Clock LOW Time	45% P_{SCK}	55% P_{SCK}	45% P_{SCK}	55% P_{SCK}	ns
t_{CS}	CS# HIGH Time (any Read instructions)	10		10		ns
	CS# HIGH Time (all other non-Read instructions)	50		50		ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	5		2		ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	4		3		ns
t_{SU}	Data in Setup Time ($f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz)	5 / 2		1.5		ns
t_{HD}	Data in Hold Time ($f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz)	5 / 1.2		1.5		ns
t_V	Clock LOW to Output Valid (15-pF Loading)	2	6	1.5	6	ns
t_{HO}	Output Hold Time	1.5		1		ns
t_{DIS}	CS# Inactive to Output Disable Time		8		8	ns
	CS# Inactive to Output Disable Time (When Reset and Quad mode Enabled)		20			ns
t_{DP}	CS# HIGH to Deep Power-Down Mode	10			3	µs

17 Embedded algorithm performance

Table 15 compares the embedded algorithm performance parameters of S25HS01GT and S70FS01GS. While most parameter differences should not cause performance issues when migrating, it is recommended that you carefully review all the parameter differences for any potential impact.

Table 15 Embedded algorithm performance parameter comparison

Symbol	Parameter operating temperature range –40°C to +85°C	S25HS01GT			S70FS01GS			Units
			Typ	Max		Typ	Max	
t_W	Non-volatile Register Write Time		44	357.5		240	750	ms
t_{PP}	Page Programming (256 bytes)		480	1700		360	2000	µs
	Page Programming (512 bytes)		570	1700		475	2000	µs
t_{SE}	Sector Erase Time (4-KB parameter sectors)		42-4	335		240	725	ms
	Sector Erase Time (256-KB Long Retention sectors)		773	2677		930	2900	ms
	Sector Erase Time (256-KB High Endurance sectors)		773	5869		-	-	ms
	Bulk Erase Time (1 Gb)		398	1381		440	1440	s

18 Summary

This migration guide is intended as a supplement to the S25HS01GT datasheet. It discusses the new features of the S25HS01GT device and software considerations the designer should make when migrating from the 65-nm S70FS01GS MCP Quad SPI 1.8 V flash to the 45-nm S25HS01GT Monolithic Quad SPI 1.8 V SEMPER™ flash. It describes some important functions in the S25HS01GT SEMPER™ flash device and how to configure and operate the devices.

Related documents

SPI NOR flash documents

[1] **S25HS-T** SEMPER™ with Quad SPI interface flash datasheet

- 002-12345: S25HS256T, S25HS512T, S25HS01GT, 256Mb / 512Mb /1 SEMPER™ flash Quad SPI, 1.8 V/3.0 V

[2] S70FS01GS datasheet

- **002-03833**: S70FS01GS, 1Gbit (128 MByte) FS-S flash, SPI multi-I/O, 1.8 V

[3] **S25FS-S** family datasheet

- **002-00488**: S25FS512S, 512 Mb, FS-S flash, SPI multi-I/O, 1.8 V

[4] AN218550

- 002-18550: Migration guide for 45-nm S25HS-T SEMPER™ flash Quad SPI from 65-nm S25FS-S Quad SPI flash

[5] **AN218481**

- 002-18481: Endurance flex explained – Wear-leveling techniques and usage in SEMPER™ flash devices

Revision history

Document version	Date of release	Description of changes
**	2018-09-25	New application note.
*A	2019-06-13	Updated AC Specification.
*B	2021-03-16	Updated to Infineon template.
*C	2022-08-03	Updated the following: • Enduraflex to Endurance flex • Cypress to Infineon • Mirrorbit™ to MIRRORBIT™; Corrected Transaction names: RDAYx_C_0, RDAYx_4_0, PRDLP_0_1, WRENV_0_0. Added S25HS01GT datasheet link. Corrected AC parameters: DDR - t_V from 2.0 to 1.5nS, t_{HO} from 1.0 to 1.5nS, t_{SE} from 44 to 42mS, t_{CSH0} from 4 to 3nS; SDR - t_{CS} from 20 to 10nS, t_{HO} from 1.0 to 1.5nS. Removed "Typ" columns from **Table 13** and **Table 14**.

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