Migration guide for 45-nm S25HL01GT SEMPER™ flash with Quad SPI from 65-nm S70FL01GS Quad SPI flash

About this document

Scope and purpose

AN221389 provides the new features of the monolithic S25HL01GT SEMPER™ flash with Quad SPI 3.0 V and software considerations when migrating from the multi-chip package (MCP) Infineon 65-nm S70FL01GS Quad SPI 3.0 V flash.

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1 Introduction

Infineon S25HL01GT SEMPER™ flash with Quad SPI device is a 3.0 V, single-supply flash memory device based on 45-nm advanced MIRRORBIT™ technology. This migration guide discusses features of the S25HL01GT device and software considerations when migrating from the MCP S70FL01GS device. This document helps software developers write low-level drivers, setup software, or application software for the S25HL01GT device.

2 Package architecture

2.1 Block diagrams

The S70FL01GS device is an MCP with a dual-die stack of two S25FL512S dies (see **Figure 1**). S25HL01GT is a monolithic die (see **Figure 2**). When migrating from S70FL01GS to S25HL01GT, consider the following:

- The two CS# pins of S70FL01GS are reduced to a single CS# pin in S25HL01GT.
- The HOLD pin and feature are not supported on S25HL01GT.
- S25HL01GT has a new feature of muxing the RESET# with the IO3 on the same pin.

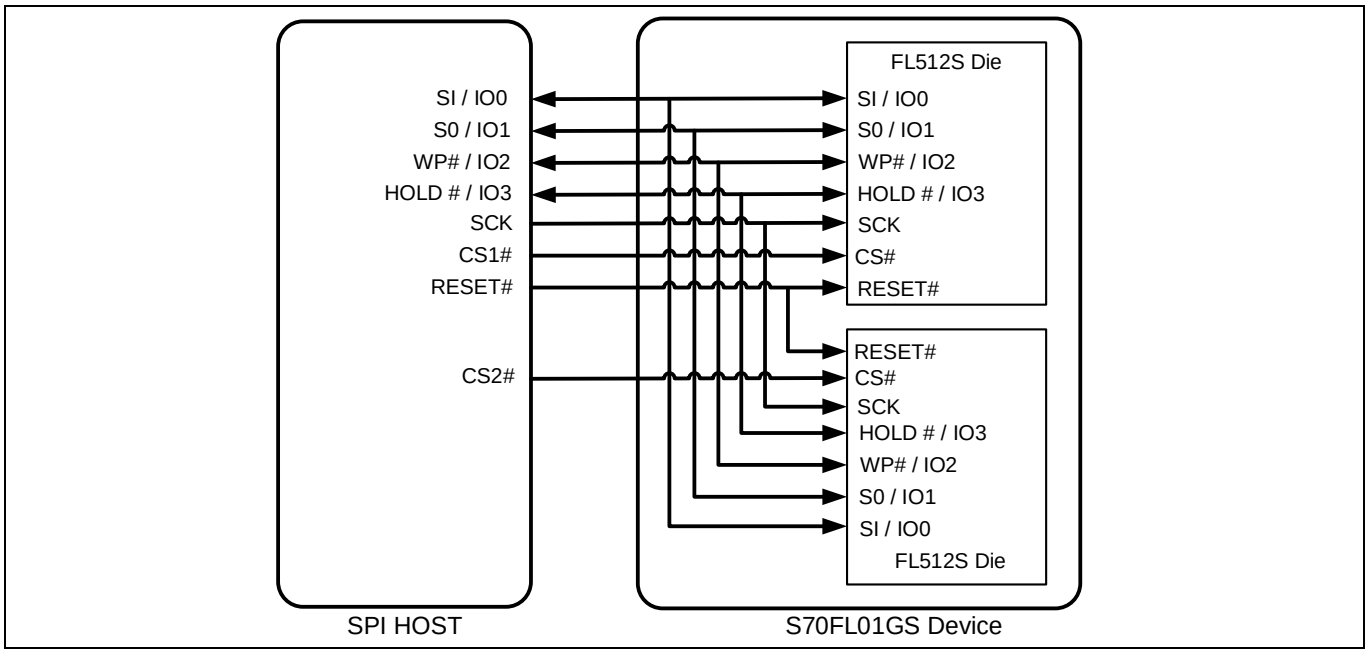

Figure 1 Block diagram of S70FL01GS MCP package

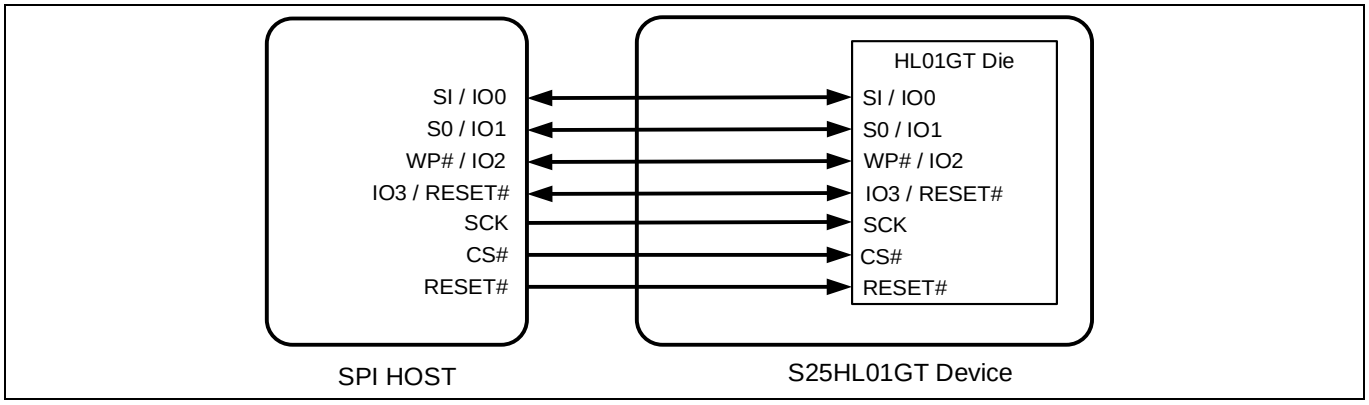

Figure 2 Block diagram of S25HL01GT monolithic package

Note: When migrating from S70FL01GS to S25HL01GT, the two CS# pins of S70FL01GS are reduced to a single CS# pin in S25HL01GT.

2.2 BGA-24 package

The monolithic S25HL01GT die does not fit into the BGA-24 6x8 mm package that is supported by S70FL01GS. The wider BGA-24 8x8 mm package will fit the S25HL01GT die with no changes to ball placement.

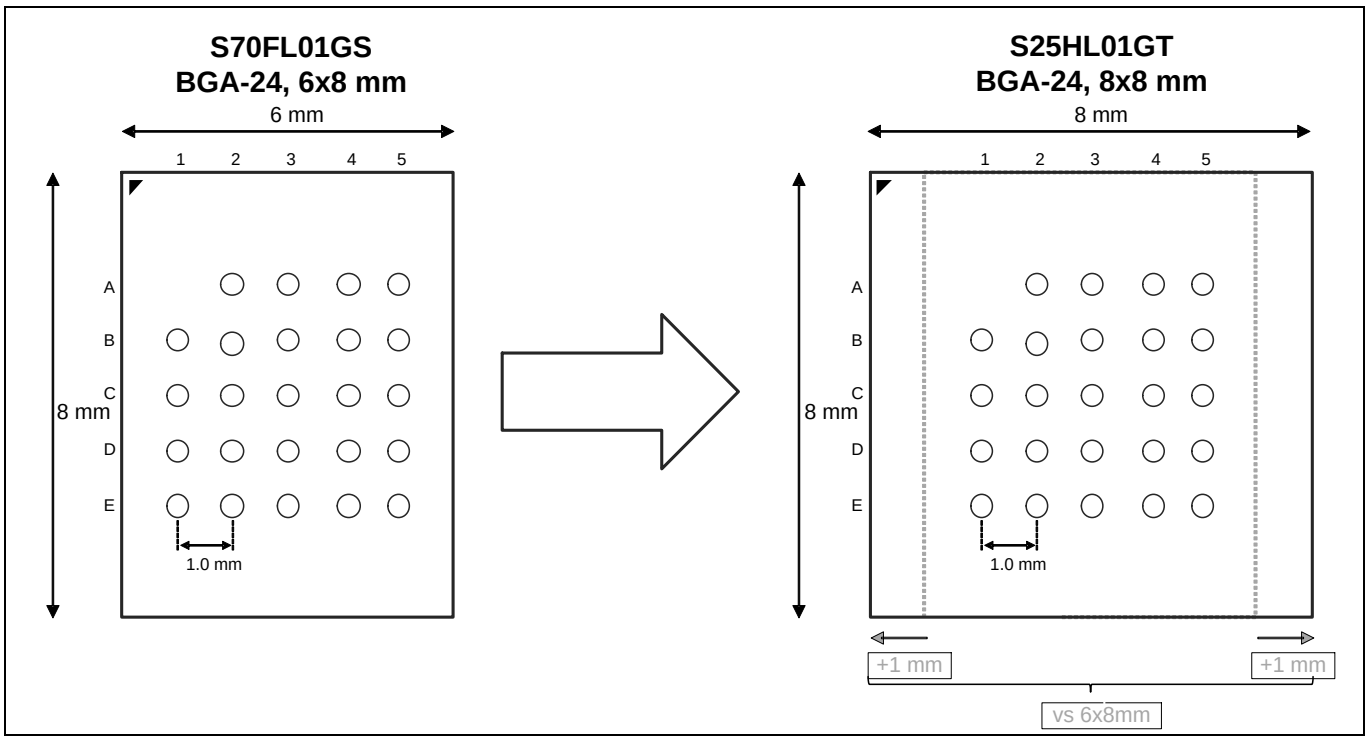

Figure 3 BGA package comparison

3 Sector architecture

S25HL01GT has a flexible sector architecture, which provides both large “normal” sectors and small “parameter” sectors. Large sectors are 256 KB and parameter sectors are 4 KB in size. A small set of 32 parameter sectors can be located at the lowest (bottom) or highest (top) address of a device or split with 16 parameter sectors both top and bottom. Parameter sectors can also be removed from the address space of the device so that all sectors are uniform in size. S70FL01GS supports only uniform 256-KB sectors.

To erase these two types of sectors (4-KB parameter sectors and 256-KB uniform size sectors), S25HL01GT provides two sets of transactions: To erase parameter sectors, use the ER004_C_0 or ER004_4_0 transaction. To erase uniform sectors, use the ER256_C_0 or ER256_4_0 transaction.

Configuration Register-1 non-volatile bit 6 (CFR1N[6]) equal to ‘1’ defines the logical location of the parameter sectors; they are split with half at the highest and half at the lowest memory address space. When (CFR1N[6]) is equal to ‘0’, split parameter sectors are disabled and the logical location of the parameter sectors is selected by CFR1N[2].

Configuration Register-1 non-volatile bit 2 (CFR1N[2]) equal to ‘0’ overlays the parameter sectors at the bottom of the lowest address uniform sector. CFR1N[2] equal to ‘1’ overlays parameter sectors at the top of the highest address uniform sector.

There is a configuration option to remove 4-KB parameter sectors from the address map so that all sectors are uniform size. Configuration Register-3 non-volatile bit 3 (CFR3N[3]) equal to ‘0’ selects the hybrid sector architecture with 4-KB- parameter sectors. TBPRAM bit CFR3N[3]=’1’ selects the uniform sector architecture without parameter sectors.

The device array configuration needs to be set before any programming of sectors.

Table 1 to **Table 5** show all sector combinations that S25HL01GT and S70FL01GS devices may have. The device array configuration needs to be set before any programming of sectors.

Table 1 S70FL01GS sector address map (256KB uniform sectors)

Die	Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
Die 1	256	256	SA00	00000000h-0003FFFFh	Sector starting address
			:	:	—
			SA255	03FC0000h-03FFFFFFh	Sector ending address
Die 2	256	256	SA00	00000000h-0003FFFFh	Sector starting address
			:	:	—
			SA255	03FC0000h-03FFFFFFh	Sector ending address

Sector architecture

Table 2 S25HL01GT sector address map (256KB uniform sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
256	512	SA00	00000000h-0003FFFFh	Sector starting address — Sector ending address
		:	:	
		SA511	07FC0000h-07FFFFFFh	

Note: Configuration: CFR3N[3]=1.

Table 3 S25HL01GT sector address map (Bottom thirty-two 4-KB sectors and 256-KB uniform sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
4	32	SA00	00000000h-00000FFFh	Sector starting address — Sector ending address
		:	:	
		SA31	0001F000h-0001FFFFh	
128	1	SA32	00020000h-0003FFFFh	
256	511	SA33	00040000h-0007FFFFh	
		:	:	
		SA543	07FC0000h-07FFFFFFh	

Note: Configuration: CFR3N[3]=0, CFR1N[6]=0, CFR1N[2]=0. This is the default configuration.

Table 4 S25HL01GT sector address map (Top thirty-two 4-KB sectors and 256-KB uniform sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
256	511	SA00	0000000h-003FFFFh	Sector starting address — Sector ending address
		:	:	
		SA510	07F80000h-07FBFFFFh	
128	1	SA511	07FC0000h-07FDFFFFh	
4	32	SA512	07FE0000h-07FE0FFFh	

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
		:	:	
		SA543	07FFF000h-07FFFFFFh	

Note: Configuration: CFR3N[3]=0, CFR1N[6]=0, CFR1NV[2]=1.

Table 5 S25HL01GT sector address map (Bottom sixteen and top sixteen 4-KB sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
4	16	SA00	00000000h-00000FFFh	Sector starting address — Sector ending address
		:	:	
		SA15	0000F000h-0000FFFFh	
192	1	SA16	00010000h-0003FFFFh	
256	510	SA17	00040000h-0007FFFFh	
		:	:	
		SA526	07F80000h-07FBFFFFh	
192	1	SA527	07FC0000h-07FEFFFFh	
4	16	SA528	07FF0000h-07FF0FFFh	
		:	:	
		SA543	07FFF000h-07FFFFFFh	

Note: Configuration: CFR3N[3]=0, CFR1N[6]=1.

These tables show the sector architectures of S25HL01GT and S70FL01GS devices. Some of the configurations show a mid-size sector due to memory overlay. You should ensure that the address associated with the Sector Erase command is correct.

Sector architecture

In S25HL01GT, you have an option to enable the blank check feature during an erase. By default, when an erase command is issued, the sector is unconditionally erased. However, if the blank check feature is enabled, by turning on Bit 5 of Configuration Register 3 (CFR3x[5]), the device will first check if the last erase was successfully completed on this sector and the sector is all blank. If so, it returns the successful erase status. This dramatically reduces the erase time. If the blank check finds any '0' values in the array, the erase operation starts immediately.

This blank check feature is very useful, especially in the manufacturing environment where most often the devices being programmed are new. However, to ensure that programming is successful, most manufacturer software will perform an erase regardless. With the blank check feature enabled, the erase time will be improved dramatically when the device is new while erasing the sector properly when it encounters a non-blank sector.

4 Addressing schemes

For devices that are 128 Mb or less, an address length of 3 bytes is sufficient to address the whole device. For devices that are of higher densities, an address length of 4 bytes is needed. To accommodate these different address length requirements, S25HL01GT provides two alternatives:

- A set of transactions that always require a 4-byte address. These transactions can be used to access up to 32 Gb of memory. These transactions include all read commands, page program commands, erase transactions, and DYB/PPB protection transactions.
- The RSFDP_3_0 (5Ah) transaction always uses 3-byte addressing scheme regardless of the current addressing mode as required by the JEDEC JESD216 (SFDP) standard.

5 Features comparison

S25HL01GT supports a superset of the S70FL01GS feature set.

Table 6 Feature comparison

		S25HL01GT	S70FL01GS
Features	Technology	45-nm MIRRORBIT™	65-nm MIRRORBIT™
	Density	1 Gb	
	V_{CC}	2.7 V to 3.6 V, no V_{IO} option	2.7 V to 3.6 V/1.65 V to 3.6 V V_{IO}
	Temp range	– 40°C to + 85°C	
		– 40°C to + 105°C	
		– 40°C to + 125°C	
	Data bus width	SPI (x1), DIO (x2), QIO (x4), QPI	SPI (x1), DIO (x2), QIO (x4)
	Erase sector size	4 KB/256 KB	256 KB
	Page size	256 B/512 B	
	Burst read/wrap	Yes	
	Security regions	32 x 32 B	
	Cycling endurance	2,560-k cycles. Endurance flex high-endurance	100-k cycles
	Data retention	25 Years. Endurance flex long retention	20 years
	AutoBoot	Yes	
	ECC	Yes	
	Data integrity check	Yes	No
	Endurance flex	Yes	No
Package	SOIC 8 (208 mil)	No	
	SOIC 16 (300mil)	Yes	
	BGA (8x6 mm) (5 x 5 ball)	No	Yes
	BGA (8x8 mm) (5 x 5 ball)	Yes	No
Options	Reset#	Yes	
	IO3/Reset#	Yes	No
	Legacy protection BP[x]	Yes	
	Security protection	ASP	
	Program suspend/resume	Yes	
	Erase suspend/resume	Yes	
	Parameter table	SFDP	
	Status register protect	Yes	

6 New features S25HL01GT

6.1 Endurance flex architecture (Wear-leveling)

The endurance flex architecture allows partitioning of the main memory array into regions that can be configured as either high-endurance or long-retention. Endurance flex implements wear-leveling in high-endurance regions where program/erase cycles are spread evenly across all sectors, which are part of the wear-leveling pool. This greatly improves the reliability of the device by avoiding premature wear-out of an individual sector.

Architecturally, endurance flex's wear-leveling algorithm is based on a mapping of logical sectors to physical sectors. During the lifetime of the part, this mapping is changed to maintain a uniform distribution of program/erase cycles over all physical sectors. The logical-to-physical mapping information is stored in a dedicated flash array, which is updated when sectors are swapped. Sector swaps occur when an erase transaction is given.

Endurance flex’s high-endurance region requires a minimum set of 20 sectors. To provide flexibility between configuring long-retention, high-endurance, or both regions, a four-pointer architecture is provided. The factory default setting designates all sectors as high-endurance as part of the wear-leveling pool with all pointers disabled. The four pointers can be used to form a maximum of five regions that can each be configured as either long-retention or high-endurance. The pointers are one-time-programmable and must be configured during the initial device setup.

Data that is frequently updated should be stored in high-endurance partitions to enable the highest number of program/erase cycles and longest device lifespan. Boot code which is infrequently updated should be stored in long-retention partitions to enable highly-reliable 25-year retention.

Note: *4-KB sectors are not part of the endurance flex architecture. Only the main array 256-KB sectors are included.*

For detailed definitions of endurance flex, see Related documentsRelated documentsRelated documents.

6.2 Sector Erase Count (SEC)

S25HL01GT has a new command that allows the software to check the Sector Erase Count. The command outputs the number of erase cycles for the sector with the address specified. Each sector’s erase cycle count information is stored in the counters in a dedicated flash array.

See the datasheet for a detailed definition of the Sector Erase Count command.

6.3 ECC Error Address Trap

A register is provided to capture the data unit address where an ECC error is first encountered during a read of the flash array. The Error Lower Address Register and Error Upper Address Register contain the address that was accessed when the error is detected. The failing bits may not be located at the exact address indicated in the registers but will be located within the aligned 16-byte data unit where the error was detected. If errors are found in multiple data units during a single read operation, the address of the first failing data unit address is captured in the Error Lower and Upper Address registers.

See the datasheet for a detailed definition of the ECC Error Address Trap register.

6.4 Error Detection Counter

A counter is provided to keep track of the number of 1-bit or 2-bit errors that occur as data units are read from the flash array. Only errors recognized in the main array will cause the Error Detection Counter to increment. The counter will be set to '0' on POR, hardware reset, or with the ECC Clear command.

See the datasheet for a detailed definition of the Error Detection Counter.

6.5 SafeBoot

Power-on initialization failure or corrupt registers can render the device unusable. If it is not a catastrophic failure, such as the firmware getting permanently corrupted, it is possible to potentially recover the device. The SafeBoot feature uses the status register polling sequence to detect if there is a Power-On Failure or Register Corruption occurred.

See the datasheet for a detailed definition of the SafeBoot process.

6.5.1 Power On Detection

During the device initialization process, a failure may occur and make the device unusable. A hardware reset initiated by the master controller (host) can potentially recover the device. S25HL01GT family devices provide a failure signature (0x61) in its status register upon detecting an initialization breakdown. The host must go through a status register polling process to determine if a hardware reset is required to reinitialize the device.

See the datasheet for a detailed definition of the bootup failure recovery process.

6.5.2 Configuration corruption detection

A WRR or WRAR transaction sequence to non-volatile configuration registers may get interrupted by a brown out or hardware reset; this will corrupt the configuration data. S25HL01GT can detect a corrupted configuration and enter a default mode where the device can be accessed, while providing a configuration corruption signature in its status register. The host can detect this to initiate reprogramming of the non-volatile configuration registers' data.

See the datasheet for a detailed definition of the configuration corruption detection process.

6.6 Deep Power-Down mode

S25HL01GT supports Deep Power-Down mode and does not use the Release from Deep Power-Down command. Driving CS# LOW will release S25HL01GT from the Deep Power-Down mode. Release from Deep Power-Down will take the time duration of t_{RES}.

7 Transaction set comparison

Table 7 summarizes the supported transactions for each device. Pertinent differences will be discussed in subsequent sections. The SEMPER™ Flash family has new definitions of transaction names for easier recognition of the transaction operation.

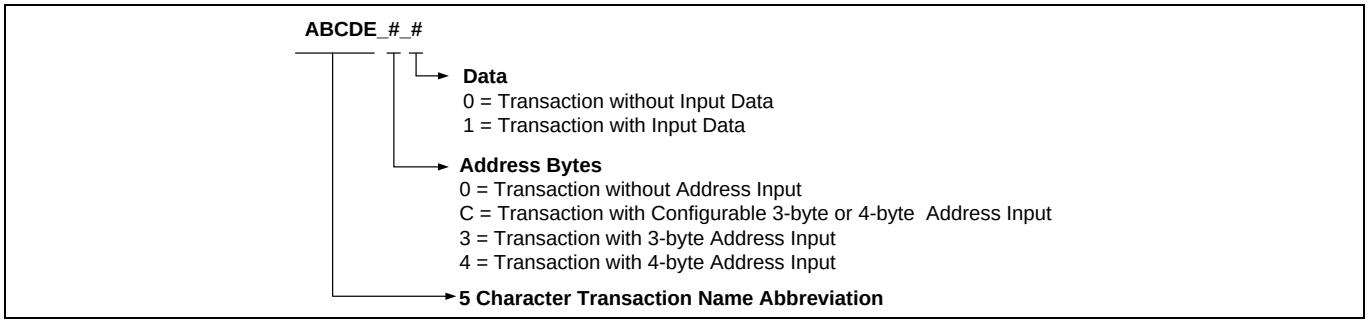

Figure 4 SEMPER™ flash transaction name decoder

Table 7 Transaction set comparison

Function	Transaction name		Description	Command code	
	S25HL01GT	S70FL01GS		S25HL01GT	S70FL01GS
Array protection	PRASP_0_1	ASPP	Advanced Sector Protection Register Program/Write	2F	N/A
	WRPLB_0_0	PLBWR	PPB Lock Bit Write	A6	
	RDPLB_0_0	PLBRD	PPB Lock Bit Read	A7	
	RDDYB_4_0	4DYBRD	DYB Read (4-Byte)	E0	
	WRDYB_4_1	4DYBWR	DYB Write (4-Byte)	E1	
	RDPPB_4_0	4PPBRD	PPB Read (4-Byte)	E2	
	PRPPB_4_0	4PPBP	PPB Program (4-Byte)	E3	
	ERPPB_0_0	PPBE	PPB Erase / Clear	E4	
	PWDUL_0_1	PASSU	Password Unlock	E9	
	RDDYB_C_0	DYBRD	DYB Read	FA	N/A
	WRDYB_C_1	DYBWR	DYB Write	FB	N/A
	RDPPB_C_0	PPBRD	PPB Read	FC	N/A
	PRPPB_C_0	PPBP	PPB Program / PPB Write	FD	N/A
	Note[1]	PASSRD	Password Read	N/A	E7
	PGPWD_0_1	PASSP	Password Program / Password Write	E8	
CRC	DICHK_4_1	N/A	Data Integrity Check	5B	N/A
Erase / Pprogram/DIC suspend/resume	SPEPD_0_0	EPCS	Erase / Program / DIC Suspend	75	75[2]
	SPEPA_0_0	EPS	Erase / Program Suspend Alternate	85	85[3]
				B0	N/A
	RSEPD_0_0	EPCR	Erase / Program / DIC Resume	7A	7A[4]

1 To read the password, use the Read Any Register transaction RDARG_C_0.

2 Erase Suspend only.

3 Program Suspend only.

4 Erase Resume only.

Transaction set comparison

Function	Transaction name		Description	Command code	
	S25HL01GT	S70FL01GS		S25HL01GT	S70FL01GS
	RSEPA_0_0	EPR	Erase / Program Resume Alternate	8A	8A[5]
				30	N/A
Erase array	ER004_C_0	P4E	Parameter Sector Erase 4 KB	20	N/A
	ER004_4_0	4P4E	Parameter Sector Erase 4 KB (4-Byte)	21	N/A
	SEERC_C_0	N/A	Sector Erase Count	5D	N/A
	ERCHP_0_0	BE	Chip Erase	60	
	ERCHP_0_0	BE	Chip Erase	C7	
	EVERS_C_0	EES	Evaluate Erase Status	D0	N/A
	ER256_C_0	SE2	Sector Erase 256 KB	D8	
	ER256_4_0	4SE2	Sector Erase 256 KB (4-Byte)	DC	
Identification	RDUID_0_0	N/A	Read Unique Identification Register	4C	N/A
	RSFDP_3_0	RSFDP	Read Memory Discovery Parameters	5A	
	RDIDN_0_0	RDID	Read Identification Register	9F	
	RDQID_0_0	RDQID	Quad Read Identification Register	AF	N/A
Secure silicon region	PRSSR_C_1	OTPP	Program Secure Silicon Region	42	
	RDSSR_C_0	OTPR	Read Secure Silicon Region	4B	
Program array	PRPGE_C_1	PP	Program Page	02	
	PRPGE_4_1	4PP	Program Page (4-Byte)	12	
	N/A	PP	Program Page	N/A	32
	N/A	4PP	Program Page (4-Byte)	N/A	38
Read array	RDAY1_C_0	READ	Read Normal	03	
	RDAY1_4_0	4READ	Read Normal (4-Byte)	13	
	RDAY2_C_0	FAST_READ	Fast Read	0B	
	RDAY2_4_0	4FAST_READ	Fast Read (4-Byte)	0C	
	N/A	DDRFR	DDR Fast Read	N/A	0D
	N/A	4DDRFR	DDR Fast Read (4-Byte)	N/A	0E
	RDAY4_C_0	DIOR	Read Dual I/O	6B	
	RDAY4_4_0	4DIOR	Read Dual I/O (4-Byte)	6C	
	N/A	DDRDIOR	DDR Read Dual I/O	N/A	BD
	N/A	4DDRDIOR	DDR Read Dual I/O (4-Byte)	N/A	BE
	RDAY2_C_0	QOR	Read Quad Output	0B	
	RDAY2_4_0	4QOR	Read Quad Output (4-Byte)	0C	
	RDAY5_C_0	QIOR	Read Quad I/O	EB	
	RDAY5_4_0	4QIOR	Read Quad I/O (4-Byte)	EC	
	RDAY7_C_0	DDRQIOR	Read Double Data Rate Quad I/O	ED	
	RDAY7_4_0	4DDRQIOR	Read Double Data Rate Quad I/O (4-Byte)	EE	
Register access	WRREG_0_1	WRR	Write Register (Status & Configuration)	01	
	WRDIS_0_0	WRDI	Write Disable	04	
	RDSR1_0_0	RDSR1	Read Status Register 1-1	05	
	WRENB_0_0	WREN	Write Enable (Non-volatile)	06	

5 Program Resume only

Transaction set comparison

Function	Transaction name		Description	Command code	
	S25HL01GT	S70FL01GS		S25HL01GT	S70FL01GS
	RDSR2_0_0	RDSR2	Read Status Register-2	07	
	[6]	ABRD	AutoBoot Register Read	N/A	14
	WRAUB_0_1	ABWR	AutoBoot Register Write	15	
	RDECC_4_0	4ECCRD	ECC Read (4-Byte) Data Unit	18	
	RDECC_C_0	N/A	ECC Read Data Unit	19	N/A
	CLECC_0_0	N/A	Clear ECC Register(s)	1B	N/A
	CLPEF_0_0	CLSR1	Clear Program and Erase Failure Flags	30	
		CLSR2	Clear Program and Erase Failure Flags	82	N/A
	RDCR1_0_0	RDCR1	Read Configuration Register-1	35	
	RDDLP_0_0	DLPRD	Read Data Learning Pattern	41	
	PRDLP_0_1	PNVDLR	Program Data Learning Register	43	
	WRDLP_0_1	WVDLR	Write Data Learning Register	4A	
	WRENV_0_0	N/A	Write Enable (Volatile)	50	N/A
	RDARG_C_0	RDAR	Read Any Register	65	N/A
	WRARG_C_1	WRAR	Write any Register	71	N/A
	EN4BA_0_0	4BAM	Enter 4-byte address mode	B7	N/A
	EX4BA_0_0	N/A	Exit 4-byte address mode	B8	N/A
	Note[7]	SWL2	Set Wrap Length	N/A	C0
	N/A[8]	BRRD	Bank Register Read	N/A	16
	N/A	BRWR	Bank Register Write	N/A	17
Reset	SRSTE_0_0	RSTEN	Reset Enable	66	
	SFRST_0_0	RST1	Software Reset	99	
	SFRSL_0_0	RST2	Legacy Software Reset	F0	
DPD	ENDPD_0_0	N/A	Enter Deep Power-Down Mode	B[9]	N/A

6 Use Read Any Register transaction to read AutoBoot register.

7 To Set Wrap Length, use the Write Any Register transaction WRARG_C_1 to write to Configuration Register 4 bits [1:0].

8 Bank Addressing not supported.

9 To exit Deep Power-Down Mode, toggle CS# low.

8 Status and Configuration registers

S25HL01GT and S70FL01GS devices provide many control and customization abilities to users through a series of Status and Configuration registers. Most of these registers have two versions: non-volatile and volatile. The register value in a non-volatile register will be retained after a power cycle. The register value in a volatile register is reset back to the same value as its non-volatile counterpart upon device power up, hardware reset, or software reset.

The existence of a volatile version of the registers provides users the ability to test settings in the early product development phase before programming the value to the non-volatile registers. Some of the bits in non-volatile registers are one-time programmable (OTP) bits, thus the changes are not reversible. The volatile version of the registers also allows for overriding the value loaded during reset from the non-volatile register.

The detailed definitions of the Status and Configuration registers can be found in the datasheet. This document points out some useful information for software developers.

Table 8 Register set comparison/matching

Register	Type	S25HL01GT	S70FL01GS
Status Register-1	Non-volatile	Yes	No
	Volatile	Yes	Yes
Status Register-2	Volatile	Yes	Yes
Configuration Register-1	Non-volatile	Yes	Yes
	Volatile	Yes	No
Configuration Register-2	Non-volatile	Yes	No
	Volatile	Yes	No
Configuration Register-3	Non-volatile	Yes	No
	Volatile	Yes	No
Configuration Register-4	Non-volatile	Yes	No
	Volatile	Yes	No
ECC Status Register	Volatile	Yes[10]	No
ECC Data Unit Status Register	Volatile	Yes	Yes
Bank Address Register	Volatile	No	Yes
ASP Register	RFU	Yes	Yes
Password Register	Non-volatile OTP	Yes	Yes
PPB Lock Register	Volatile	Yes	Yes
PPB Access Register	Non-volatile	Yes	Yes
DYB Access Register	Volatile	Yes	Yes
SPI DDR Data Learning Registers	Non-volatile	Yes	Yes
	Volatile	Yes	Yes
AutoBoot Register	Non-volatile	Yes	Yes
Data Integrity Check Register	Volatile	Yes	No

10 The ECC Status Register for S25HL01GT has a different function from the S70FL01GS Register. Use the Read Any Register transaction to read the ECC Status Register. S25HL01GT has the ECC Data Unit Status, which is the same function as the S70FL01GS ECC Status Register. See the datasheet for more details.

Register	Type	S25HL01GT	S70FL01GS
SEC Register	Volatile	Yes	No
Address Trap Register	Volatile	Yes	No
Error Detection Counter Register	Volatile	Yes	No
Endurance flex Pointer Address Registers	OTP	Yes	No

There are two ways to access Status and Configuration registers for the S25HL01GT device:

- Traditional method. These transactions exist in older Infineon SPI devices:
  - Using WRREG_0_1 (01h) to write to STR1N, and CFR1N;
  - Using RDSR1_0_0 (05h), RDSR2_0_0 (07h), or RDCR1_0_0 (35h) to read STR1V, STR2V, or CFR1V.

Note: The WRREG_0_1 transaction writes to the non-volatile version of the registers while the read transactions read from the volatile version of the registers. When writing to the non-volatile registers, the volatile version will be updated automatically.

- The preferred method is to use the Read or Write Any Register transactions to access any registers.
  - WRARG_C_1 (71h) to write to any register
  - RDARG_C_0 (65h) to read any register

Note that to use these new commands, register addresses in **Table 9** should be used. Also, note that S70FL01GS does not have WRAR and RDAR commands, so the register addresses listed in **Table 9** only apply to S25HL01GT.

Table 9 Register address map

Function	Register type	S25HL01GT	
		Volatile component address (Hex)	Non-volatile component address (Hex)
Device status	Status Register 1	00800000	00000000
	Status Register 2	00800001	N/A
Device configuration	Configuration Register 1	00800002	00000002
	Configuration Register 2	00800003	00000003
	Configuration Register 3	00800004	00000004
	Configuration Register 4	00800005	00000005
Endurance flex architecture	Endurance Flex Arch. Selection Register 0 [1:0]	N/A	00000050
	Endurance Flex Arch. Selection Register 1 [7:0]	N/A	00000052
	Endurance Flex Arch. Selection Register 1 [10:8]	N/A	00000053
	Endurance Flex Arch. Selection Register 2 [7:0]	N/A	00000054
	Endurance Flex Arch. Selection Register 2 [10:8]	N/A	00000055
	Endurance Flex Arch. Selection Register 3 [7:0]	N/A	00000056

Function	Register type	S25HL01GT	
		Volatile component address (Hex)	Non-volatile component address (Hex)
	Endurance flex Arch. Selection Register 3 [10:8]	N/A	00000057
	Endurance flex Arch. Selection Register 4 [7:0]	N/A	00000058
	Endurance flex Arch. Selection Register 4 [10:8]	N/A	00000059
Error correction	ECC Status Register	00800089	N/A
	ECC Count Register [7:0]	0080008A	N/A
	ECC Count Register [15:8]	0080008B	N/A
	ECC Address Trap Register [7:0]	0080008E	N/A
	ECC Address Trap Register [15:8]	0080008F	N/A
	ECC Address Trap Register [23:16]	00800040	N/A
	ECC Address Trap Register [31:24]	00800041	N/A
AutoBoot	AutoBoot Register [7:0]	00800042	00000042
	AutoBoot Register [15:8]	00800043	00000043
	AutoBoot Register [23:16]	00800044	00000044
	AutoBoot Register [31:24]	00800045	00000045
Data learning	Data Learning Register [7:0]	00800010	00000010
	Data Learning Register [15:8]	00800011	00000011
Erase count	Sector Erase Count [7:0]	00800091	N/A
	Sector Erase Count [15:8]	00800092	N/A
	Sector Erase Count [23:16]	00800093	N/A
Data integrity check	DIC Register [7:0]	00800095	N/A
	DIC Register [15:8]	00800096	N/A
	DIC Register [23:16]	00800097	N/A
	DIC Register [31:24]	00800098	N/A
Protection & security	Advanced Sector Protection Register [7:0]	N/A	00000030
	Advanced Sector Protection Register [15:8]	N/A	00000031
	ASP PPB Lock Register (Persistent Protection Block)	0080009B	N/A
	ASP Password Register [7:0]	N/A	00000020

Function	Register type	S25HL01GT	
		Volatile component address (Hex)	Non-volatile component address (Hex)
	ASP Password Register [15:8]	N/A	00000021
	ASP Password Register [23:16]	N/A	00000022
	ASP Password Register [31:24]	N/A	00000023
	ASP Password Register [39:32]	N/A	00000024
	ASP Password Register [47:40]	N/A	00000025
	ASP Password Register [55:48]	N/A	00000026
	ASP Password Register [63:56]	N/A	00000027

9 Order of execution

Some bits in the Configuration register are important to the sector architecture of the device. Ensure that these register bits are set before any program or erase is done to the device. These bits are:

- TB4KBS (Bit 2) in CFR1N[2]: Determines where parameter sectors are – bottom or top.
- SP4KBS (Bit 6) in CFR1N[6]: Determines whether parameter sectors are split between bottom and top overrides (Bit2) if set. New feature for S25HL01GT.
- UNHYSA (Bit 3) in CFR3N[3]: Determines whether parameter sectors exist in user memory.

If you modify any of these bits after a program operation to the main array, contents of the array are not guaranteed to still present. Therefore, as a best practice, you should configure these bits before accessing the flash array.

Some Status and Configuration register bits can be modified with the same transaction, but some bits have protection interactions with each other. For example, the WRREG_0_1 transaction can write both STR1x and CFRx in one transaction. LBPROT bits are in STR1x[4:2] and the TLPROT bit is in CFR1x[0]. It is recommended in software to first set LBPROT bits, then use a separate WRREG_0_1 transaction to set the TLPROT bit to protect LBPROT bits. However, if you issue the new LBPROT bit values and TLPROT bit value in the same transaction, it will still work because the device will act upon the current TLPROT value.

After you choose a protection mode for the device – protection modes are discussed later in this document, CFR1N (except TLPROT and QUADIT), CFR2N, CFR3N, and CFR4N are protected. It is important to note that any modification in these registers must be done before choosing the protection mode.

10 Protection

10.1 Legacy Bit protection

The Legacy Bit protection in S25HL01GT works the same way as in S70FL01GS except there is separate bit protection for each die in S70FL01GS. LBPROT bits protect a part or all the flash memory depending on the values.

There are two versions of LBPROT bits. The non-volatile version is in STR1N. The volatile version is in STR1V. When using the RDSR1_0_0 (05h) transaction to read, it always reads the STR1V value. If you want to read the non-volatile version of LBPROT bits, use the RDARG_C_0 (65h) transaction. The STR1NV value will be returned.

When using the WRREG_0_1 (01h) or WRARG_C_1 (71h) transaction to write LBPROT bits, depending on the LBPROT non-volatile value (in CFR1V), the transaction writes to LBPROT bits in STR1N or STR1V.

10.2 Advanced sector protection (ASP) protection

There are two ASP modes in the S25HL01GT SEMPER™ flash family:

- Persistent protection
- Password protection

You can select one by programing Bit 1 or Bit 2 of the ASP register. Note that these two bits are mutually exclusive. If you try to program both bits to ‘0’, the program transaction will result in an error and the previous setting will be retained.

After one of the modes is selected, most of the bits in Configuration registers are protected, as mentioned earlier in this document. So, it is important to program all configuration registers first before choosing the protection mode.

If the protection mode has not been selected, the device will function as if in Persistent Protection mode. Infineon strongly recommends that you explicitly select the desired mode so that malicious code cannot later change the protection behavior of the device.

11 Quad peripheral interface (QPI) operations

S25HL01GT supports QPI mode in which all information, including the instruction code, is transferred in 4-bit width. In the datasheet, this is referenced as 4-4-4 transaction protocol, as the instruction, address, and data are all transferred in 4-bit width.

To operate in QPI mode, write to the QPI-IT (Bit 6) bit in CFR2x[6].

To try out the QPI mode, use the QPI-IT volatile bit in the CFR2V register. This is the volatile version of the QPI-IT bit; the device will go back to normal mode after reset. Note that once QPI-IT volatile bit is set, the QUADIT bit (Bit 1) in CFR1V[1] will be set automatically. That indicates that all I/O signals are used for information transfer, and the WP# and HOLD# functions are disabled.

When QPI-IT volatile bit is reset back to ‘0’, the QUADIT Bit in CFR1V[1] will remain ‘1’. You must reset it back to ‘0’ if necessary. After the QPI mode has been tested thoroughly, you can set the QPI-IT bit to permanently run the device in QPI mode if required.

Although with the QPI-IT non-volatile bit set, you can still set QPI-IT volatile bit to ‘0 ‘so the device reverts to normal mode, this is not a recommended operation because the device would always revert to QPI after reset.

12 Secured silicon region (SSR)

The secured silicon region in S25HL01GT works in the same way as in S70FL01GS except that there are separate SSRs for each die in S70FL01GS. The S25HL01GT SEMPER™ Flash family provides 1024 bytes of secured silicon region (SSR) area separated from the main flash array. The area is divided into 32 individually lockable, 32-byte-aligned regions. (32 x 32 bytes = 1024 bytes) as monolithic die, where as there is separate bit protection for each die in S70FL01GS.

SSR is protected by the bit in CFR1V[0]. If TLPROT is set, the SSR program transaction will be ignored. No error is reported.

Region 0 of the SSR (first 32 bytes) is a special region. The first 16 bytes of Region 0 are reserved for Infineon to program in a random number that can be used as a unique device identification; for example, serial number. The next four bytes are the lock bits. Each lock bit controls the corresponding 32 SSR regions, from Region 0 to Region 31. Any attempt to program to the random number area will result in a program error. If an SSR region is locked by its lock bit, any attempt to program into the region will result in a program error.

13 Deep Power-Down mode

Only the S25HL01GT support Deep Power-Down modes. The S25HL01GT device does not use the release from Deep Power-Down command. Driving CS# LOW will release the S25HL01GT device from the Deep Power-Down mode. Release from Deep Power-Down will take the time duration of t_{RES}.

14 Capacitance characteristics

Table 10 Capacitance

Symbol	Parameter	S25HL01GT		S70FL01GS		Units
		Min	Max	Min	Max	
C_{IN}	Input capacitance		4.0		16	pF
C_{OUT}	Output capacitance		7.5		16	pF

15 DC parameters

Table 11 compares the DC parameters of S25HL01GT and S70FL01GS. While most parameter differences should not cause performance issues when migrating, it is highly recommended that users carefully review all the parameter differences for any potential impact.

Table 11 DC parameter comparison[11]

Symbol	Parameter operating temperature range – 40°C to +85°C	S25HL01GT			S70FL01GS			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage	2.70	3.00	3.60	2.70	3.00	3.60	V
V_{CC} (min)	V_{CC} (minimum operation voltage)	2.70			2.70			V
V_{CC} (cutoff)	V_{CC} (cut-off where reinitialization is needed)	2.40			2.40			V
V_{CC} (low)	V_{DD} (low voltage for initialization to occur)	0.7			1.00			V
V_{IL}	Input LOW voltage	V_{CC} x -0.15		V_{CC} x 0.35	–0.5		0.3 x V_{CC}	V
V_{IH}	Input HIGH voltage	V_{CC} x 0.65		V_{CC} x 1.15	0.7 x V_{CC}		V_{CC} +0.4	V
V_{OL}	Output LOW voltage			0.2			0.15 x V_{CC}	V
V_{OH}	Output HIGH voltage	V_{CC} – 0.2			0.85 x V_{CC}			V
I_{LI}	Input leakage current			±2			±2	µA
I_{LO}	Output leakage current			±2			±2	µA
I_{CC1}	Active power supply current (READ) – Serial SDR 50 MHz		10	21			18	mA
	Active power supply current (READ) – Serial SDR 133 MHz						36	mA
	Active power supply current (READ) – QPI SDR 80 MHz						50	mA
	Active power supply current (READ) – QPI SDR 104 MHz						61	mA
	Active power supply current (READ) – QPI SDR 133 MHz							mA
	Active power supply current (READ) – QPI SDR 166 MHz		53	69				mA
	Active power supply current (READ) – QPl DDR 66 MHz						75	mA
	Active power supply current (READ) – QPl DDR 80 MHz						90	mA

11 Typical values are at 25°C and minimum, maximum values are at -40°C, - 85°C respectively.

DC parameters

Symbol	Parameter operating temperature range – 40°C to +85°C	S25HL01GT			S70FL01GS			Units
		Min	Typ	Max	Min	Typ	Max	
	Active power supply current (READ) – QPI DDR 102 MHz		50	68			N/A	mA
I_{CC2}	Active power supply current (page program)		50	66			100	mA
I_{CC3}	Active power supply current (WRR or WRAR)		50	66			100	mA
I_{CC4}	Active power supply current (SE)		50	66			100	mA
I_{CC5}	Active power supply current (HBE, BE)		50	66			100	mA
I_{SB}	Standby current @ 85C		14	126		140	200	µA
I_{DPD}	Deep power-down current		2.2	26				µA
I_{POR}	Power-on reset current			80				mA

16 AC parameters

Table 12 and Table 13 compare the AC parameters of S25HL01GT and S70FL01GS. While most parameter differences should not cause performance issues when migrating, it is recommended that you carefully review all the parameter differences for any potential impact.

Table 12 Single data rate (SDR) AC parameter comparison[12]

Symbol	Parameter operating temperature range –40°C to +85°C	S25HL01GT			S70FL01GS			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK} - 1	SCK clock frequency for Fast, Dual and Quad commands			166			133	MHz
f_{SCK} - 2	SCK clock frequency for READ and 4READ instructions			50			50	MHz
P_{SCK}	SCK clock period	1/ f_{SCK}		∞	1/ f_{SCK}			
t_{WH}, t_{CH}	Clock HIGH time	45% P_{SCK}		55% P_{SCK}	45% P_{SCK}		55% P_{SCK}	ns
t_{WL}, t_{CL}	Clock LOW time	45% P_{SCK}		55% P_{SCK}	45% P_{SCK}		55% P_{SCK}	ns
t_{CS}	CS# HIGH time (Read instructions)	10			10			ns
	CS# HIGH time (Read instructions with RESET & QUAD enabled)	20						ns
	CS# HIGH time (Program/Erase transactions)	50			50			ns
t_{CSS}	CS# Active setup time relative to CK ($f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz)	5 / 4			3 / 3			ns
t_{CSH0}	CS# Active hold time (relative to CK)	4			3			ns
t_{CSH3}	CS# Active hold time (relative to CK)	6			3			ns
t_{SU}	Data in setup time ($f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz)	5 / 2			1.5			ns
t_{HD}	Data in hold time (FCK ≤ 50 MHz / $f_{CK} > 50$ MHz)	5 / 2			2			ns
t_V	Clock LOW to output valid (30-pF loading)	2		9			8	ns
	Clock LOW to output valid (15-pF loading)	2		8			6.5	ns
t_{HO}	Output hold time	1.5			1			ns
t_{DIS}	Output disable time			9			8	ns
t_{DP}	CS# HIGH to Deep Power-Down mode			3				µs
t_{RES}	Release from Deep Power-Down mode to wakeup			380				µs

12 Minimum, maximum values are at -40°C - 85°C.

AC parameters

Table 13 Double data rate (DDR) AC parameter comparison

Symbol	Parameter operating temperature range –40°C to +85°C	S25HL01GT			S70FL01GS			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK} – 1	SCK clock frequency			102			80	MHz
P_{SCK}	SCK clock period	1/ f_{SCK}			1/ f_{SCK}			
t_{WH}, t_{CH}	Clock HIGH time	45% P_{SCK}		55% P_{SCK}	45% P_{SCK}		55% P_{SCK}	ns
t_{WL}, t_{CL}	Clock LOW time	45% P_{SCK}		55% P_{SCK}	45% P_{SCK}		55% P_{SCK}	ns
t_{CS}	CS# HIGH time (Read instructions)	10			10			ns
	CS# HIGH time (Read instructions with RESET & QUAD enabled)	20						ns
	CS# HIGH time (Program/Erase transactions)	50			50			ns
t_{CSS}	CS# Active setup time relative to CK ($f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz)	5 / 4			3			ns
t_{CSH0}	CS# Active hold time (relative to CK in mode 0)	4			3			ns
t_{SU}	Data in setup time ($f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz)	2			1.5			ns
t_{HD}	Data in hold time ($f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz)	1.2			1.5			ns
t_V	Clock LOW to output valid (15-pF loading)	2		8			6.5	ns
t_{HO}	Output hold time	1.5			1.5			ns
t_{DIS}	Output disable time			9			8	ns
t_{DP}	CS# HIGH to Deep Power-Down mode			10				µs
t_{PU} /t_{RPH}	Reset time			450[13]			35	µs

13 The Reset time is the same as POR for S25HL01GT.

17 Embedded algorithm performance

Table 14 compares the embedded algorithm performance parameters of S25HL01GT and S70FL01GS. While most parameter differences should not cause performance issues when migrating, it is recommended that you carefully review all the parameter differences for any potential impact.

Table 14 Embedded algorithm performance parameter comparison

Symbol	Parameter operating temperature range –40°C to +85°C	S25HL01GT			S70FL01GS			Units
		Min	Typ	Max	Min	Typ	Max	
t_W	Non-volatile register write time		44	357.5		140	500	ms
t_{PP}	Page programming (256 bytes)		480	1700		250	750	µs
	Page programming (512 bytes)		570	1700		340	750	µs
t_{SE}	Sector erase time (4-KB parameter sectors)		42	335				ms
	Sector erase time (256-KB Long Retention sectors)		773	2677		520	2600	ms
	Sector erase time (256-KB High Endurance sectors)		773	5869				ms
	Bulk erase time (1Gb)		386	1381		206	920	s

18 Summary

This guide is intended as a supplement to the S25HL01GT datasheet and discusses the new features of the S25HL01GT device and software considerations the designer should make when migrating from the Infineon 65-nm S70FL01GS MCP Quad SPI 3.0 V Flash to the Infineon 45-nm monolithic S25HL01GT SEMPER™ Flash with Quad SPI 3.0 V. It describes some important functions in S25HL01GT and how to configure and operate the devices.

Related documents

SPI NOR flash documents

[1] S25HL-T SEMPER™ flash family datasheet

- 002-12345 - S25HS512T/S25HS01GT, 512MB (64 MB), 1 GB (128 MB), HS-T (1.8-V), HL-T (3.0 V) SEMPER™ flash with Quad SPI

[2] S70FL01GS datasheet

- 001-98295 - S70FL01GS, 1 GBIT (128 MBYTE) 3.0V SPI FLASH

[3] S25FL512S family datasheet

- 001-98284 - S25FL512S, 512 Mbit (64 Mbyte) 3.0 V SPI flash memory

[4] Migration guide for 45-nm S25HL-T SEMPER™ flash Quad SPI from 65-nm S25FL-S Quad SPI flash

- AN218548 discusses the new features of the Infineon S25HL-T SEMPER™ flash Quad SPI family and software considerations the designer should make when migrating from the Infineon 65-nm S25FL-S Quad SPI 3.0 -V flash family.

[5] Endurance flex application note

- AN218481 provides insights into Infineon’s endurance flex wear-leveling architecture implemented in SEMPER™ flash family of devices and shows use cases for customers to exploit its benefits.

[6] Automatic ECC for Infineon MIRRORBIT™ Eclipse architecture Serial NOR flash memory families application note

- AN200731 provides supplemental information regarding the automatic ECC feature for Infineon MIRRORBIT™ Eclipse architecture that is built into the Infineon FL/S-S, HL/S-T and KL/S-S Serial NOR flash memory families.

[7] SafeBoot in Infineon SEMPER™ NOR flash application note

- AN226393 describes the SafeBoot feature in Infineon SEMPER™ NOR flash memories and provides guidelines and suggestions to implement host application software.

[8] DLP optimized read performance for SEMPER™ flash with Quad SPI

- AN2264996 highlights the use of the data learning pattern (DLP) feature that can optimize read performance for the SEMPER™ flash with Quad SPI.

Revision history

Document version	Date of release	Description of changes
**	2018-09-25	New application note.
*A	2019-12-10	Updated Table 11, Table 12, and Table 13 Updated Related Documents.
*B	2021-02-26	Migrated to Infineon template.
*C	2022-06-23	Updated the following: • Enduraflex to Endurance flex • Cypress to Infineon • Mirrorbit™ to MIRRORBIT™.

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