AN220402

Traveo Family MCUs: Power Supply Drop Below Minimum Supply Voltage Level But Above Vreset

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Associated Part Family: Traveo™

Related Application Notes: For a complete list, click here."

This app note presents different measures to ensure that Cypress Traveo™ family MCUs operate within the specified conditions when the power supply falls below VCC_{min} but above V_{reset} especially in multi-power systems.

1 Introduction

This application note describes a power supply drop below the minimum VCC level (VCC_{min}) but above the supply reset threshold (VCC_{reset}) leading to compromised device operation that is not detected by a system reset. This is a general scenario for a drop of the internal core supply and power up with a residual voltage without the internal monitor detecting it and triggering a low-voltage reset. In such cases, the application needs to make sure an external reset is executed to reinitialize the MCU to a safe state.

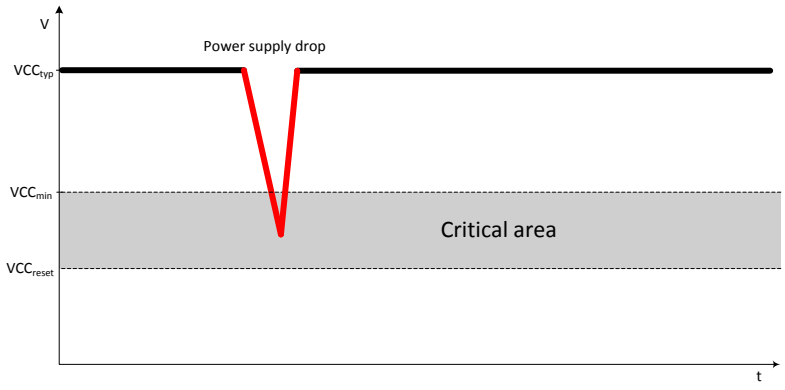
Voltage drops, glitches, or crank impulses in different power domains are unpreventable in an automotive application. Figure 1 illustrates a power supply drop event on the VCC power domain. This kind of disturbance on VCC can be caused by different power events (for example, during starting of the engine, or by a short power OFF/ON event during low-power mode).

If the power supply drops into the critical voltage area below VCC_{min} but above VCC_{reset}, registers might not have been initialized properly and the content of retention RAM may not be assured. The application must take care to minimize the risk that the residual voltage during power events is below V_{reset}, and reset conditions are met to restart the system with initialized values.

Typical Cypress Traveo family MCUs in a multiple power supply system use several power monitors to detect power up for power-on reset (POR) or power-down for low voltage (LVD) and brown-out detection (BOD). Monitors for POR observe the internal core supply and generate a reset based on a fixed detection level. Monitors for external I/O supplies (LVD) are configurable by the user application. The LVD supports fixed or adjustable voltage detection levels and usage as either a hard reset or a warning interrupt.

Additional case studies are available in AN220401 – Power Supply Drop Above VCC_{min} and Supply Monitor Detection Level and AN220973 – Power Supply Drop Below V_{reset} and System Recovers Safely.

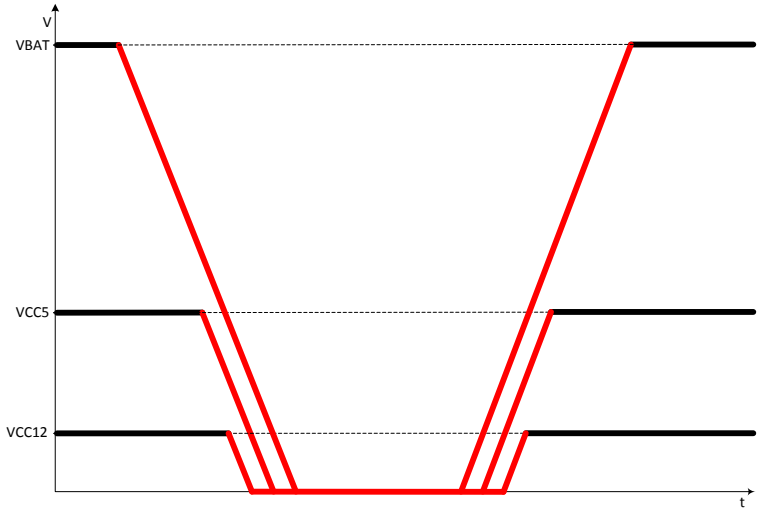
Figure 1. Critical Voltage Drop Below VCC_{min} But Above V_{reset}



2 Power Drop and Impact on Core Supply

In a multiple power supply system, power domains are generated by different voltage regulators that are dependent on each other. An unintended power cycle on the battery voltage domain (VBAT) may cause a voltage drop on related voltage domains subsequently. As shown in Figure 2, a typical power drop in automotive applications must always follow the specified power sequencing. In Traveo MCU devices, for example, the core voltage must always be lower than the high-level voltage domain (VCC5 ≥ VCC12). The core voltage is always the last voltage domain that is affected by a power drop on VBAT.

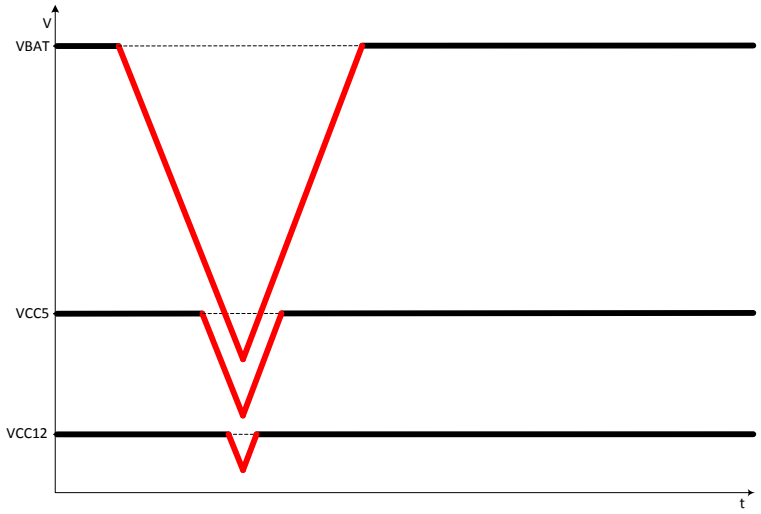
Figure 2. Dependencies Among Power Domains During a Power Cycle on VBAT



The power cycle duration defines the residual voltage of each power domain. If the power OFF period is sufficiently long, all voltages can be discharged to GND level and all requirements for proper POR generation can be met. See AN220973 for more details.

In the case of a short voltage drop, power domains may not be discharged completely. Figure 3 illustrates the case when the power OFF period is not long enough for power domains to recover from a residual voltage level.

Figure 3. Short Power Cycle on VBAT with a Residual Voltage on Related Power Domains



For more details on unintended power cycle scenarios, see AN220339.

3 Dependences of Power-Up with Residual Voltage

3.1 Leakage Current and Residual Voltage Versus Ambient Temperature

During a power drop, capacitors connected on power domains are discharged. The leakage current is the most important factor that defines the discharge period. There is a nonlinear dependency between leakage current and ambient temperature. Leakage current increases at higher temperatures (HT) and decreases at lower temperatures (LT). The worst-case scenario is at an LT condition where the voltage crosses the critical voltage area between VCC_{min} and V_{reset} very slowly (up to several minutes) with a high risk to restart the system with a residual voltage outside of specified operating conditions ($VCC < VCC_{min}$).

4 Preventing Start Up with Residual Voltages

4.1 Avoiding a Residual Voltage During Power Cycle

There are different options to detect a voltage drop on power domains:

- Supervision of the VBAT voltage domain by an ADC range comparator (<7 V). A pre-warning interrupt can be used to save sensitive data from RAM to work flash. In addition, the load on VCC can be reduced to allow a recovery on affected voltage domains. See AN220401 for more details.
- Supervision of the high-level I/O and core voltage domains ($VCC \le VCC_{min}$). A critical power drop scenario is detected when the voltage drops below the minimum VCC level. Different actions must be taken to minimize the risk of restarting the system with a residual voltage within the critical area ($VCC_{reset} \le VCC \le VCC_{min}$):
  1. Reset the MCU.
  2. Disable voltage regulators.
  3. Activate a controlled discharge process of the core voltage. This can be realized by different options:
     - Turning ON a resistor via a MCU-GPIO pin. Figure 4 shows a principal example for active discharging. After a reset is issued by the voltage supervisor, the GPIO pin is in HI-Z mode and automatically turns ON the discharge resistance.
     - The auto discharge function of an external voltage regulator (see Figure 5).

     There are pros and cons in regard of power down with discharging. On one hand, this is the only way to ensure the proper generation of a POR by crossing the critical voltage area between VCC_{min} and V_{reset} quickly. On the other hand, the BOM costs increase due to additional supervision components needed, especially for the advanced voltage regulators that support active discharging.

Figure 4. Active Discharging Controlled by MCU

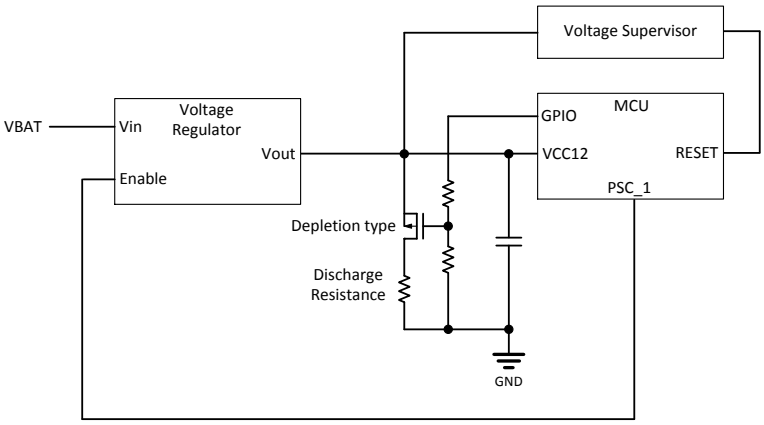
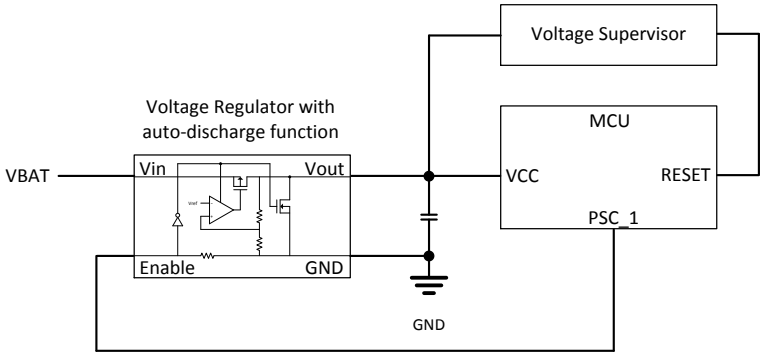


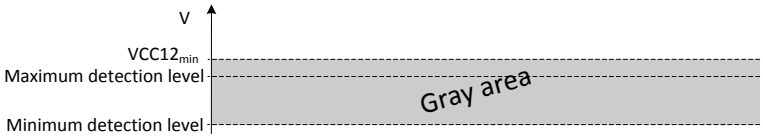
Figure 5. Auto-Discharge Function Integrated into External Voltage Regulator



4.2 Reducing the Critical Supply Range from Low-Voltage Detection Level to Minimum Core Operation Supply Level

Voltage supervisors are designed to work at a specified voltage detection level. Ideally, this level should be defined as close as possible to the minimum core supply voltage ($VCC12_{min}$). Due to process parameter variations, the actual detection level also varies within the specified range. Figure 6 illustrates the challenge during system design, where an adequate detection level must be defined to minimize the gray area to be below $VCC12_{min}$.

Figure 6. Gray Area to be Considered During Supervision Level Definition



The following requirements for the power monitor are recommended:

- Use high-accuracy, trimmable, detection levels.
- For programmable detection levels, use a maximum threshold close to $VCC12_{min}$.

4.3 Using an External Monitor

MCU-internal low-voltage detection monitor (LVD) levels are not always accurate enough to fulfill system requirements. In such cases, external voltage supervisors must be used to observe dedicated supply voltage levels to generate an interrupt or reset signal. Note the following recommendations during design:

- Use voltage supervisor components with minimum tolerance (≤1%) to minimize the gap (see Section 4.2).
- Place components close to the MCU power supply pins for best accuracy.

5 Summary

Embedded systems are exposed to different environmental conditions where a stable power supply cannot be guaranteed. In each scenario, the power supply architecture in an application must ensure that the recommended operating conditions – specified in the datasheet – are always complied with. Once the power supply is disturbed causing a voltage drop, different mechanisms must trigger actions to back up sensitive data and to recover the system smoothly.

A power drop on the VCC domain to a level below the VCC_{min} but above the V_{reset} level is very critical regarding the operational conditions of the MCU. An unintended restart of the power supply in that voltage area can lead to uninitialized MCU registers compromising the system. To minimize the risk, there are different techniques possible for recognizing a power drop.

To fulfill system-level safety requirements, a combination of internal voltage monitors (LVDs) with external voltage supervisors should be used so that different observation levels can trigger appropriate actions. In any case, a fast power-down is required where the critical voltage area between $VCC12_{min}$ and V_{reset} is quickly crossed by turning on additional loads on the core voltage domain to assure defined discharging conditions during all environmental conditions.

It is recommended to handle voltage drops below VCC_{min} with resets to bring the system into a defined condition. In case of MCU-internal POR generation, see AN220973 – Safe System Recovery from Power Supply Drop Below V_{reset} where the timing and voltage conditions are explained in detail.

6 Definitions, Acronyms and Abbreviations

VCC_{min}	Minimum specified voltage level of the supply voltage, VCC
V_{reset}	Voltage level of VCC where a power-on reset (POR) is issued
POR	Power-on reset
LVD	Low-voltage detection
VCC12	MCU Core voltage domain
VCC5	High-level I/O voltage domain
VBAT	Batterie voltage domain

7 Related Documents

- Traveo Family S6J3310/S6J3320/S6J3330/S6J3340 Series 32-bit Microcontroller Datasheet
- AN220401 – Traveo Family MCUs: Power Supply Drop Above VCCmin and Supply Monitor Detection Level
- AN220973 – Traveo Family MCUs: System Safe Recovery when Power Supply Drops Below Vreset
- AN220338 – Traveo Family MCUs: Intended Power Cycles
- AN220339 – Traveo Family MCUs: Unintended Power Cycles

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