AN220401

Traveo Family MCUs: Power Supply Drop Above VCC_{min} and Supply Monitor Detection Level

Author: Peter Berndt

Associated Part Family: Traveo™

Related Application Notes: For a complete list, click here.

This app note presents different measures to ensure that Cypress MCUs operate within the specified conditions when the power supply falls above VCC_{min} and the voltage supervisor detection level especially in multi-power systems.

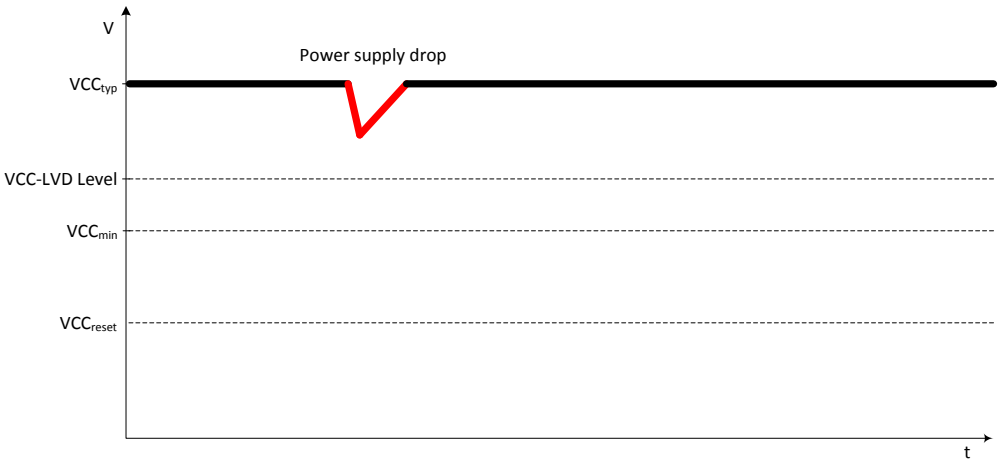
Contents

1 Introduction

This application note is intended to describe the general scenario of IR drop in an MCU application, where the power supply drops above the minimum VCC level (VCC_{min}) and above supply monitor detection level (VCC-LVD level). This kind of disturbance is usually an uncritical power drop if the MCU supports isolated power domains in a multi-power system. The core logic must support the level shifter between an internal always-on power domain and external power domain.

Voltage drops, glitches, or crank impulses in different power domains are unpreventable in an automotive application. Figure 1 illustrates a power supply drop event on the VCC power domain. Short disturbances on VCC can be caused either by a short voltage drop on the battery or after an active load reduction. They are uncritical if the power voltage recovers to a stable condition (VCC_{typ}).

Figure 1. Uncritical Voltage Drop Above VCC_{min} and VCC-LVD Level



The introduced scenario is the first out of three different power drop factors. Additional case studies are available in AN220402 – Traveo Family MCUs: Power Supply Drop Below Min Supply Voltage But Above V_{reset} and AN220973 – Traveo Family MCUs: System Safe Recovery when Power Supply Drops Below V_{reset}.

This document describes the options how to recognize a power drop on the high-level I/O domain compared to the low-level core domain. In addition, it shows how a power drop above the minimum supply voltage level (VCC_{min}) should be recovered with a reset or interrupt by detecting it with an internal or external voltage monitor on a detection level above VCC_{min}.

1.1 Power Drop on High-Level I/O Domain

The supervision of the high-level I/O domain (VCC) can be managed by internal or external voltage monitors; an internal LVD is recommended for observing the related power domain though optionally, an external supervisor can be used. Note that monitoring the supply voltage externally will not guarantee measuring the same level as from inside the MCU silicon. If external supervision is the only option, an adequate, increased threshold level must be defined to consider the required margin between internal and external voltage levels. Figure 2 illustrates the power drop detection on the high-level I/O domain with internal and external voltage monitors. The threshold level of an external supervisor is higher than the MCU LVD threshold level.

In both cases, an interrupt can be generated by an LVD interrupt, external interrupt, or NMI. Note that these interrupts must have a high priority to allow handling the critical power issue in time.

Consider the following actions after a power drop is recognized:

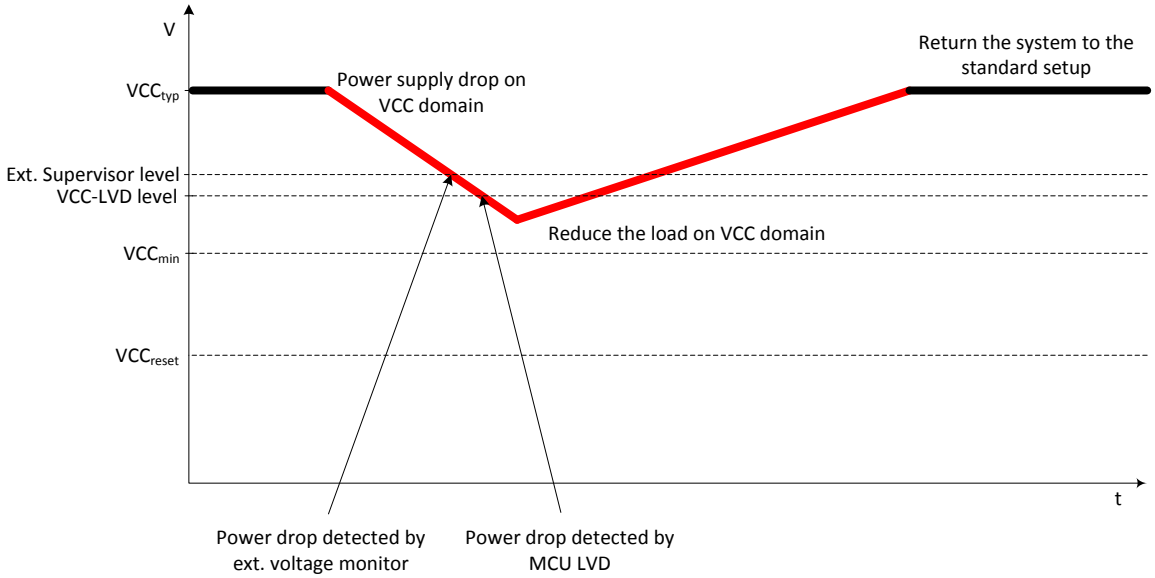
- Save sensitive data from RAM into Work Flash
- Reduce as much load on VCC as possible (e.g., switch OFF display backlight). Note that a power drop on VCC domain can be a consequence of a power drop on a higher-level power domain like the battery voltage. Thus, it makes sense to reduce the load on all domains.
- Disable PLL and switch to lower clock speed
- Switch to a conservative and stable I/O setup (e.g., disable interfaces and external transceivers which are not required in a safe state)

Assuming that there is only a short disturbance on VCC, these measures can recover the voltage to return to a stable condition. Once the power supply recovers, the system can return to the standard configuration. Note that all these actions are a reaction to an unexpected exception. If possible, minimize the period where the system is in an “emergency mode”.

If these power drops occur in a higher frequency, the system power is extensively affected. In that case, the system should switch to a failure mode and the user must informed on by warning information (e.g. on the display). In the scenarios where the power supply cannot be recovered and the voltage level drops below VCC_{min}, additional actions must be taken. See application notes AN220402 and AN220973 for more details.

Note that it is not recommended to issue a reset after a voltage drop is detected. This will disable all loads on VCC; in an unrecoverable scenario, the voltage cannot leave the critical area between VCC_{min} and VCC_{reset} fast enough. See application note AN220402 for more details.

Figure 2. Voltage Drop Detection on High-Level I/O Domain



1.2 Power Drop on Low-Level Core Domain

Depending on the MCU power concept, in addition to an internal voltage regulator, there might be also an external power supply connected to the microcontroller's core supply (VCC12). Although the high-level I/O supply is stable, the core voltage might drop below the specified range; different measures must be taken to protect the system.

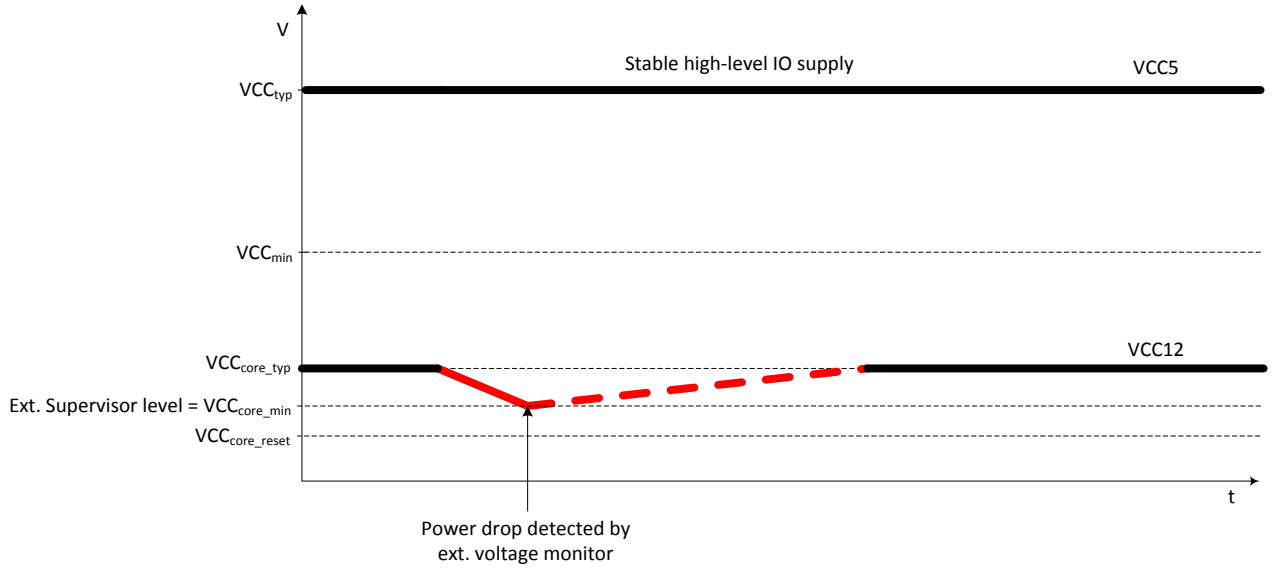
There are different options to realize the power concept for an external core voltage supply generation. The external core voltage regulator can be permanently enabled or actively disabled in the low-power mode. For this, some MCUs might provide dedicated enable signals (e.g., PSC_1 signal in Traveo MCUs). See also Section 5).

If the external core voltage regulator is shut-down during the low-power mode, monitoring of this domain must be disabled during the low-power mode to ensure that an unintended reset is not issued. Similarly, the internal VCC12 monitor must be disabled accordingly (e.g., set an adequate PSS profile in Traveo MCUs) before the application enters low-power mode.

The other case is the unintended power-drop due to a voltage disturbance. In that case, reset should be asserted if the internal or external monitor level is reached.

Depending on the supply architecture, a power drop event on the external core supply has different consequences. In any case, the MCU must be secured to ensure minimum operating conditions. The specific difficulty is to define an adequate protection threshold for the voltage supervisor. There is only a small margin between VCC_{core_min} and VCC_{core_reset} and the tolerance of the monitor level must also be considered. If a voltage drop is detected by the voltage supervisor, a reset must be issued to minimize the risk that the core is operating in an unspecified condition ($VCC_{core} < VCC_{core\_min}$).

Figure 3. Power Supply Drop on Low-Level Core Domain



2 Pros and Cons of an External Voltage Monitor

External voltage supervisor components are designed to monitor the supply voltage in embedded systems with very high accuracy specified for both industrial as well as automotive applications. There are different types of voltage monitors on the market supporting various monitor levels which can generate active HIGH or active LOW resets or interrupt signals if an under-voltage condition is detected. When a voltage drop is detected, the supervisory circuit will reset the MCU and keep it in that state as long as the under-voltage condition persists. This type of reset is called brown out reset.

Advantages

- Can actively change the status of an MCU by reset or interrupt (NMI, etc.) to recover the system from an undefined condition
- Active part of power and safety concept
- Highly accuracy (≤1%)
- Factory-trimmed threshold levels for monitoring
- Various monitor levels useful for triggering different actions
- Wide range of external voltage monitors on the market supporting dedicated, adjustable threshold levels
- Overvoltage and undervoltage detection

Disadvantages

- Monitors only the local voltage on the PCB, not the voltage on the microcontroller's silicon
- Advanced requirements on the PCB layout to minimize any kind of disturbance, which may have an impact on the supply voltage to be monitored
- Expensive

3 Pros and Cons of an Internal Voltage Monitor

Cypress' microcontrollers support internal voltage monitors by low-voltage detection (LVD) circuits including the supervision of internal and external supply voltages. LVDs can generate POR, LVD reset, or interrupts. Therefore, depending on the degree of power drop, different actions can be taken. Small voltage drops can issue a high prioritized interrupt which can be used to disable external loads (e.g., display) for recovering the system, or save sensitive data before the system switch off due to missing power. Some LVDs can generate a POR, which is a reset signal when power is applied to the device or when the power drops below Vreset threshold. It ensures that the device starts operating in a known state.

The major advantage of an internal voltage monitor compared to an external component is that the power supply is measured directly on the silicon. This means that the external power supply connected to the MCU pins is supervised after the signal passed the bond wire, lead-frame, and pad structure, which may impact the power supply on the die and cannot be observed by the external voltage monitor.

Advantages

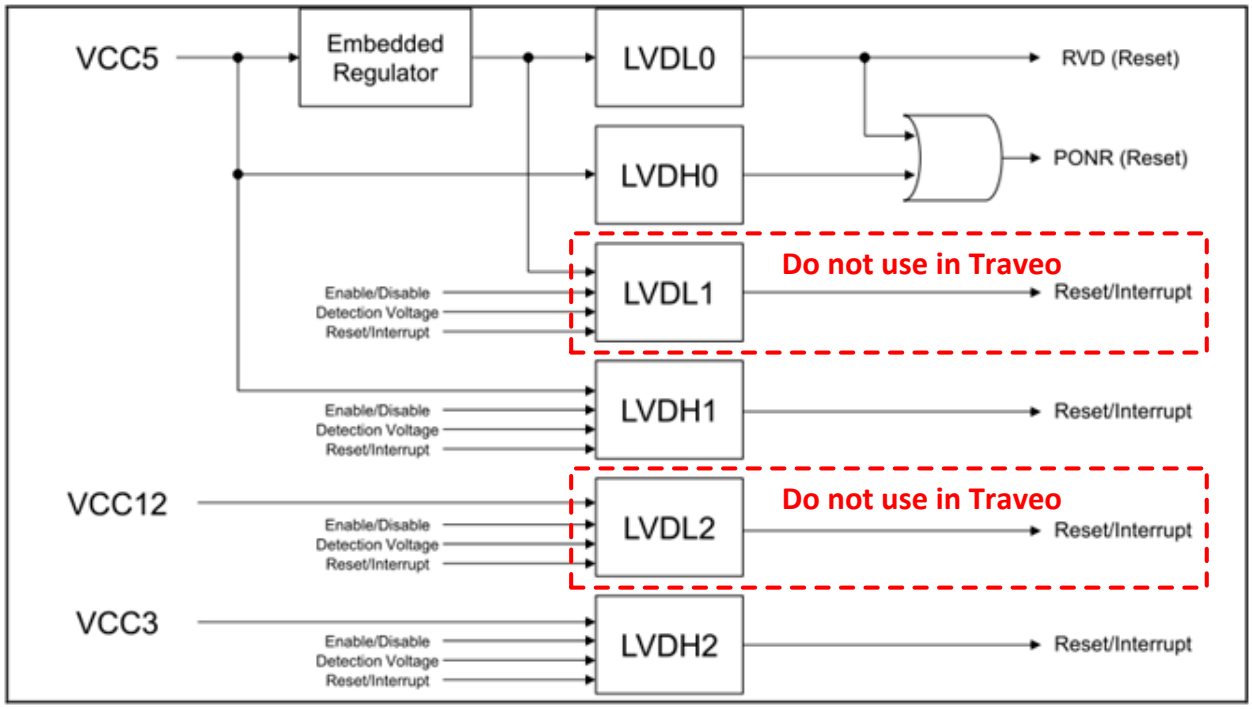
- Power-on reset (POR) generation
- Low-voltage detection and reset for RAM retention
- Internal regulator output supervision
- External power supply supervision
- On-chip voltage monitoring of external power supply. This enables the option to detect the power drop on the critical points of internal logic like Core or Backup RAM.
- Less expensive than an external voltage monitor

Disadvantages

- Internal voltage regulator may not sufficient to fulfill safety concept requirements
- Does not support over-voltage detection. Can alternatively compensated by ADC voltage monitoring.
- Core voltage supervision not supported in Traveo MCUs. Adjustable threshold values are out of recommended operating conditions.
- Insufficient granularity; too few options to define the LVD threshold values in Traveo MCUs.

Figure 4 shows the voltage monitors used in Traveo devices. Overall, there are six supply voltage supervisors observing internal and external power supplies. Two fixed LVDs connected to VCC5 and Vcore, which can generate POR. In addition, these have four adjustable LVDs connected to all internal and external power domains (VCC5, VCC3, VCC12, and Vcore), which can generate LVD resets or interrupts. Note that in Traveo devices, monitor levels for the core voltage domain cannot be set to operate in a specified condition. Do not use LVDL1 and LVDL2 because these are examples of functional limitations discussed in Section 4. See the related datasheet for additional information.

Figure 4. LVD Hardware in Traveo Devices

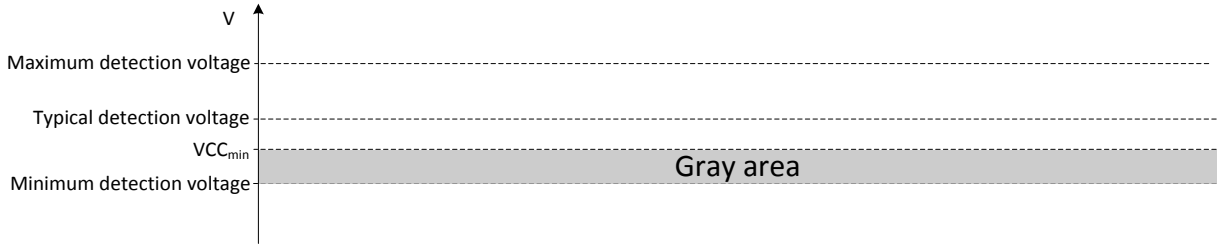


4 The Gray Zone and Functional Limits of Voltage Monitors

Generally, voltage monitors cannot be produced that work on fixed threshold levels. Process tolerances during manufacturing of the device create deviations with upper and lower limits. See the related datasheet for specified values.These limits must be considered during the definition of voltage monitor levels. The related minimum value of the threshold must be above the minimum allowed supply value VCC_{min}.

For this reason, LVDL1 and LVDL2 are not usable in Traveo MCUs because all adjustable threshold limits are below VCC_{min}.

Figure 5. Grey Area and Functional Limits of Voltage Supervisor



The following table shows critical threshold settings in Traveo MCUs for VCC observation (VCC_{min} = 2.7 V):

LVDH1V*	0	1	2	3	4	5	6	7
Min. Threshold	2.4 V	2.5 V	3.2 V	3.4 V	3.6 V	3.8 V	2.2 V	2.3 V
Typ. Threshold	2.7 V	2.8 V	3.6 V	3.8 V	4.0 V	4.2 V	2.5 V	2.6 V
Max. Threshold	3.0 V	3.1 V	4.0 V	4.2 V	4.4 V	4.6 V	2.7 V	2.9 V

*Configuration register for LVDH1 threshold level in Traveo devices.

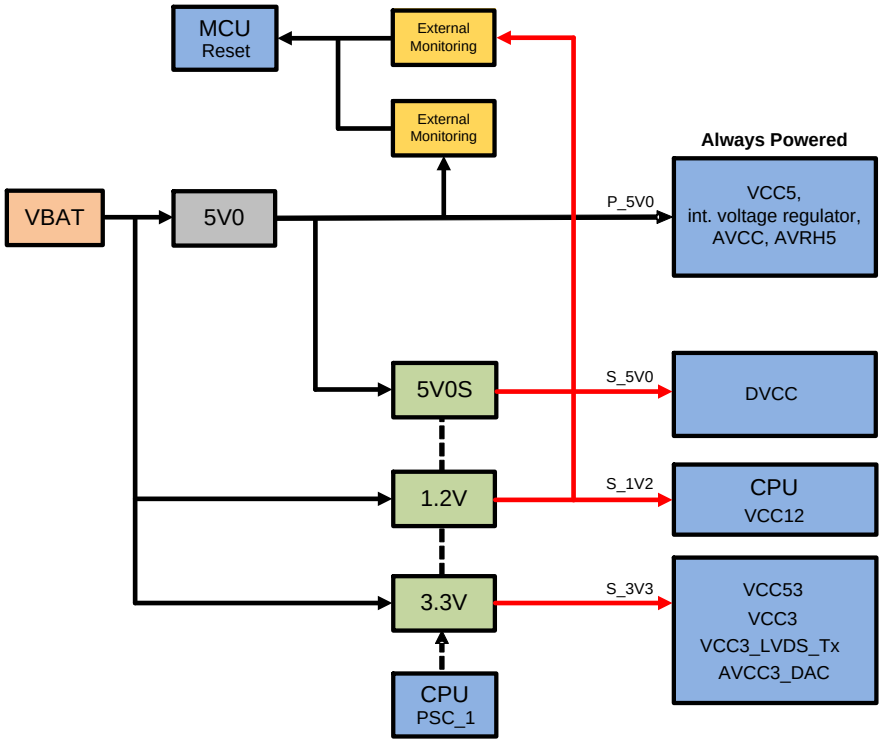
5 Architectures for Automotive Applications

In low-power mode, external power supplies can be switched OFF to minimize the current consumption. However, the controlled shut-down of power domains include a risk to generate a short voltage drop if an asynchronous wakeup event restarts the voltage generation too early. There are two main architectures which must be considered in automotive applications related to an intended shut down of external power supplies during low-power mode.

1. External low-level core domain regulator disabled, but VCC is still active.

   Generating a POR is linked to VCC and internal core voltage (internal voltage regular). Under regular conditions, both power domains are stable and are applied during the low-power mode; a potential short power cycle is solely related to external switched power domains. Therefore, there is no impact on POR generation. A wakeup event (e.g., RTC timer event or CAN wakeup) issues a wakeup reset, which initializes the MCU and restarts the system. The monitoring of switched power domains must only be done in RUN mode when all voltage regulators are stable and switched ON. Unintended voltage drops on VCC and external low-level core domain must be detected by internal or external voltage supervisors.

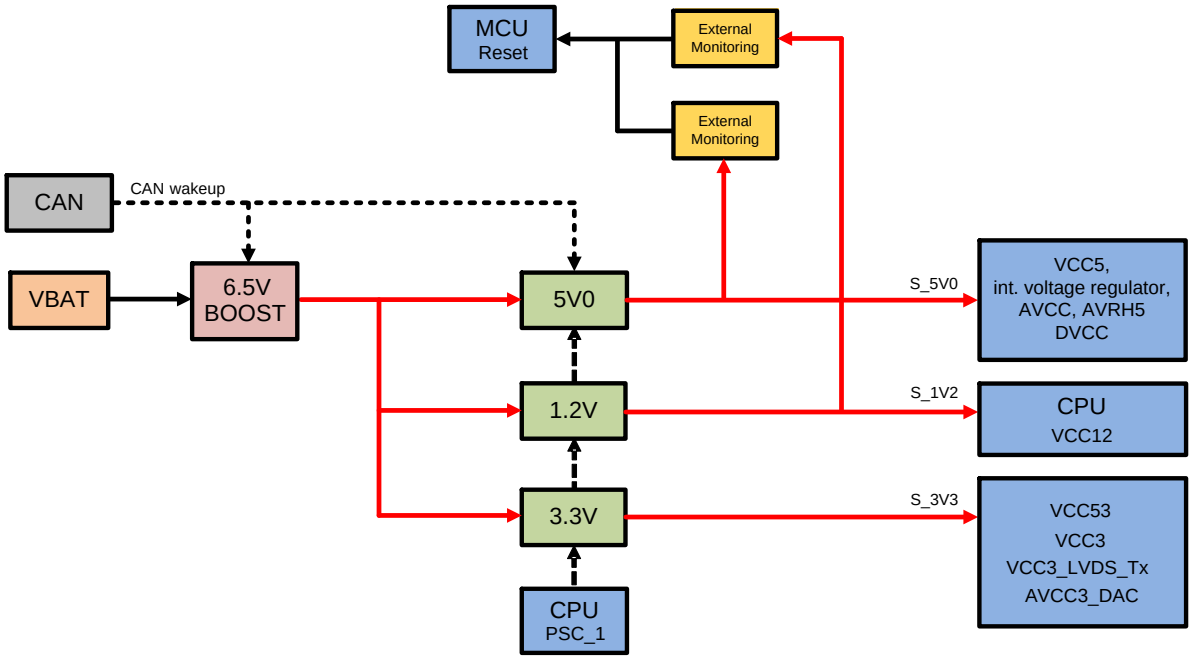
Figure 6. High-Level IO Domain Always Powered in Low-Power Mode



2. Disable all power domains including high-level I/O domain to shut-down the whole system for minimum power consumption (see Figure 8).

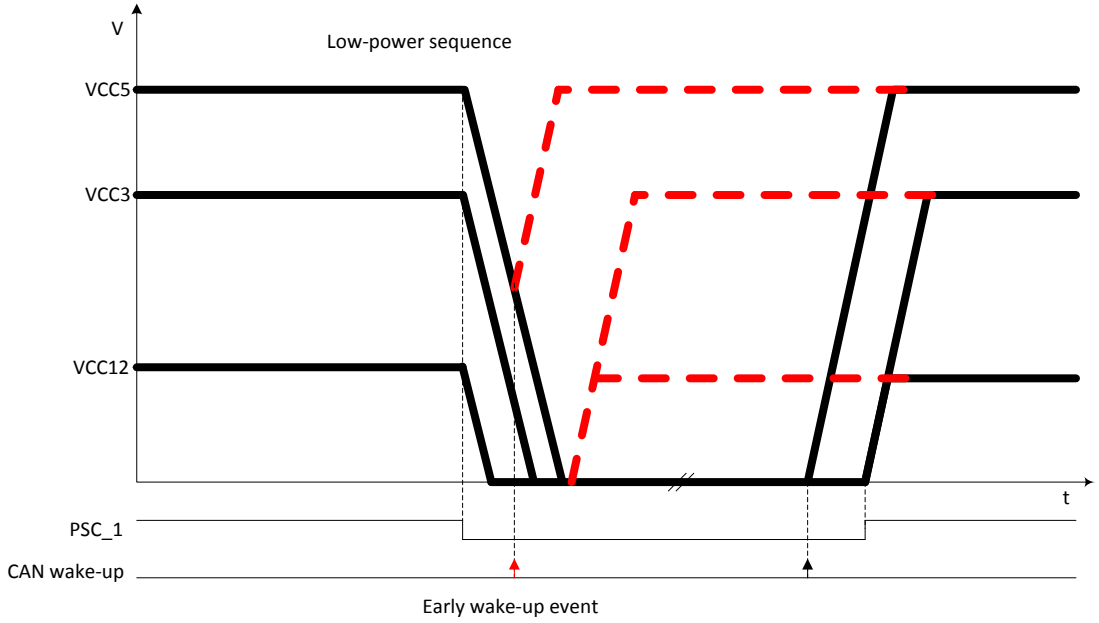
   In that scenario, all power supply voltages are discharged ideally to ground level. The system is woken up by an external event (e.g., CAN wakeup). In a worst-case wakeup timing (early wakeup event), however, power supplies may enter a critical area which may prevent a proper POR generation. This casuses the MCU to start in an undefined condition. See application notes AN220402 and AN220973 which explain how to prevent a system restart in a voltage-critical area (VCC_{reset} < VCC < VCC_{min}).

Figure 7. All Power Domains Shut Down in Low-Power Mode



Note that this architecture includes also a 6.5-V booster, which is used in many customer applications to ensure stable input voltages for the regulators in case of low battery.

Figure 8. Entering and Leaving Low-Power Mode for Shutdown Power Concept



6 Conclusion

Embedded systems are applied in different environment conditions where stable power supply cannot be guaranteed. In each scenario, the power supply concept in an application must ensure that the recommended operating conditions – specified in the datasheet – are always complied with. Once the power supply is disturbed by a voltage drop, different mechanisms must trigger any action to back up sensitive data and to recover the system smoothly or to act to reduce the load on the related power domain, which allows the system to return to a stable condition.

A power drop on VCC domain to a level above the VCC_{min} and to above the supply detection level of the internal voltage monitor is uncritical regarding the operational conditions of the MCU. However, different applied measures can interrupt the regular system behavior such as reducing the load by switching OFF the display backlight or a reset restarting the application. In both cases, this is an exceptional condition and have an impact to the regular use case of the application. An uninterrupted operation cannot be guaranteed which might be visible to the user (e.g., display flickering).

There are different techniques possible how a power drop can be recognized. To fulfill standard safety requirements, a combination of internal voltage monitors (LVDs) with external voltage supervisors should be used so that different observation levels can trigger appropriate actions.

It is recommended to handle voltage drops on the high-level I/O domain with interrupts exclusively to save sensitive data and to bring the system into a recoverable condition. Potentially, forcing any reset will lead the system into a more critical position and the supply voltage enters a critical area (below VCC_{min}) where the POR generation can only be guaranteed under special conditions. See AN220402 for more information.

7 Definitions, Acronyms and Abbreviations

VCC_{min}	Minimum specified voltage level of supply voltage VCC
V_{reset}	Voltage level of VCC where a power on reset (POR) is issued
MCU	Microcontroller
POR	Power-on reset
LVD	MCU-internal low voltage detection
PSC_1	Enable signal for external voltage regulators

8 Related Documents

- Traveo Family S6J3310/S6J3320/S6J3330/S6J3340 Series 32-bit Microcontroller Datasheet
- AN220402 – Traveo Family MCUs: Power Supply Drop Below Min Supply Voltage But Above Vreset
- AN220973 – Traveo Family MCUs: System Safe Recovery when Power Supply Drops Below Vreset
- AN220338 – Traveo Family MCUs: Intended Power Cycles
- AN220339 – Traveo Family MCUs: Unintended Power Cycles

About the Author

Name:	Peter Berndt
Title:	Staff Applications Engineer
Background:	Peter Berndt has experience in HW design and testing for automotive applications

Document History

Document Title: AN220401 – Traveo Family MCUs: Power Supply Drop Above VCCmin and Supply Monitor Detection Level

Document Number: 002-20401

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5898069	PEBE	09/27/2017	Initial version

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Videos | Blogs | Training | Components

Technical Support

cypress.com/support

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709