AN220339

Test Scenarios of Unintended Power Cycles in Automotive Applications

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Associated Part Family: Traveo™

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It may not be possible to protect the power supply against an unintended power cycle and reset. Therefore, the MCU needs a safe reset logic to ensure that a correct reset always happens. This application note shows typical test scenarios for interruption or disturbance on a car power supply whereby the MCU cannot be powered up from a 0 V level.

1 Introduction

For automotive applications, there are typical test scenarios for interruption or disturbance on the car power supply. In such cases of unintended power cycles, often the MCU must be powered up from a residual voltage level correctly to ensure correct system operation.

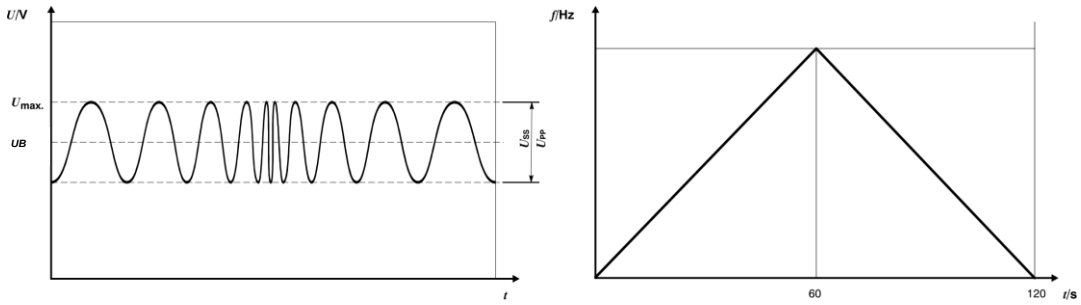
Effects like power fails causing a reset by the low-voltage detector, violation of DC characteristics, and power supply sequencing can occur due to a short interruption or disturbance on the power supply. Therefore, there are several test scenarios for the power supply and I/O pins (diagnosis or sensor input lines) on the system level.

2 Automotive Test Scenarios for Power Supply Disturbances

2.1 Noise Ripple on the Operating Voltage

This involves testing for component immunity to ripple on power supply leads. AC-injected voltages can be superimposed on the vehicle electrical system.

Figure 1. Noise Ripple on the Operating Voltage



Battery voltage (UB) with superimposed sinusoidal AC voltage

Frequency sweep

Frequency range: 50 Hz to 20 kHz, sine waveform, UB = 13.5V,

Severity level 1: Upp = 1 V, Severity level 2 Upp = 4 V,

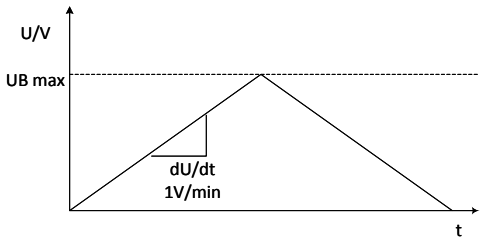
Type of frequency sweep: Triangular, linear

Sweep period: 60 seconds

2.2 Slow Decreasing/Increasing of Operating Voltage

If the operating voltage is reduced from UB max to 0 V (for example, due to a defective alternator or discharging of the car battery), or increased from 0 V to UB max at a rate of 1 V per minute following any subsequent return to operating voltage, no malfunctions shall occur. The voltage decrease/increase shall not cause any memory faults or undefined behavior of port pins (for example, swinging of reset). If a component contains circuits of differing voltage ranges (for example, 5.0 V, 3.3 V, and 1.1 V) the component must not malfunction, or be damaged if these voltages vary within their normal operating ranges.

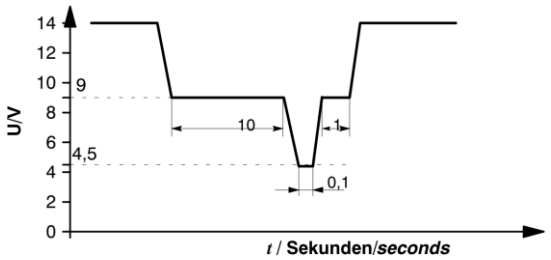
Figure 2. Very Slow Power Ramp-Up and Ramp-Down, Sweep 1 V/min, UB max = 16 V



2.3 Very Brief Voltage Dip

This test simulates the blowing of a fuse in another electric circuit, which typically causes a brief voltage dip.

Figure 3. Very Brief Voltage Dip



Test conditions: 4.5 V ≤ UB ≤ 9 V for t ≤ 100 ms; cycle time T ≥ 20 seconds;

Subject the assembly to the impulse five times in succession.

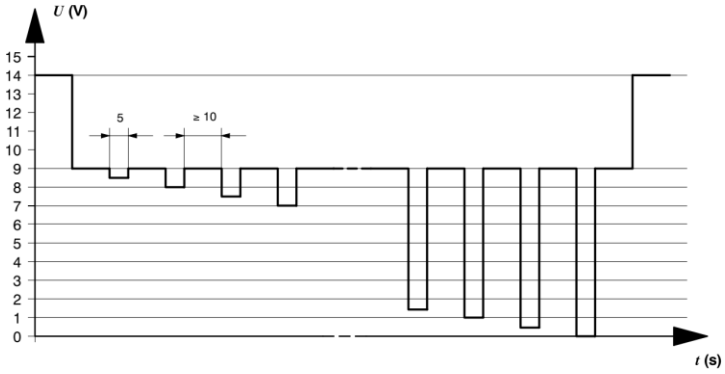
The maximum rise/fall time (10 %, 90 %) is ≤ 10 ms.

2.4 Brief Voltage Dip

This test case simulates the resetting characteristic of an electronic assembly that causes a voltage dip.

Test conditions: 0 V ≤ UB ≤ 9 V; Decrease of operating voltage UB min in 0.5-V steps. For each step, an operational test for ≥ 10 seconds shall be performed.

Figure 4. Brief Voltage Dip



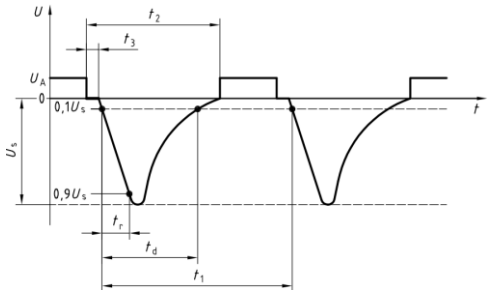
2.5 Voltage Drops Due To Switch-ON of Electrical Loads

Onboard net loads must behave in a manner compatible to the onboard net. Short-term (transient) voltage drops on the onboard net must not lead to perceptible, interfering effects. This applies in particular to periodically recurring interferences. There are several characteristics of start current (peak current up to max 90 A) of load, due to the kind of loads such as capacitive, clocked, or controlled. The load change on the board net occurs at a maximum slew rate of dI/dt = 300 A/s. Due to the impedance of the onboard net and the minimum dynamics of the generator (5 ms dead time of generator) a short-term voltage drop (for 12 V system about Vp= 6 - 7 V and td=50-100 ms) could happen.

2.6 Voltage Impulses Due To Switch-OFF of Inductive Loads

This test relates to Pulses 1 per ISO 7637-2 that simulates transients due to supply disconnection from inductive loads. It is applicable to DUTs which as used in the vehicle that remain connected directly in parallel with an inductive load.

Figure 5. Voltage Impulses Due To Switch-OFF of Inductive Loads



Parameters for test pulse 1

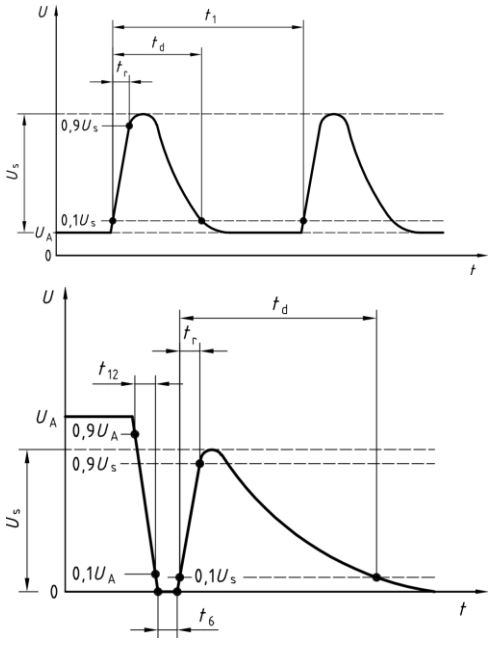
Parameter	12 V system	24 V system
U_s	–75 V to – 100 V	– 450 V to – 600 V
R_i	10 Ω	50 Ω
t_d	2 ms	1 ms
t_r	$\left(1^{\ 0}_{-0,5}\right)$ µs	$\left(3^{\ 0}_{-1,5}\right)$ µs
t_1 [a]	0,5 s to 5 s	
t_2	200 ms	
t_3 [b]	< 100 µs	

2.7 Voltage Impulses Due To Switch-OFF of Transient Loads

This test relates to Pulses 2a and 2b per ISO 7637-2.

Pulse 2a simulates transients due to a sudden interruption of currents in a device connected in parallel with the DUT due to the inductance of the wiring harness. Pulse 2b simulates transients from a DC motor after power is switched OFF.

Figure 6. Voltage Impulses Due To Switch-OFF of Transient Loads



Parameters for test pulse 2a

Parameter	12 V system	24 V system
U_s	+ 37 V to + 50 V	
R_i	2 Ω	
t_d	0,05 ms	
t_r	$\left(1^{\ 0}_{-0,5}\right)$ µs	
t_1 [a]	0,2 s to 5 s	

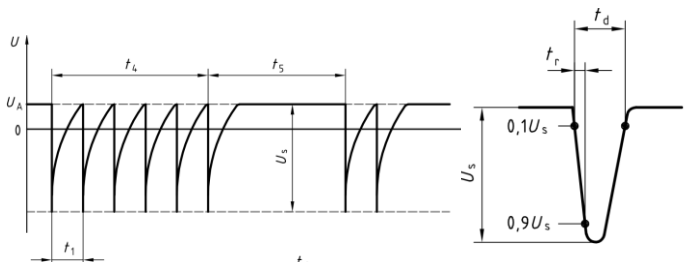
Parameters for test pulse 2b

Parameter	12 V system	24 V system
U_s	10 V	20 V
R_i	0 Ω to 0,05 Ω	
t_d	0,2 s to 2 s	
t_{12}	1 ms ± 0,5 ms	
t_r	1 ms ± 0,5 ms	
t_6	1 ms ± 0,5 ms	

2.8 Voltage Impulses Due To Switching with Fast Transient

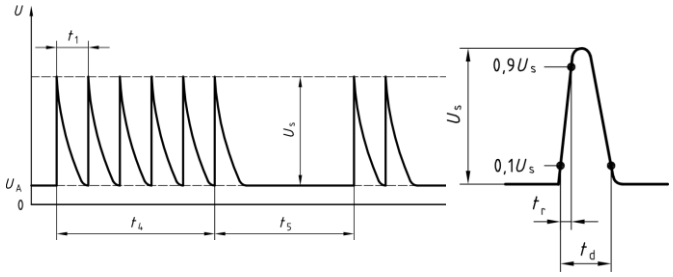
Pulses 3a and 3b per ISO 7637-2 provide simulation of fast transients which occur as a result of the switching processes. The characteristics of these transients are influenced by distributed capacitance and inductance of the wiring harness.

Figure 7. Voltage Impulses Due To Switching with Fast Transient



Parameters for test pulse 3a

Parameter	12 V system	24 V system
U_s	– 112 V to – 150 V	– 150 V to – 200 V
R_i	50 Ω	
t_d	$\left(0{,}1\,^{+0{,}1}_{0}\right)$ µs	
t_r	5 ns ± 1,5 ns	
t_1	100 µs	
t_4	10 ms	
t_5	90 ms	



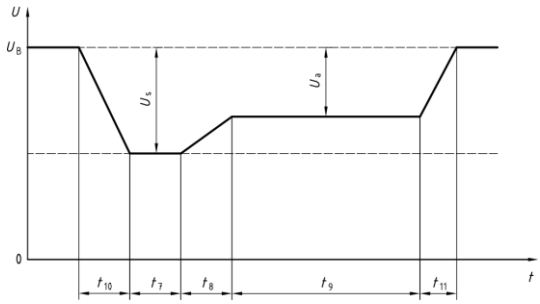
Parameters for test pulse 3b

Parameter	12 V system	24 V system
U_s	+ 75 V to + 100 V	+ 150 V to + 200 V
R_i	50 Ω	
t_d	$\left(0{,}1\,^{+0{,}1}_{0}\right)$ µs	
t_r	5 ns ± 1,5 ns	
t_1	100 µs	
t_4	10 ms	
t_5	90 ms	

2.9 Crank Impulse

Pulse 4 per ISO 7637-2 simulates supply voltage reduction caused by energizing the starter-motor circuits of internal combustion engines.

Figure 8. Crank Impulse



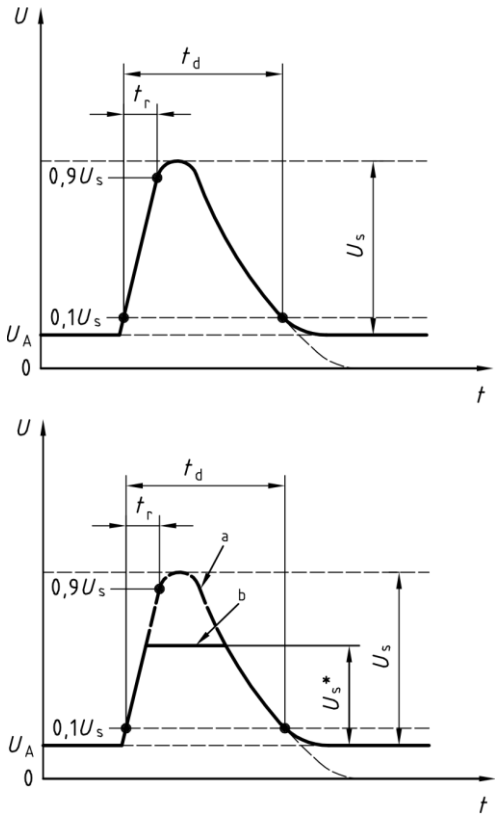
Parameters for test pulse 4

Parameter	12 V system	24 V system
U_s	– 6 V to – 7 V	– 12 V to – 16 V
U_a	– 2,5 V to – 6 V with $\lvert U_a \rvert \leqslant \lvert U_s \rvert$	– 5 V to – 12 V with $\lvert U_a \rvert \leqslant \lvert U_s \rvert$
R_i	0 Ω to 0,02 Ω	
t_7	15 ms to 40 ms [a]	50 ms to 100 ms [a]
t_8	⩽ 50 ms	
t_9	0,5 s to 20 s [a]	
t_{10}	5 ms	10 ms
t_{11}	5 ms to 100 ms [b]	10 ms to 100 ms [c]

2.10 Load Dump Impulses

Pulses 5a/5b per ISO 7637-2 relate to immunity to interference and immunity to transients on power supply lines. This test is a simulation of load dump transient that occurs in the event of a discharged battery being disconnected while the alternator is generating the charging current. The device or system may operate out-of-tolerance from design during exposure to the electromagnetic disturbance, but must return to normal after the disturbance has been removed. During this procedure, storage functions must remain in functional state A.

Figure 9. Load Dump Impulses



Parameters for test pulse 5a

Parameter	12 V system	24 V system
U_s	65 V to 87 V	123 V to 174 V
R_i	0,5 Ω to 4 Ω	1 Ω to 8 Ω
t_d	40 ms to 400 ms	100 ms to 350 ms
t_r	$\left(10\ ^{0}_{-5}\right)$ ms	

Parameters for test pulse 5b (car supply system with external protection unit)

Parameter	12 V system	24 V system
U_s	65 V to 87 V	123 V to 174 V
U_s*	As specified by customer	
t_d	Same as unsuppressed value	

2.11 Protection Against Polarity Reversal

The resistance of the test specimen against polarity reversal during a jump start is tested in this case. Typically, reverse polarity of -14 V / -28 V is tested for 60 seconds.

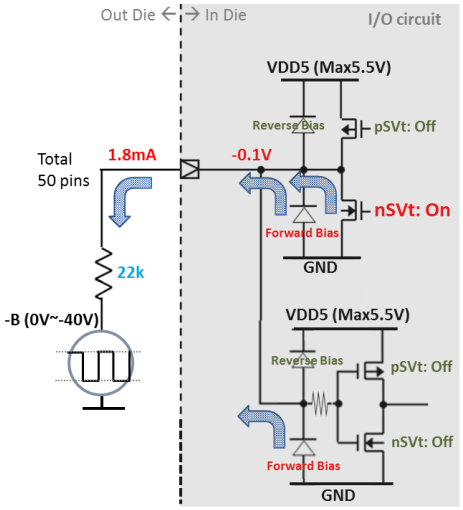
2.12 Extended Requirements for Total Maximum Clamping Current

The (total) maximum clamping current as specified in the datasheet is extended for two dedicated cases under certain limited conditions which are described below.

2.12.1 Case A: MCU in Normal Operation, Pulsed Voltage Applied to I/O Pins

The MCU is operational, I/O is driving LOW level (i.e., NMOS transistor active), negative biased pulses (-B signal) are applied to the active I/O according to the following specification (must not be exceeded).

Figure 10. Case A of Total Maximum Clamping Current: MCU in Normal Operation, Pulsed Voltage Applied to I/O Pins



Pulse condition specification:
U_pulse = max -40V
T_pulse = max 1ms
#_pulse = max 5000

Current and Power Dissipation:
U_peak = -40 V
R_serial = 22 kΩ
I_pin = 1.8 mA (calculated I/O current)

U_out = -0.1 V (current drawn mainly over NMOS transistor)

I_total = 50pins x 1.8 mA = 90 mA
P_total = 50 pins x (1.8 mA x 0.1 V) = 9 mW

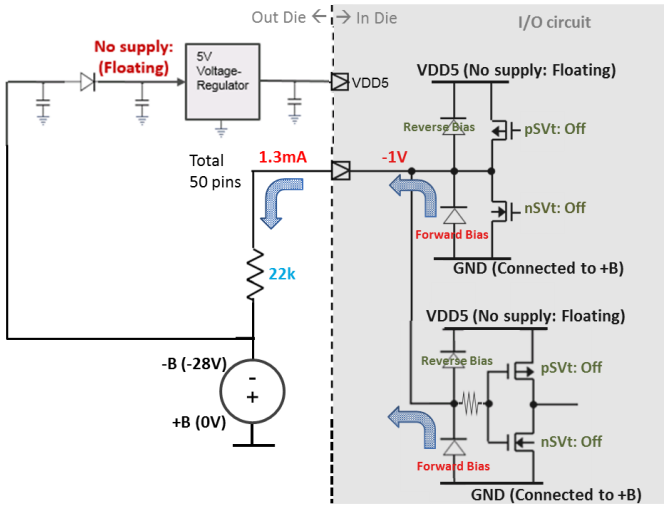
I_total and P_total are within allowed limits of extended specification.

2.12.2 Case B: MCU Non-Operational, MCU Not Supplied Due To Inverse Protection Diode

MCU is non-operational, PCB is in reverse polarity condition (supply of the MCU is OFF), a negative biased voltage level (-B signal) is applied to the inactive I/O according to following specification (must not be exceeded):

No MCU supply due to inverse protection diode on the target board but GND is connected to inverse battery power (14 V/28 V). The I/O is connected to inverse battery power (-28 V) for up to four hours.

Figure 11. Case B of Total Maximum Clamping Current: MCU Non-Operational, MCU Not Supplied Due To Inverse Protection Diode



Reverse polarity condition specification:
U_reverse = max -28 V
T_reverse = max 4 h

Current and Power Dissipation:

U_reverse = -28 V
R_serial = 22 kΩ
I_pin = 1.3 mA (calculated I/O current)

U_out = -0.7 V (current drawn mainly over clamping diodes)

I_total = 50 pins x 1.3 mA = 65 mA
P_total = 50 pins x (1.3 mA x 0.7 V) = 46 mW

I_total and P_total are within allowed limits of extended specification.

3 Summary

For Automotive applications, there are specific requirements and test setups based on the ISO standard and customer approval tests for disturbances on the power supply system within the car. The design evaluation based on simulation data does not cover the influence of disturbance on the power system. Short power interruptions can be a general problem for the MCU power up from a residual voltage level outside the specified operating range.

To avoid such critical scenarios caused by unintended power cycles, there are several automotive power supply concepts and possibilities of smart monitoring of the on-board and on-chip supply. If a power drop is detected (for example, drop on the 12-V car supply), the MCU should be able to start dedicated measures such as writing back the system-relevant data to the nonvolatile memory. Smart monitoring of the power supply is intended to recover the system function by restarting from a residual voltage. Recommendations for the usage of dedicated power supply concepts and smart monitoring of power supplies are shown in the additional application note AN220338 - Traveo Family MCUs: Intended Power Cycles.

4 Related Documents

- AN209861 – Getting Started with the Traveo™ Family S6J3200 Series
- AN203898 – Getting Started with the Traveo™ Family S6J3300 Series
- AN220338 – Traveo Family MCUs: Intended Power Cycles
- AN220401 – Traveo Family MCUs: Power Supply Drop Above VCCmin and Supply Monitor Detection Level
- AN220402 – Traveo Family MCUs: Power Supply Drop Below Min Supply Voltage But Above Vreset
- AN220973 – Traveo Family MCUs: System Safe Recovery when Power Supply Drops Below Vreset

5 References

ISO7637-2 (2004), Road vehicles - Electrical disturbances from conduction and coupling, Part 2: Electrical transient conduction along supply lines only

GS 95003-2 (2003), Electrical/Electronic Assemblies, Motor Vehicles, Electrical Requirements

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