TRAVEO™ Family MCUs: Scenarios of Intended Power Cycles

About this document

Scope and purpose

Low power consumption for ECU in standby mode is a critical requirement for automotive power supply systems. There are different low-power concepts that use intended power supply cycles. The power supply and reset circuit must ensure that correct power sequencing and reset always happens. This application note shows how to ensure that the MCU is powered up correctly to ensure correct system operation.

Associated Part Family

TRAVEO™

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1 Introduction

The standby/sleep current for a typical automotive application must be ≤ 100 µA for the Electronic Control Unit (ECU) measured at the car power supply connector. This requires using power and clock gating, standby, power shutdown mode, and partial wakeup on the MCU device to save power while the ECU is in standby/sleep mode. To ensure that the critical requirements of low power consumption and reduction in leakage current are met, the external power supply must be shut down except for the wakeup circuit. The wakeup circuit is connected to Controller Area Network (CAN), Media Oriented Systems Transport (MOST), and Ethernet (ETH) transceiver. If a dedicated wakeup message is received on one of this communication network, the switchable power supply powers up and the MCU starts with power-on reset (POR)

The general problem of all automotive applications with power up and power down sequencing in a single or multi power supply system is the restart of the system from a residual voltage level. This happens if a critical drop of power supply occurs and the supply system cannot achieve the 0-V level. In addition, system components such as the Microcontroller (MCU), Graphics Display Controller (GDC), and memory require different power up/down and reset sequences.

Cypress TRAVEO™ MCU supports several features for controlling the external power supply with the power save control (PSC) and voltage monitors for the system to apply a valid Power-On Reset (POR).

POR and Power Safe State (PSS) of today's MCU devices have a complex set of reset features to help users ensure the MCU is in the correct state.

When the MCU powers up from 0-V level, a valid POR is achieved. However, if the MCU device has been restarted by an External Reset (RSTX), and then subsequently experiences a drop in supply voltage below the minimum operating voltage where the residual voltage of the MCU supply does achieve a valid POR – i.e., a Brownout – then the MCU may not re-power to the normal operation state. In this case, the MCU may work in an uninitialized and undefined state (malfunction of flash boot controller and freeze of the system).

2 Reset sources

The MCU supports several reset levels to initialize and restart from different states. In principle, there are two ways to hard reset the MCU device:

- POR: Power-on Reset is the traditional way to fully initialize the MCU via power supply control.
- RSTX: External Reset where the device resets all registers and I/O ports to HI-Z only. The MCU restarts faster without the stabilization wait time for oscillator and voltage regulator, and without read of flash and device configuration from the Boot ROM table, because the internal core supply was still stable.

In the case of an external power shutdown, the internal reset logic requires the power supply to be within the valid operating range to propagate the reset through the MCU device, before the MCU goes into power shutdown. See the specified VCC12 core supply and RSTX sequence in the datasheet. In the case of a very fast or short power down scenario on the external core supply, the core might be powered up without the internal reset completed. Therefore, a review of power-safe mode and power cycles is recommended to fulfill the Power and Reset Sequence.

3 Power supply concepts

3.1 Single supply system

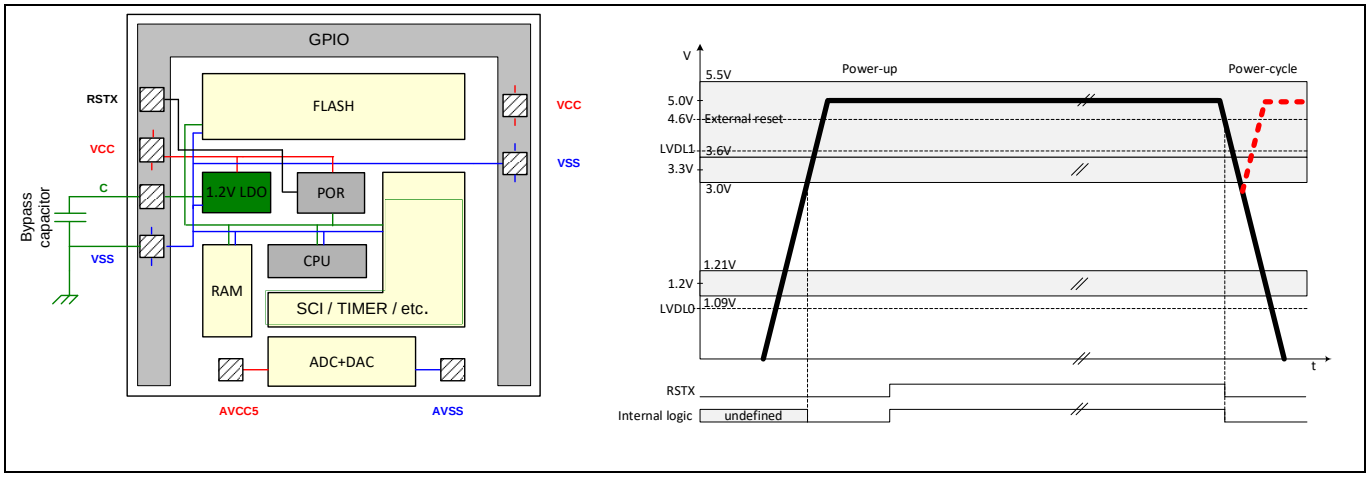


Figure 1 Single supply system

A single power-supply system has one common voltage supply for all power supply pins. This very simple power supply system has no specific requirements for power up or power down. Internal POR does not work if the power cycle is very short, and the drop in VCC does not go below the specified POR threshold level. In such cases, a reset must be effected by using an external voltage supervisor reset.

3.2 Multiple supply system

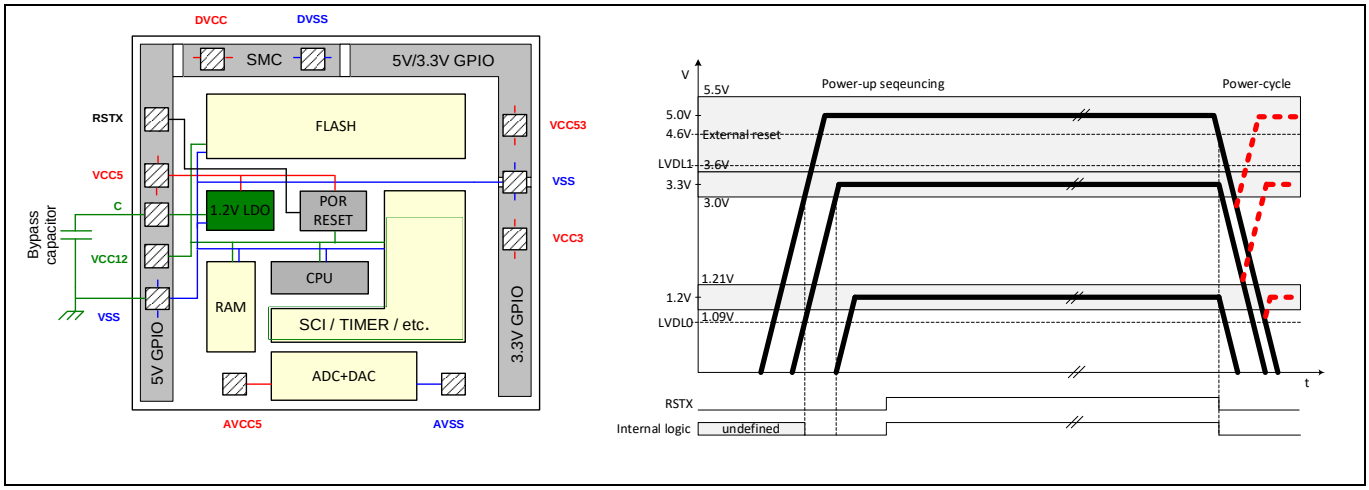


Figure 2 Multiple supply system

A multiple power supply system has several voltage supplies for dedicated power supply pins such as external GPIO5V, GPIO3.3V, and external core supply. External power supplies require a certain power up and power down sequencing to meet recommended operating conditions. Power sequencing should be realized by cascading the external voltage regulators (e.g., primary buck boost regulator for the 5-V domain and secondary voltage regulator for 3.3-V and 1.2-V power domains).

The ‘power good’ output of a voltage regulator is recommended to be used as the enable/disable signal for subsequent voltage regulators. As a result, the 3.3-V voltage regulator is enabled after the 5-V regulator is

activated and the output voltage is stable in the specified range. When the 3.3-V supply is stable, the 1.2-V supply is enabled.

During the ramp up/ramp down time, the external RSTX must be asserted to the active level. The reset hold time of the external reset must cover the external ramp up time plus the RSTX reset input time t_{RSTL}=10 µs.

TRAVEO™ MCUs have several on-chip voltage monitors, of which the LVD0L (internal low-voltage detection for VDD) and LVD1L (external low-voltage detection for VCC5) are able to issue POR and BOD reset.

If the application cannot fulfill the specified threshold level and timing for POR and BOD, the external reset at the RSTX pin is needed. In such cases, you must use an external voltage supervisor circuit.

Usually, VCC5 is the intended power supply for the system pins like oscillator, mode, and reset pins. If the 1.2-V external core supply is shared with other external components such as GDC, both 5-V and 1.2-V power domains must be served by an external voltage supervisor reset.

4 Automotive power supply concepts

Depending on the application, you can use the following power supply concepts and use cases.

4.1 The low-power challenge

The number of ECUs is increasing exponentially in the automotive application area. About 100 and more ECUs are installed in a high-end car these days with control units requiring MCU functionality are replacing passive and mechanical systems throughout the vehicle. Therefore, the low power consumption allowed per ECU is decreasing. For the low-power state, the power consumption is specified ≤ 100 µA for the ECU measured at the KL30 connector. To meet this requirement, there are two main low-power concepts, which must be considered in automotive applications related to an intended shut down of external power supplies during low-power mode.

4.1.1 Concept A: MCU always powered and manages wakeup events

Pros:

- MCU in a low-power mode can still manage wakeup events
- MCU controls the power supply for core and I/Os
- Faster recovery/start up time

Cons:

- In the low-power state, the MCU contributes to power consumption (due do clock gating only)

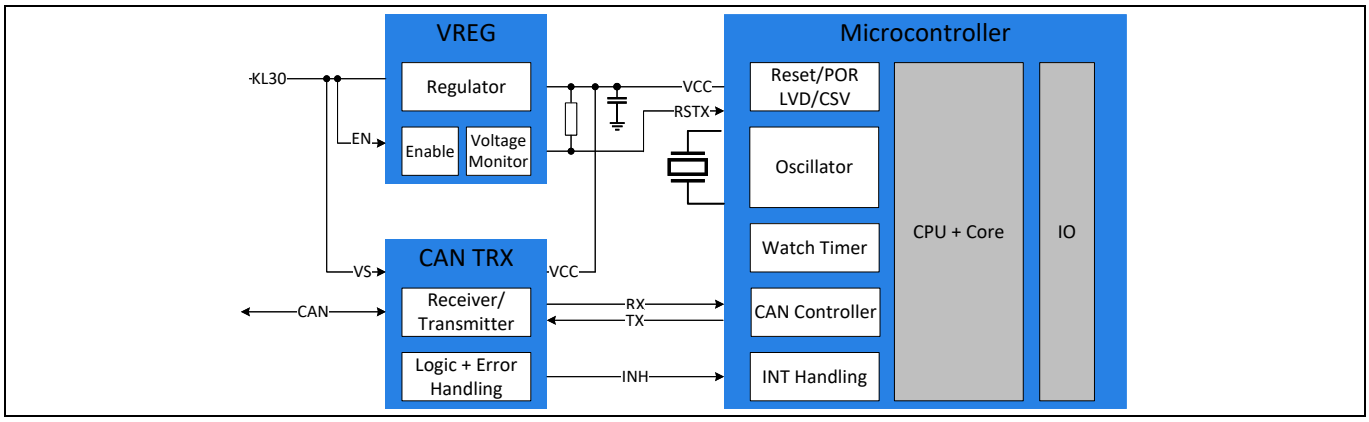


Figure 3 MCU always powered and performs wakeup from low-power state

4.1.2 Concept B: System base chip (SBC) performs wakeup and controls power shutdown of MCU

Pros:

- SBC can manage different wakeup events (partial wakeup), thus allowing the MCU to be unpowered in low-power state
- MCU and peripherals do not contribute to low power consumption at all

Cons:

- Wake up timing is longer (VDD stabilization time, reset timing)
- VCC5 and VCC12 must be stable before releasing the external reset

- Additional time needed for the oscillator of the MCU to start up
- Potential risk for power up from residual voltage level due to very short intended power cycles (e.g., power up before all supplies fully discharged)

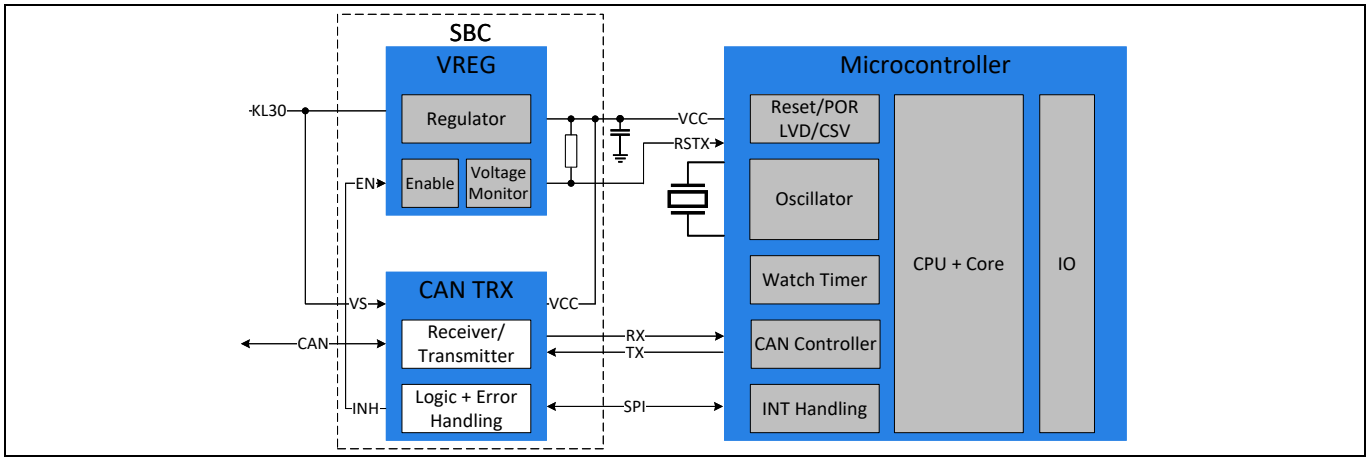


Figure 4 MCU unpowered in low-power state, SBC performs wakeup and controls power enable

Conclusion: For very low power consumption, the power supply for the MCU and I/Os must be switched OFF, which in turn leads to intended power cycles controlled by SBC. Intended power cycles in an application are in principle not an issue.

However, power cycles are a potential risk for power up from a residual voltage level. The residual voltage level is a risk because the internal logic is undefined and often the internal supply monitors do not issue a reset. Therefore, in such cases, the MCU will start up with an undefined logic.

The power down phase is under the control of the MCU and external voltage monitor, but the occurrence of a wakeup event comes from the external system such that both events are asynchronous to each other. Therefore, power off time of the voltage regulator (SBC) is not predictable and by this no minimum time off can be defined. Therefore, in principle it is unavoidable to face scenarios in such applications where a startup/wakeup from a residual voltage level occurs. See Cypress application notes **AN220402** and **AN220973** that provide guidance/measures on how to prevent a system restart from a residual voltage level (VCC_{reset} < VCC < VCC_{min}).

4.2 Power shutdown control

TRAVEO™ MCUs support multiple power supply systems (5-V I/Os, 3.3-V I/Os and 1.2-V core supply) and internal separated low-voltage power domains (for example, PD1 internal 1.2-V always-on domain and PD2 external 1.2-V core domain). Therefore, TRAVEO™ MCUs need a dedicated power up and power down sequence according to the electric characteristics as specified in the datasheet. To reduce the current consumption in the power save mode (PSS), low-level power domains (VCC12 and VCC3) must be shut down when transitioning into the PSS mode. For this reason, the application needs an external circuit to enable the external 1.2-V and 3.3-V regulators. The control of the regulator enable signal via a GPIO pin by the user program cannot be applied, because the GPIO cannot be controlled when the core is not already supplied, and the CPU is running (supply power up phase).

In the worst case, such a system could get into a deadlock situation and the system never starts up. Because of these reasons, Cypress highly recommends to not implement such a system.

Automotive power supply concepts

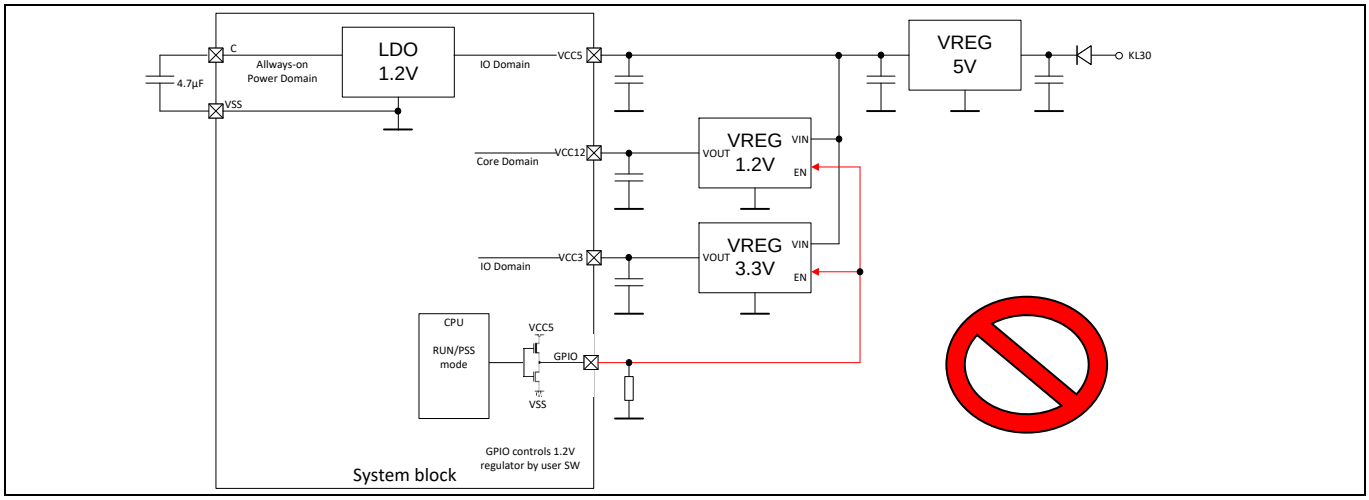


Figure 5 Low-power control with GPIO pin cannot applied for TRAVEO™ MCU

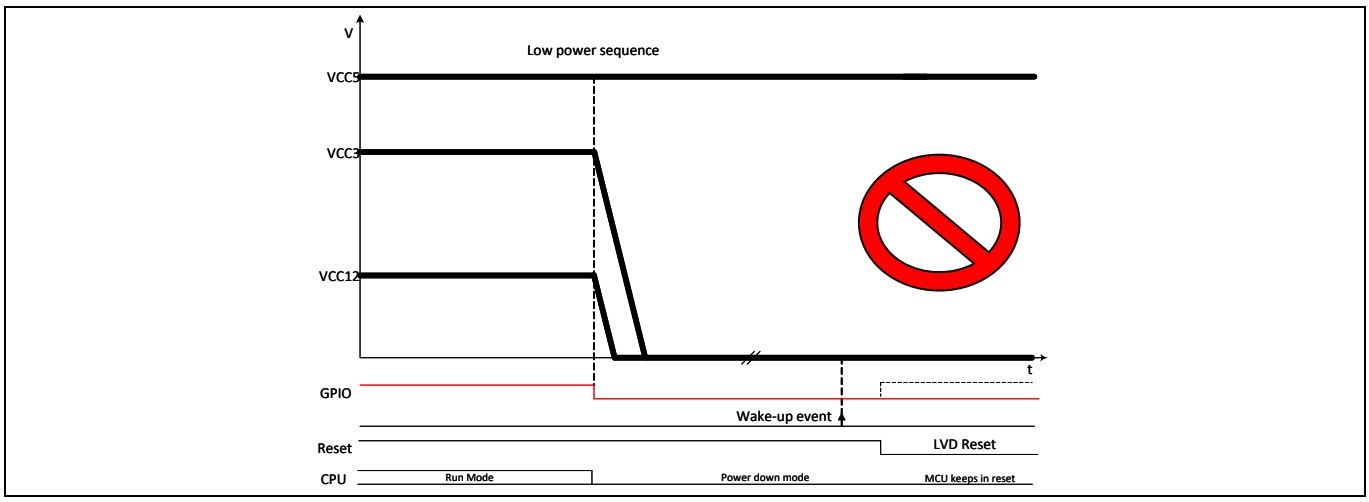


Figure 6 Entering and leaving low-power with GPIO pin generates deadlock

Deadlock: The disable/enable signal of the external core supply by GPIO needs a running CPU, but for restarting the CPU, the core supply must be powered up and stable before the GPIO pin can be activated by the user program. Therefore, TRAVEO™ MCUs offer a dedicated Power Save Control pin that is already activated after VCC5 power up depending on the internal control logic and MCU state transition.

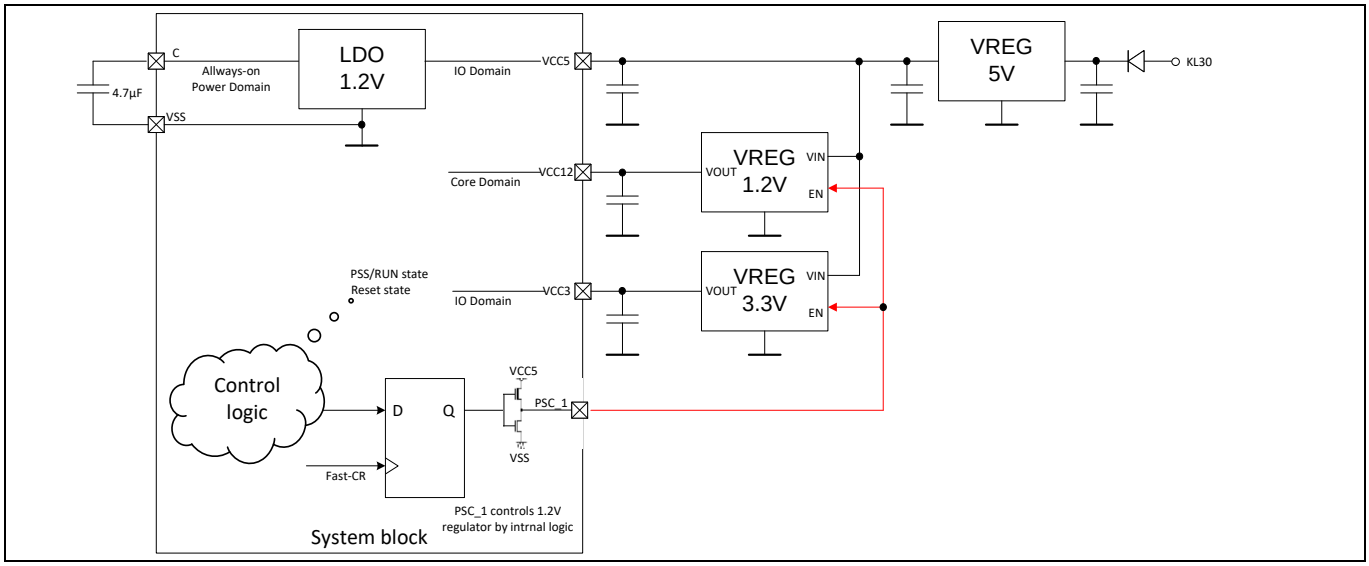


Figure 7 Low-power control with PSC_1 pin intended solution for TRAVEO™ MCU

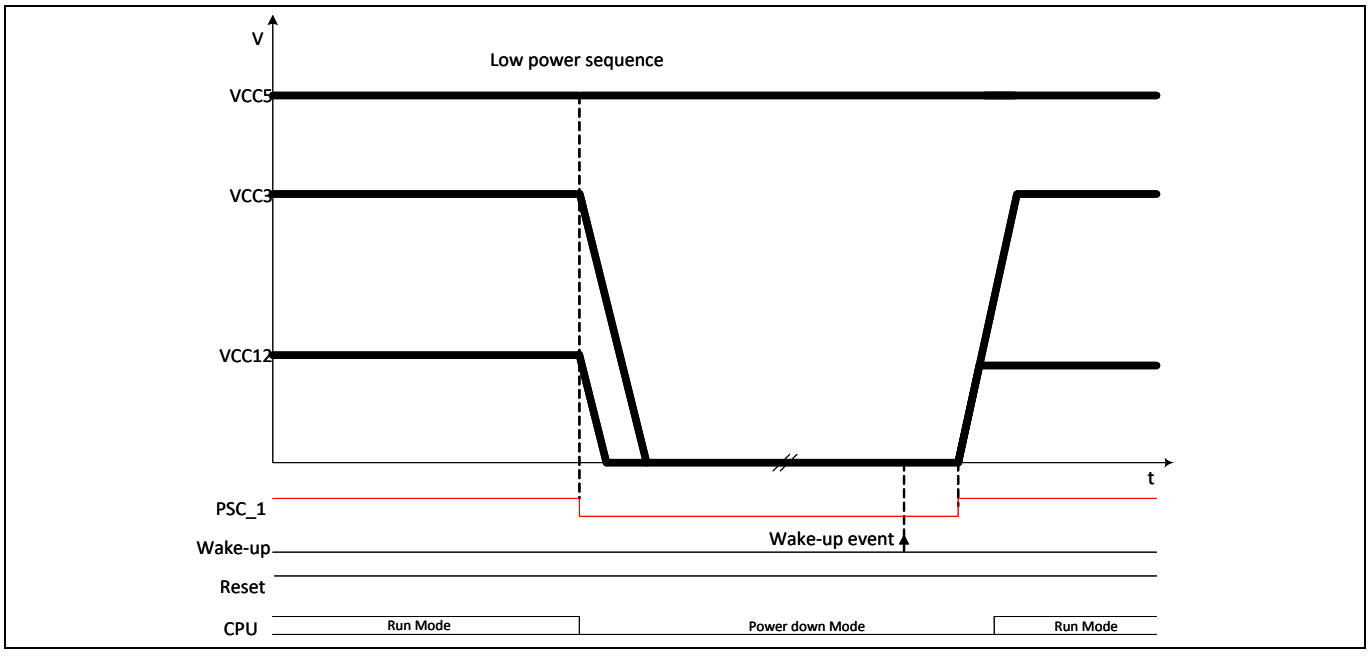


Figure 8 Entering and leaving low-power with PSC_1 pin

Smart Solution: The disable/enable signal of the external core supply is controlled by Power Save Control pin (PSC_1) before the MCU start up is done and the user program is running.

Conclusion: Irrespective of the method implemented (concept A or concept B) in an application, the shutdown control of external regulators via PSC_1 pin must be used.

It is highly recommended to always enter PSS mode before disabling any supply, which guarantees that the internal logic has entered safe state before shutting down. Nevertheless, it is the user application's responsibility to shut down and power up with the required supply sequence. The developer should consider the discharge behavior of the supplies.

4.3 Example for low-power concept A

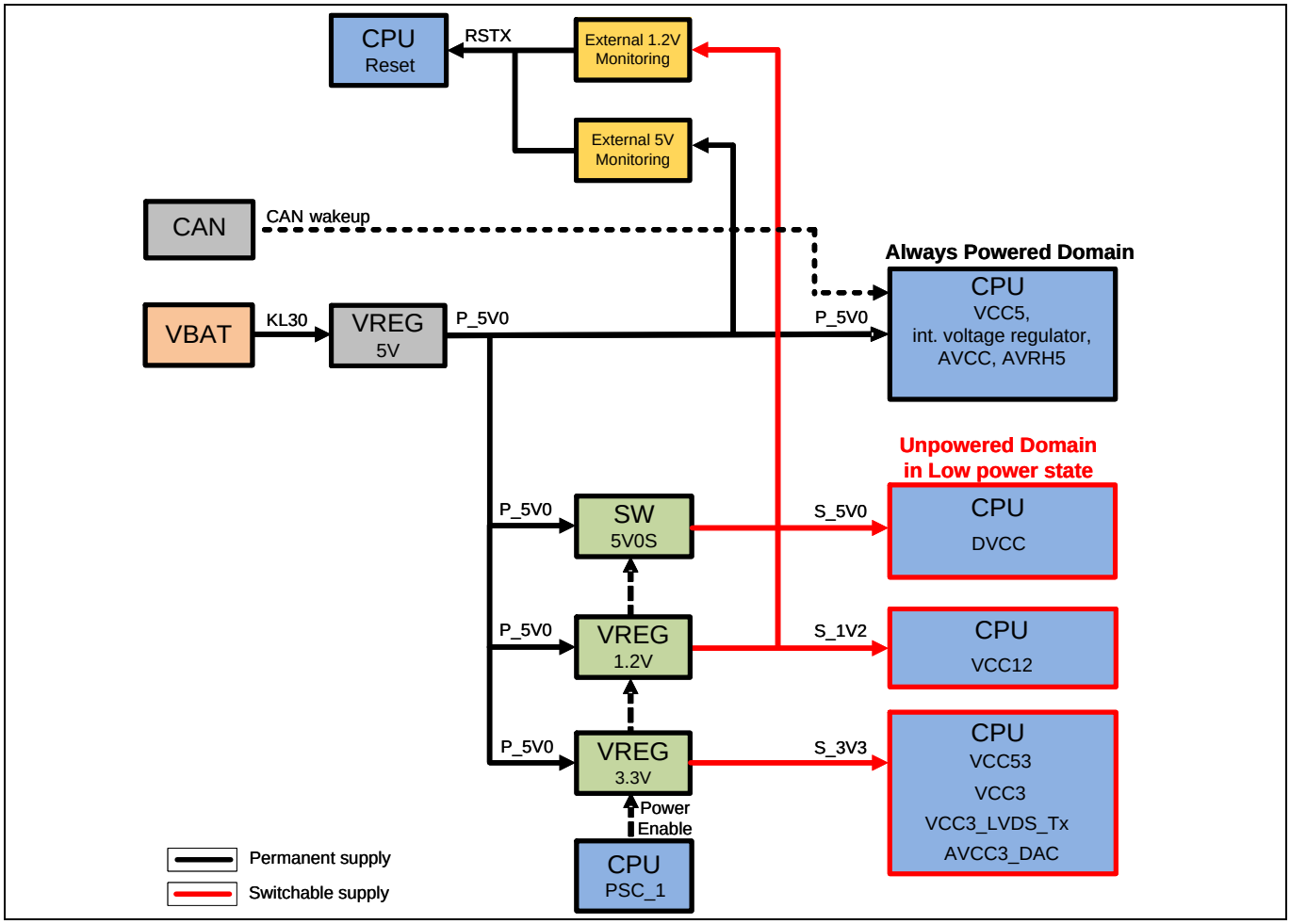


Figure 9 CPU always-ON and all other supplies unpowered in shutdown

The High-Level I/O domain is always supplied. In low-power mode, the external low-level core domain regulator is disabled, but the VCC Always ON domain is still active. The Power Save Control pin (PSC_1) of TRAVEO™ MCUs controls the Power Enable of the switchable external power domains depending on the Power Save, Wakeup, or Reset transition. A wakeup event (for example, RTC timer, push button, or CAN) initializes the MCU and restarts the system after the enable of the external power domain and stabilization of the external core supply. Monitoring of the switchable power domain must be enabled with a GPIO port by the user software in the RUN mode to avoid an external reset during the PSS transition.

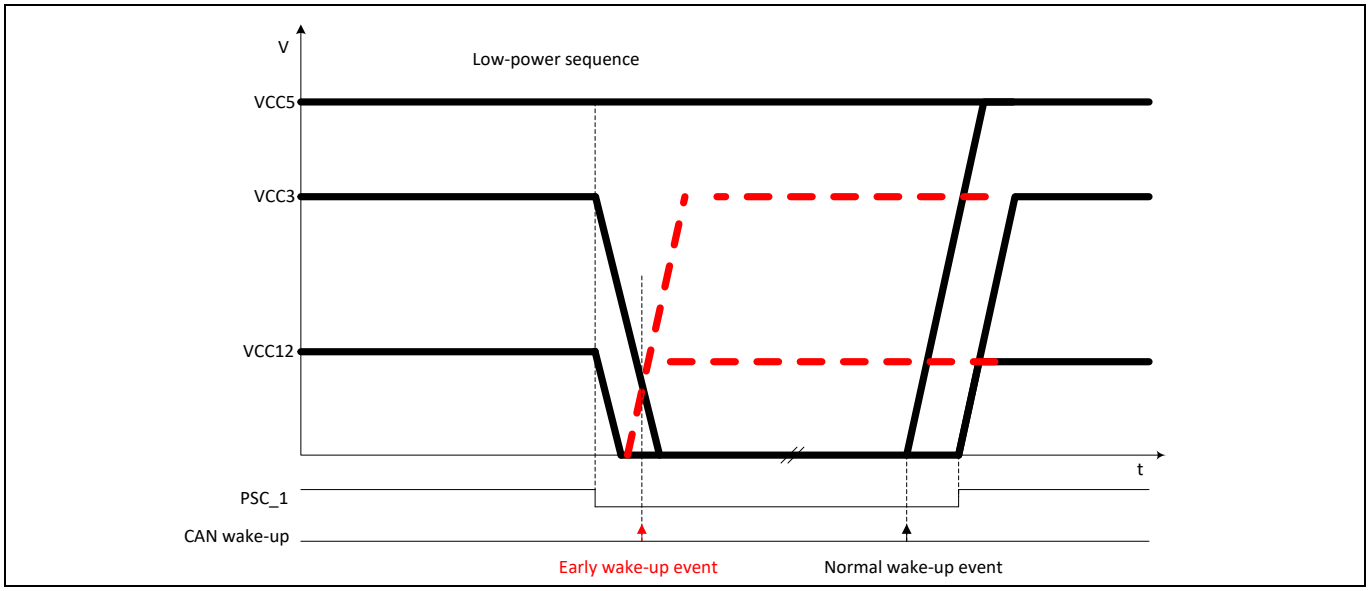


Figure 10 Entering and leaving low-power state for shutdown power concept A

4.4 Example for lower power concept B

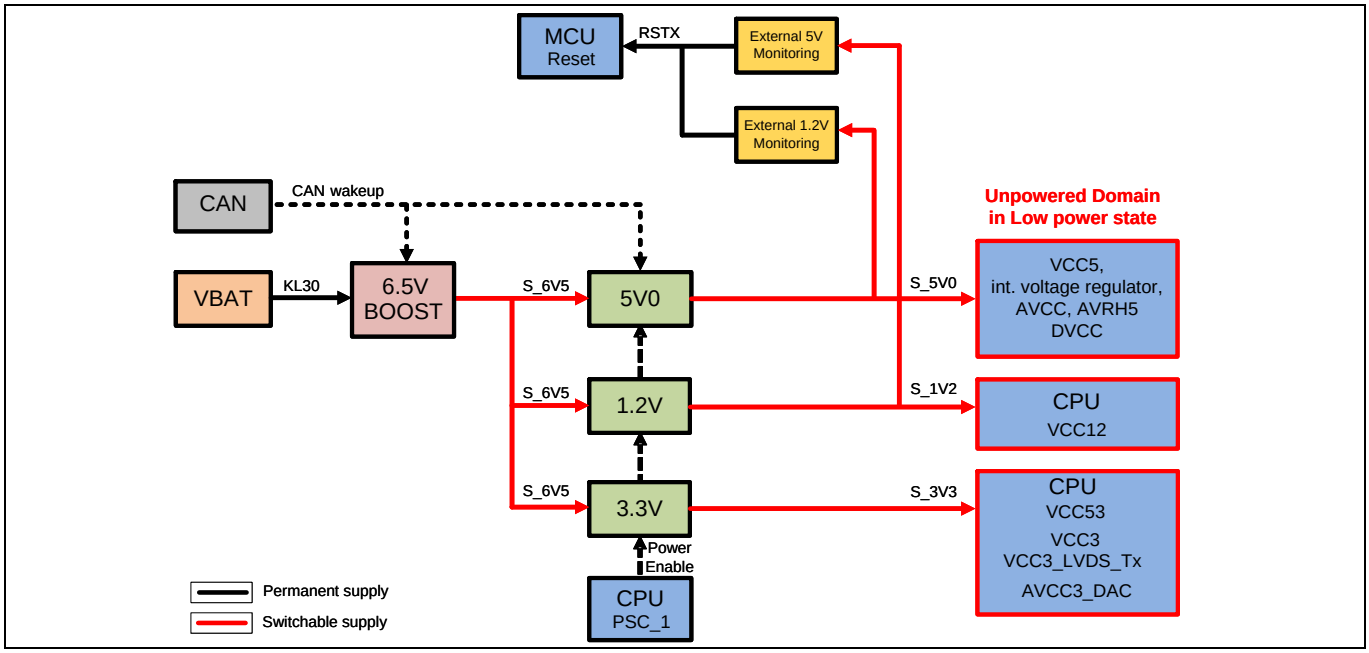


Figure 11 CPU and all other supplies unpowered in shutdown

All power domains including the high-level I/O domain are switchable. The whole system goes in shutdown for minimum power consumption. The MCU receives the shutdown request via CAN. The CAN transceiver is configurable via SPI. In the case of a system shutdown request, the MCU must ensure the following procedure:

1. The CPU restores the relevant system data for system restart to the EEPROM.
2. The CPU reinitializes peripheral functions like CAN and I/O ports.
3. The CPU changes the state of the CAN transceiver to shutdown state.
4. The CPU state transitions to PSS mode to disable low-level power domains and completes an internal reset for flash and control logic before the whole system power is down (not recommended).

Automotive power supply concepts

5. The CAN transceiver disables the high-level power domain to archive whole system shutdown.

A wakeup event (for example, CAN or push button) enables power supplies and restarts the system as follows:

1. The CAN transceiver enables the high-level power domain.
2. The CPU restarts the control logic and enables the PSC_1 pin for low-level power domains.
3. The CPU restarts the system after the enable of the external low-level domain and stabilization of the external core supply. Monitoring of the switchable power domain must be enabled with a GPIO port by the user software in the RUN mode to avoid an external reset during the PSS transition.
4. The CPU initializes the CAN transceiver via SPI to active mode and sends alive message to the top-level system.

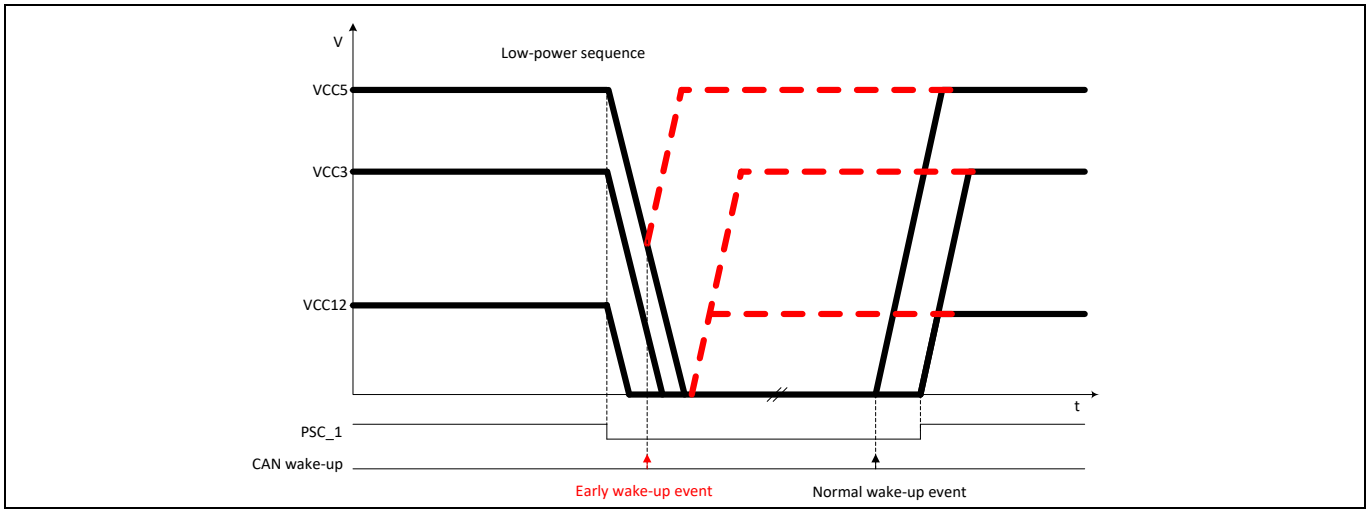
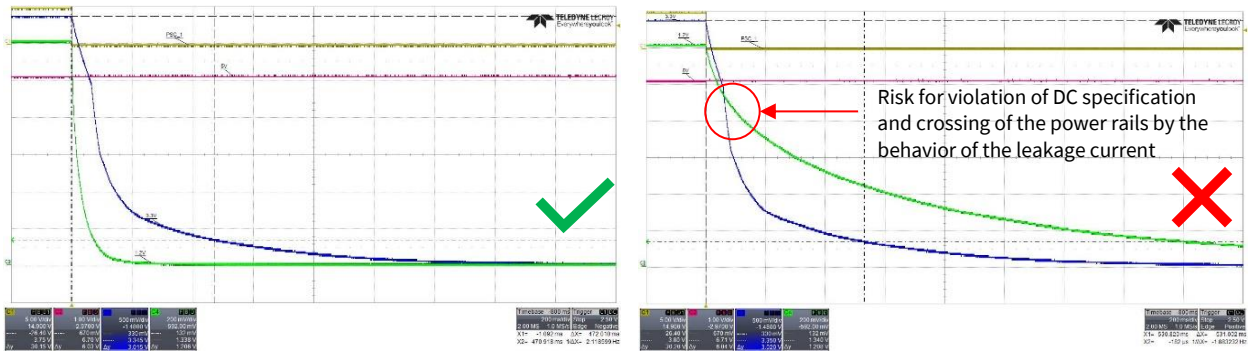


Figure 12 Entering and leaving low-power state for shutdown power concept B

5 How to avoid residual voltage

The general problem of all different power supply scenarios is the transition from RUN to PSS mode. Discharging of power supply domains depends on the number of buffer capacitors and leakage current of the CPU and peripherals in the PSS or RESET state. The variation of leakage current depends on the ambient temperature. The worst case is usually the very little leakage current at low temperature on the silicon. The internal LDO voltage at the C-pin is also affected by the problem with residual voltage in the case of a very short PSS power OFF time.

The following graphs show the impact of temperature and leakage on power OFF discharging time.



Discharging for 3.3 V and 1.2 V @25°C

Discharging for 3.3 V and 1.2 V @-40°C

Figure 13 Impact of temperature and leakage on power OFF discharging time

To prevent any drop of the 1.2-V core supply, you should consider using 10-µF buffer capacitors on all four sides of the packages. On the other hand, there is a potential risk for restarting the MCU from a point of residual voltage instead of the 0-V level.

Therefore, the application cannot ensure that the power OFF time was long enough for discharging of the MCU supplies below the specified POR threshold level.

5.1 Best practice to avoid residual voltage

In the case of switchable multiple power supply domains, see application notes **AN220402** and **AN220973** providing more details.

5.2 Best practice at system level

Any device/component used in a system must support a reset input and sufficient reset level in order to guarantee a safe start up (no uninitialized logic or configuration registers are allowed inside device/component).

Typical power cycle in the case of an intended power shutdown and wakeup is shown in **Figure 14**.

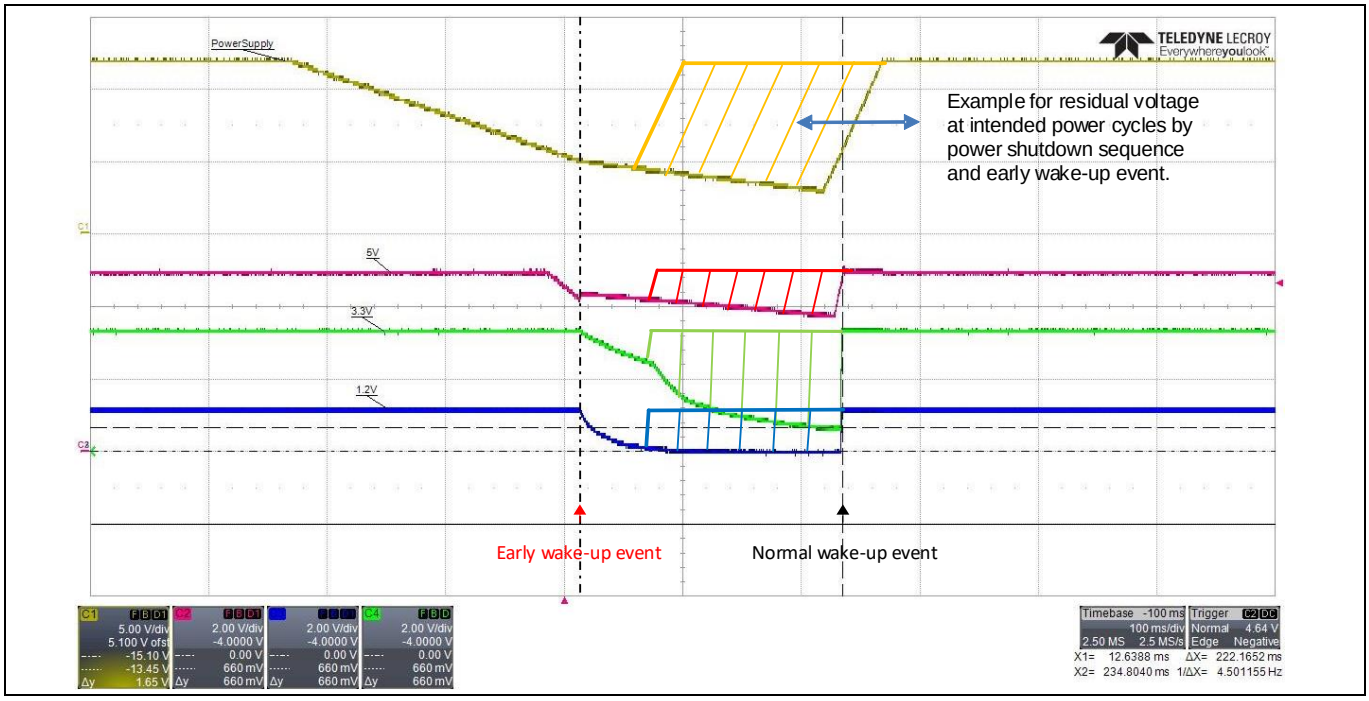


Figure 14 Typical power cycle versus discharging of 5 V, 3.3 V, 1.2 V @ 25°C

The following typical shutdown scenarios cause these supply scenarios:

1. The ECU starts by CAN wakeup on each CAN message.
2. The ECU is in normal operation mode.
3. The CAN gateway sends a sleep request to the ECU (Key-off state).
4. The ECU checks the active messages on the CAN bus.
5. If all conditions are fulfilled, the ECU enters power shutdown.
6. Any further activities on the CAN bus such as door open, or remote control restarts the ECU.
7. Repeating from Step 4 again until the CAN communication is completely down.

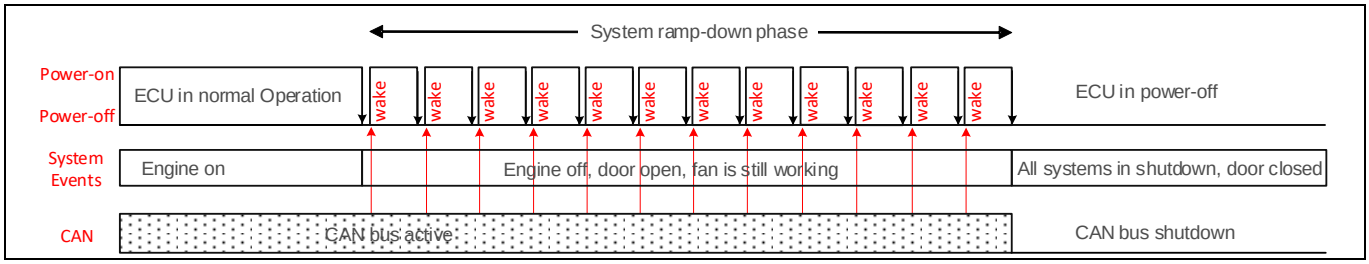


Figure 15 System-level diagram of cluster instrument with risky shutdown architecture

Use the following best practices on system level to reduce the probability of power cycling with start up/wakeup from a residual voltage level (System architecture measure).

How to avoid residual voltage

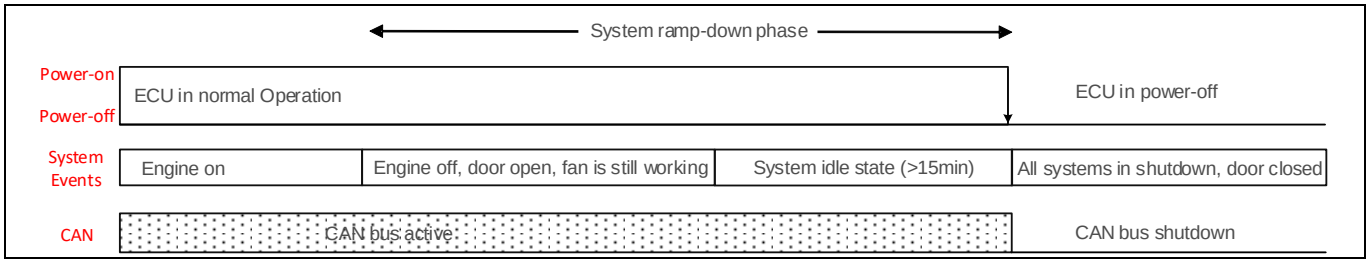


Figure 16 System-level diagram of cluster instrument with improved shutdown architecture (A)

The ECU waits for CAN bus shutdown after a CAN message for power shutdown is received. The ECU keeps active for listening on the CAN bus. After a CAN bus Idle time >15 minutes, the ECU goes into power shutdown.

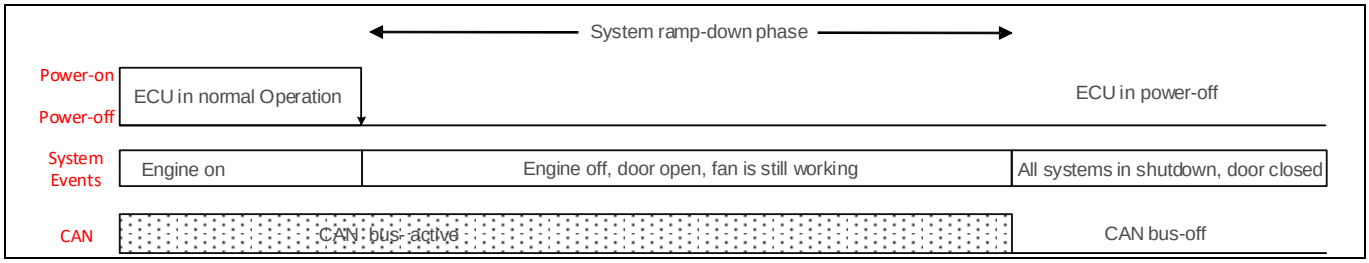


Figure 17 System-level diagram of cluster instrument with improved shutdown architecture (B)

The ECU uses the CAN transceiver with partial CAN wakeup on a dedicated wake-up message. After a CAN message for power shutdown is received, the ECU goes into power shutdown immediately. CAN nodes of remaining ECUs of the system that are still active cannot wake up the ECU without the dedicated wakeup message.

6 Summary

Today’s microcontrollers use multiple power supply systems due to the low voltage core supply for the technology and the required supply of 5 V, 3.3 V or 1.8 V for general-purpose I/O ports (GPIO). For a correct startup of the MCU, there are datasheet-specified requirements for the power up sequence and reset circuit; especially for the transition to the power save state and wakeup of the application, the intended power cycle needs to be reviewed. During the ramp-up and ramp-down of power supplies, the MCU must be kept in a safe reset state. To avoid power up of the MCU from a residual voltage, using an external voltage regulator (PMIC) with active discharging and a smart system architecture is recommended.

7 Definitions, Acronyms and Abbreviations

Table 1 Definitions, Acronyms and Abbreviations

Terms	Description
CAN	Controller Area Network
ECU	Electronic Control Unit
ETH	Ethernet
GDC	Graphics Display Controller
GPIO	General Purpose IO Port
LVD	MCU-internal low voltage detection
MCU	Microcontroller
MOST	Media Oriented Systems Transport
PMIC	Power Management IC (voltage regulator)
PD1	internal always-on power domain of TRAVEO™ MCU
PD2	external core power domain of TRAVEO™ MCU
POR	Power-on reset
PSC	Power Save Control
PSC_1	Enable signal for external voltage regulators
PSS	Power Save State
RSTX	External reset input
SBC	System Basis Chip
VCC_{min}	Minimum specified voltage level of supply voltage VCC
V_{reset}	Voltage level of VCC where a power on reset (POR) is issued

8 Related documents

- **AN209861 – Getting Started with the Traveo™ Family S6J3200 Series**
- **AN203898 – Getting Started with the Traveo™ Family S6J3300 Series**
- **AN220339 – Test Scenarios of Unintended Power Cycles in Automotive Applications**
- **AN220401 – Traveo Family MCUs: Power Supply Drop Above VCCmin and Supply Monitor Detection Level**
- **AN220402 – Traveo Family MCUs: Power Supply Drop Below Min Supply Voltage but Above Vreset**
- **AN220973 – Traveo Family MCUs: System Safe Recovery when Power Supply Drops Below Vreset**

Revision history

Document version	Date of release	Description of changes
**	2017-12-21	New application note.
*A	2021-06-24	Updated to Infineon template.

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