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Usage Guide for S6BP Series PMICs for Safety Applications

About this document

Scope and purpose

AN219802 provides design guidelines on how to implement Cypress S6BP Series automotive-grade power management IC as a power supply for electronic devices including Cypress Traveo™ MCU in an automotive electric and electronic system that targets ISO 26262 functional safety standard.

Associated Part Family

S6BP20xA, S6BP401A, S6BP50xA

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1 Introduction

Cars today are getting more electrified and the electronic equipment is getting sophisticated. More and more semiconductor devices are integrated in an electrical control unit (ECU), facilitating drivers' safety. For these ECUs, a power supply failure is a significant hazard; therefore, the functional safety for power management IC (PMIC) must be taken into consideration when implemented in a system. Cypress offers safety-aware PMICs that are used in conjunction with safety microcontrollers to ensure the power supply for the safety applications.

This application note provides design guidelines on how to implement Cypress automotive-grade PMIC as a power supply for electronic devices including Cypress Traveo™ microcontroller unit (MCU) in an automotive electric and electronic system that targets ISO 26262 functional safety standard.

This application note supports the devices listed in **Table 1**. For the sake of simplicity, hereinafter, all the supported devices are referred as "S6BP series PMIC" or "S6BP" in short. This application note describes the function of this device relevant to functional safety and gives guidelines on its usage.

Table 1 S6BP Series PMICs covered in this document

	S6BP201A, S6BP202A, S6BP203A	S6BP401A	S6BP501A, S6BP502A
Description	42 V, 2.4 A Synchronous Buck-Boost Converter	6-ch PMIC	3-ch PMIC
Target application	• Body control • Instrument cluster • Advanced driver assistant system (ADAS)	ADAS	Instrument cluster
# of regulators	1	6	3
Type of regulators	Primary	Secondary	Primary + secondary

2 S6BP series PMIC features

S6BP series PMICs regulate one or more power rails to supply electrical power to the electric and electronic devices. Plus, they provide safety functions to help the system satisfy the ISO 26262 safety requirements.

The rest of this section gives the list of the features of S6BP series PMICs. Note that all the features are not always provided by a single device. Please consult the datasheets for which features are available with your S6BP series PMIC, and install appropriate external measures if additional safety requirements need to be satisfied.

2.1 Voltage regulators

S6BP series PMICs provide one or more switching-mode power supply (SMPS), zero or more low-dropout regulators (LDO), and one voltage regulator for inner circuitry.

- DD*n* regulator
  The DD*n* regulator is a buck / boost / buck-boost DC-DC converter. The high-side MOSFET and low-side MOSFET are integrated in the device. The output voltage, output current, and switching frequency depend on the device and the channel number (*n*).
- DD*n* controller
  The DD*n* controller provides two MOSFET gate drivers to drive the external high-side MOSFET and the external low-side MOSFET for a buck regulator. A load switch is accompanied with the controller.
- LD*n* regulator
  The LD*n* regulator is an LDO intended to supply power to noise-sensitive devices. The output voltage and output current depend on the device and the channel number (n).
- VB regulator
  The VB regulator is an LDO dedicated to supply inner circuitry.

2.2 Power-good

S6BP series PMICs provide active-high open-drain indicators for each voltage regulator to show whether the output voltages are in the prescribed range. In case the S6BP series PMIC fails to regulate any of the power rails, the device detects the error and deasserts the Power-Good signal.

2.3 Watchdog timer

S6BP series PMICs provide a window watchdog timer to ensure the integrity of the microcontroller used in the system. In case the microcontroller in the system stops responding, the watchdog timer detects it and asserts a reset signal to the microcontroller.

2.4 Thermal warning

S6BP series PMICs provide an active-low open-drain indicator to show when the device temperature is as hot as +140 °C, which is close to the boundary of its operational range. The temperature is monitored locally aside the voltage regulators.

3 How to use in safety applications

This section describes how the S6BP series PMIC is recommended be used with Traveo family MCUs, which are automotive-grade microcontrollers from Cypress, whenever the application is safety-related.

An instrument cluster system is taken as an application example of interest. As illustrated in **Figure 1**, the instrument cluster comprises speedometer, gas gauge, tachometer, coolant temperature gauge, gear position indicator, telltales and a color TFT LCD. **Figure 2** depicts a block diagram of the system where the S6BP series PMIC and Traveo family MCU are used. An implementation example with S6BP502A and Traveo S6J3200 MCU is shown in **Figure 3**. Note that that the bypass capacitors for Traveo MCU are not illustrated; refer to the Technical Reference Manual of the Traveo family for the requirements for bypass capacitors.

Figure 1 Instrument cluster system

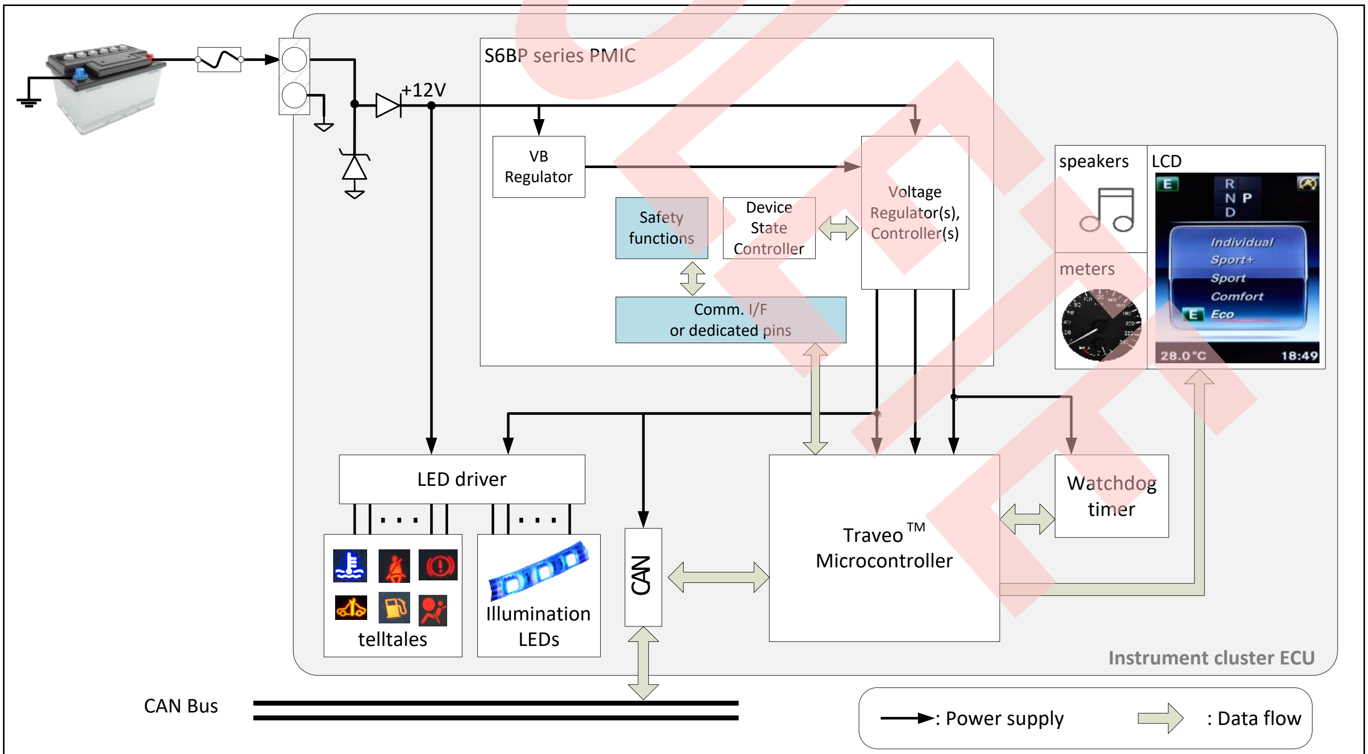

Figure 2 Instrument cluster block diagram

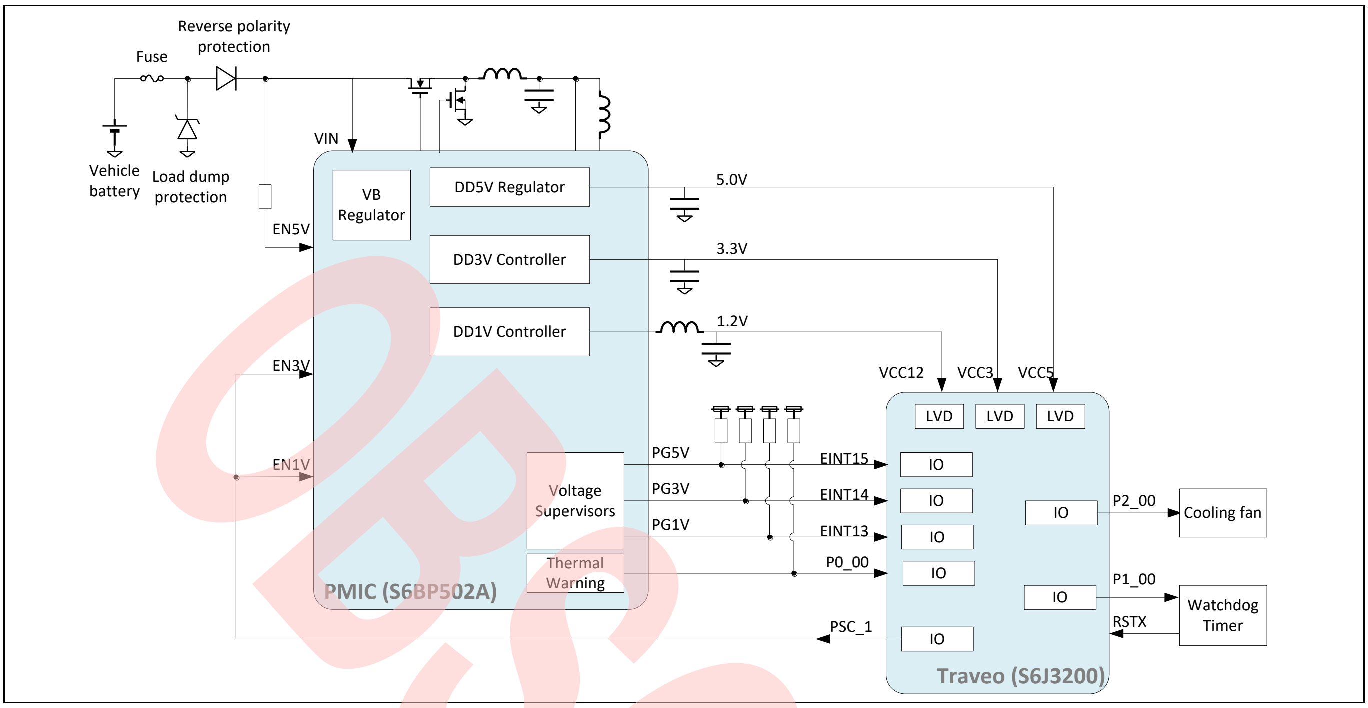

Figure 3 Implementation example with S6BP502A and Traveo S6J3200

3.1 Safe state definitions

To mitigate the risk of hazards that result from failures in the system, the system must use safety mechanisms. In this document, the states in **Table 2** are assumed to be safe.

Table 2 Safe states for the assumed system

State name	Description
SysSafe-1 state	The system has a blank screen on the LCD while the Traveo MCU is unpowered. It is assumed that the system is designed in a way to show nothing (blank screen) on the LCD when the Traveo MCU is unpowered in order not to give false information to the driver. The transition from powered to unpowered state and the other way around is expected to be covered by the system to maintain this safe state.
SysSafe-2 state	The system has a blank screen on the LCD while the Traveo MCU is being reset. It is assumed that the safety-related signals are kept in safe states during the reset state without proper control by the Traveo MCU. Pull-down resistors and pull-up resistors are typically used.
SysSafe-3 state	The system is working correctly in fault-free condition (e.g., correct software execution, correct representation of the safety-related graphical information, warning icons.) It is assumed that the system maintains its safe state if the Traveo MCU is free of faults and operates correctly.
SysSafe-4 state	The system is working with errors being detected. The failure detection state of the MCU after a safety mechanism detected any failure and reacted appropriately (such as activated/deactivated an external error notification pin, automatically disabled the display output, display output resulting in no picture at all or in a blank screen). It is assumed that the system enters and maintains its safe state if a failure in the MCU has been detected and reported. This is expected to be done within the appropriate fault tolerant time interval.

3.2 Safety mechanisms

To detect the faults that may harm safety, the system must make use of safety mechanisms provided by the S6BP series PMIC, Traveo MCU, and other devices.

3.2.1 Power fail management

Power rail regulation faults cause malfunction of the devices including the Traveo MCU. The Power-good feature of S6BP series PMIC detects the faults, and it should trigger safety mechanisms to bring the system to a safe state.

- The integrator shall choose an appropriate S6BP series PMIC, whose Power-good monitor window is appropriately set inside of the operational voltage range of Traveo.
- The Power-good signals (PG) should be pulled up to 5.0−V power rail through resistors of the order of 100 kΩ.
- The PG signal should be connected to the Traveo MCU's interrupt inputs. Upon receiving a low-level interrupt signal, the MCU can transition into a SysSafe-4 state.

Note: Apart from the Power-Good signals, the Traveo MCU equips low-voltage detection (LVD) mechanisms that monitor the integrity of its own power sources.

3.2.2 Power-up sequence management

To provide safe power-up, S6BP502A equips an undervoltage lock-out (UVLO) function that prevents contingent and/or uncertain operation of the device under low-supply conditions.

Enable (EN) terminals should be controlled by PG or by the Traveo MCU to configure an appropriate power-up sequence for the system. **Figure 4** illustrates the power-up sequence configured in **Figure 3**. When the input voltage (VIN) becomes higher than the UVLO threshold, the VOUT5V is being charged up gradually with the soft-start mechanism. The charge-up completion of VOUT5V is communicated to the Traveo MCU with the PG5V signal, starting the initialization. At the end of initialization, the Traveo MCU asserts PSC_1, which is connected to EN3V and EN1V, to power up VOUT3V and VOUT1V.

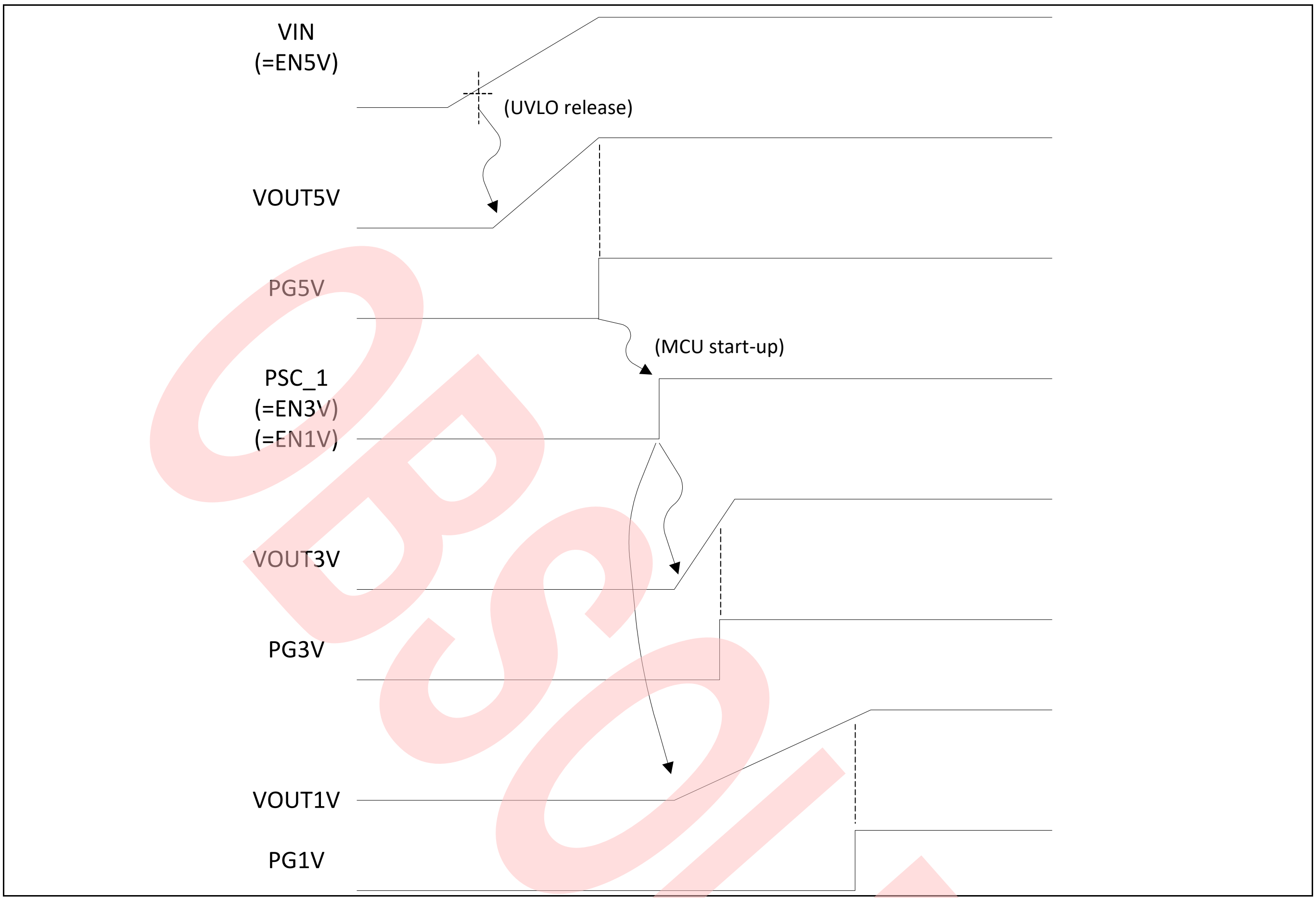

Figure 4 Power-up sequence

3.2.3 Thermal management

Overheating causes malfunction of devices. Even though the devices usually shut themselves down in overheat conditions to be safe, it is recommended to manage heating before losing the system's functionality.

- The thermal warning signal (HOT) should be pulled up to 5.0-V power rail through a resistor of the order of 100 kΩ.
- The HOT signal can be connected to the Traveo MCU for being monitored regularly.
- Upon receiving the HOT signal, the Traveo MCU can cool the system or reduce heat dissipation (e.g., turning ON a cooling fan, dimming the LCD backlight).

3.2.4 Watchdog timer

Because the Traveo MCU plays an important role for safety, its hang-up or malfunction must be detected and handled properly to bring the system into a SysSafe state. To detect failures of the Traveo MCU, the system must equip a watchdog timer independent of the Traveo MCU. In **Figure 3**, a dedicated watchdog timer is installed in the system, but you can use the one integrated in S6BP series PMICs. See **Table 1** to find which device provides a watchdog timer.

- The watchdog timer should be fed by the Traveo MCU. It applies an asynchronous reset to the Traveo MCU in case it finds discrepancies.
- The watchdog timer may drive other safety mechanisms that are independent of the Traveo MCU.

3.2.5 Requirements for external components

In order not to apply electrical overstress (EOS), which damages S6BP series PMICs, the following external devices must be installed in the system.

- Reverse polarity protection
  To protect the devices from reverse polarity battery connection, which is caused by human errors on battery replacement, a rectifier diode shall be installed between the vehicle battery and VIN terminal.
- Load dump protection
  To protect the devices from load dump surge caused by the disconnection of the vehicle battery from the alternator while the battery is being charged, a transient voltage suppressor (TVS) shall be installed to clamp the surge voltage up to 48 V.
- Fuse
  Though the S6BP series PMIC provides overcurrent protection, it is highly recommended to install a fuse to prevent the devices from being damaged by unexpected high current. A proper selection of fuse is necessary.

3.2.6 Open/short-fault management

Figure 5 illustrates the connections among a vehicle battery, a PMIC and a Traveo MCU. To simplify the analysis, and to provide common principles, **Figure 5** takes a general PMIC. The balloons in the figure show the positions of possible open-faults and short-faults related to the PMIC. **Table 3** and **Table 4** respectively show how open faults and short faults are brought to a SysSafe state.

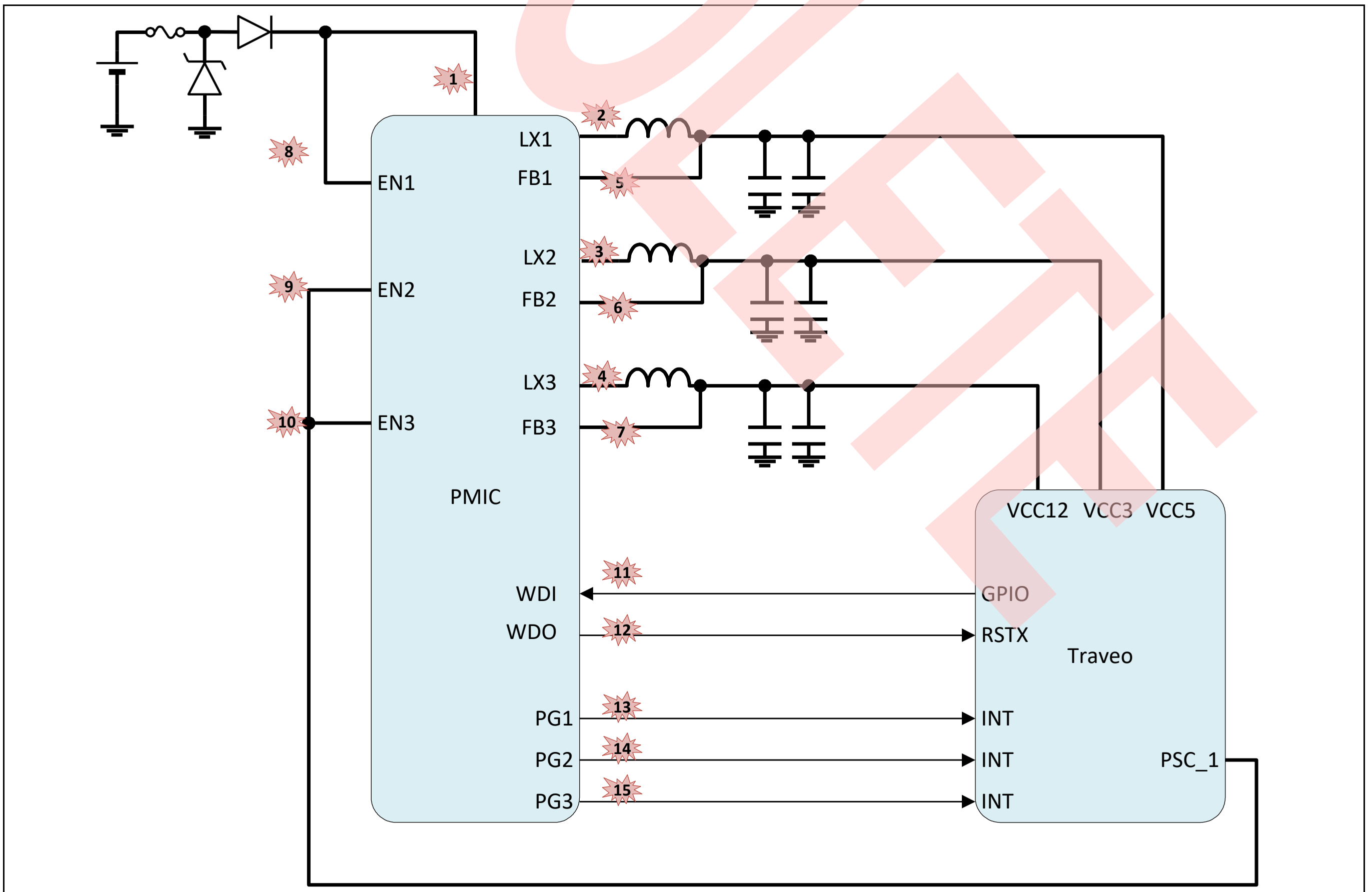

Figure 5 **Faults handled by MCU and/or PMIC**

Table 3 Open fault handling

Position	Fault mode	Results in	Description
1	open	SysSafe-1	Due to the UVLO function, a battery line open-fault deactivates the power rail regulation. The Traveo MCU becomes unpowered, and the system turns into SysSafe-1 state.
2, 3, 4	open	SysSafe-1	An inductor pin (LX) open-fault deprives the S6BP series PMIC of the path to charge the power rail. The Traveo MCU becomes unpowered, and the system turns into SysSafe-1 state.
5, 6, 7	open	SysSafe-4	A feedback pin (FB) open-fault results in charging the power rail voltage until its overvoltage protection (OVP) threshold. Before reaching the OVP threshold, however, Power-Good signal (PG) is asserted and the Traveo MCU should activate safety measures (e.g., showing warning message on the LCD) to bring the system into SysSafe-4 state before elapsing the prescribed fault tolerant time interval (FTTI).
8, 9, 10	open	SysSafe-1	Due to the integrated pull-down resistors for EN pins, EN open-fault deactivates power rail regulation. The Traveo MCU becomes unpowered, and the system turns into SysSafe-1 state.
11	open	SysSafe-2	A watchdog input (WDI) open-fault results in asserting a reset to the Traveo MCU. The system turns into SysSafe-2 state.
12	open	SysSafe-2	A watchdog output (WDO) open-fault does not turn the system into any SysSafe state. The Traveo MCU should deliberately send a wrong clock pattern to the S6BP series PMIC to check if it can receive the WDO signal. In case of failure, the Traveo MCU can turn the system into SysSafe-2 state.

Table 4 Short-to-GND fault handling

Position	Fault mode	Results in	Description
1	Short-to-GND	SysSafe-1	In the case of a Battery-to-GND short-fault, the fuse must be blown off. Both the S6BP series PMIC and the Traveo MCU become unpowered, and the system turns into SysSafe-1 state.
2, 3, 4	Short-to-GND	SysSafe-1	An LX-to-GND short discharges the power rail. The Traveo MCU becomes unpowered, and the system turns into SysSafe-1 state. The S6BP series PMIC limits the current flow through the integrated high-side MOSFET in order not to flow overcurrent from the battery line to GND.
5, 6, 7	Short-to-GND	SysSafe-2	An FB-to-GND short-fault discharges the power rail. The Traveo MCU becomes unpowered, and the system turns into SysSafe-1 state. Power-Good signal is asserted as well.
11	Short-to-GND	SysSafe-2	A WDI-to-GND fault results in asserting a reset to the Traveo MCU. The system turns into SysSafe-2.
12	Short-to-GND	SysSafe-2	A WDO-to-GND fault results in keeping the reset to the Traveo MCU asserted. The system stays in SysSafe-2.
13, 14, 15	Short-to-GND	SysSafe-4	A PG-to-GND short fault results in asserting an interrupt signal to the Traveo MCU, bringing the system into SysSafe-4 state.

3.2.7 Intra-device faults

Cypress ran a deductive fault analysis (FTA) and an inductive fault analysis (FMEDA) on the design of S6BP series PMIC, and concluded that the probability of the serious failures, including systematic ones and random ones, are low enough to satisfy the ASIL-B metric defined in ISO 26262-5:2011 (SPFM $\geq$ 90%, LFM $\geq$ 60%, PMHF $\leq 10^{-7}$ h^{-1}.)

4 Summary

This application note describes the hardware aspects on integrating Cypress' S6BP series PMIC and Traveo MCU. For further information on the material in this application note, please contact a Cypress sales representative.

5 Related documents

- AN99497 – Designing a Power Management System with S6BP201A, S6BP202A, and S6BP203A
- AN98649 – How to Design a Power Management System with S6BP401A
- AN99435 – Designing a Power Management System with S6BP501A and S6BP502A

Revision history

Document version	Date of release	Description of changes
**	2017-08-16	New application note.
*A	2021-06-14	Updated to Infineon template. Completing Sunset Review.
*B	2022-06-23	Obsolete document. Completing Sunset Review.

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