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F²MC-16LX/16FX Family MB90XXX, MB96300 Super Series 16LX to 16FX Migration

This application note compares the 16LX Family MCUs and the 16FX Family MCUs.

Contents

1 Introduction

This application note compares the 16LX Family MCUs and the 16FX Family MCUs.

The 16LX Family consists of several different Series with different pin-counts and pin-outs, different peripheral types, and different port-pin function shares. The 16LX Family is manufactured using a 0.5µm technology. In contrast, the 16FX Family is a newly designed family that offers a new core based on a 0.18µm technology. Though different Series with different pin-counts will be available, the port-pin function shares are the same among all Series. The 16FX Family is instruction set compatible with the 16LX Family. For easy transition, there will be pin-compatible devices in the 16FX Family to the MB90340, MB90350, and MB90360 Series of the 16LX Family.

The emulation chip of the 16FX Family is the MB96V300.

In the 16LX Family, different emulation chips are required, depending on the Series.

2 Hardware

The 16LX Family MCUs are manufactured in 0.5µm or 0.35µm technology. The 16FX Family MCUs are manufactured in 0.18µm technology. This shrink in structure size implies that internal capacitances differ also between 16LX and 16FX families. This may have an impact on all inputs that rely on a certain capacitance. Examples are the ADC inputs, both channel inputs and analog supply input susceptibility to noise or tuning of a resonator on the clock pins X0, X1, X0A, X1A.

2.1 Mode Setting

The assignment of Mode Pin setting to the selected mode has changed. This simplifies optional hardware for mode change enabling serial programming. The assignment is shown in the following table.

Mode Pin Setting			16LX	16FX
MD2	MD1	MD0		
0	0	0	External Vector Mode 0[*1]	External Vector Mode 0[*1]
0	0	1	External Vector Mode 1[*1]	External Vector Mode 1[*1]
0	**1**	**0**	**Reserved**	**Serial Communication Mode**
0	1	1	Internal Vector mode	Internal Vector Mode
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	**1**	**0**	**Serial Communication Mode**	**External Vector Mode 2[*1]**
1	1	1	Parallel Flash Programming mode	Parallel Flash Programming mode

[*1]: Only available for devices with External Bus interface.

The 16FX Family MCUs, when used in single chip mode, do not necessarily need different Mode pin settings for programming and run mode. Please simply select the run mode (Internal Vector Mode) as shown in the table below. Furthermore, it is not necessary to select synchronous or asynchronous programming mode by setting port pins, as it is required for the 16LX Family.

2.2 Clock Distribution

The 16FX Family features a completely new clock unit. The most notable differences between the 16LX and 16FX clock unit are shown in the following table.

	16LX	16FX
Available clocks	Main Clock PLL PLL Clock Modulator Sub Clock[*1]	Main Clock PLL PLL Clock Modulator Sub Clock[*1] RC Clock (100 kHz and 2 MHz)
PLL multipliers	x1, x2, x3, x4, x6[*2]	x1, x2, x3, x4, x5, …, x25
System Clocks	1	2
Resources connected to System Clock 1	All	CPU core (CLKB), all peripherals except CAN and Sound Generator (CLKP1)
Resources connected to System Clock 2	n/a	CAN, Sound Generator (CLKP2)
Main Clock frequency	External oscillation frequency / 2	External oscillation frequency
Clock Prescaler	n/a	/1, /2, /3, …, /16 for CLKB, CLKP1, CLKP2 separately
Clock Setting Registers	CKSCR PSCCR	CKSR CKMR CKSSR CKFCR PLLCR

[*1]: Not available on devices with 'S' suffix.
[*2]: Not available on all devices.

For common clock configurations, the register settings are shown in the following sections.

2.2.1 Main Clock

In the 16LX Family, the Main Clock used the (external oscillation frequency / 2). The 16FX Family uses the full external oscillation frequency and offers prescalers for the different clock trees (CPU Clock, Peripheral Clocks). The required register settings to run all parts of the MCU with a frequency of half the external oscillation frequency are shown in the following table.

	16LX	16FX
CKSCR	0x3C	n/a
PSCCR	0x00	n/a
CKSR	n/a	0x35
CKSSR	n/a	0xFF
CKFCR	n/a	0x1111
PLLCR	n/a	0x0000
Clock Ready Monitor	CKSCR_SCM = 1	(CKMR & 0x2F) = 0x25
Main Clock Stabilization Time selections [Main oscillator cycles]	2^{10}, 2^{13}, 2^{15}, 2^{17}	2^{10}, 2^{12}, 2^{13}, 2^{14}, 2^{15}, 2^{16}, 2^{17}, 2^{18}

2.2.2 PLL Clock

In the 16LX Family, the CPU Clock is also the Peripheral Clock. This was changed for the 16FX Family so that the CPU Clock can run with a different frequency than the Peripheral Clocks. The following table shows the settings for a PLL factor of 6, which results in a 16LX CPU Clock of 24 MHz with a 4 MHz external oscillator. For compatibility reasons, the different clocks of the 16FX are configured to behave like in the 16LX Family, i.e. they run with the same frequency as the Core Clock.

PLL factor x6	16LX	16FX
CKSCR	0x3A	n/a
PSCCR	0x01	n/a
CKSR	n/a	0x7A
CKSSR	n/a	0xFF
CKFCR	n/a	0x0001
PLLCR	n/a	0x0025
Clock Ready Monitor	CKSCR_MCM = 0	(CKMR & 0x4F) = 0x4A
PLL Clock Stabilization Time selections [Main oscillator cycles]	2^{14}	2^{12}, 2^{14}

2.2.3 Sub Clock

The Sub Clock usually is a 32.768 kHz oscillator. Internally, this frequency is divided by 2 (selectable) in the 16LX Family. In the 16FX Family, the full Sub Clock frequency can be used. For compatibility reasons, the following table shows the same divider of 2 as used in the 16LX Family.

	16LX	16FX
CKSCR	0x30	n/a
PSCCR	0x04	n/a
CKSR	n/a	0x9F
CKSSR	n/a	0xFF
CKFCR	n/a	0x1111
PLLCR	n/a	0x0000
Clock Ready Monitor	n/a	(CKMR & 0x8F) = 0x8F

	16LX	16FX
Sub Clock Stabilization Time [Sub Clock oscillator cycles]	2^{14}	2^{12}, 2^{14}, 2^{15}, 2^{16}

2.3 C-Pin

The C-pin serves as voltage stabilization for the core voltage. This voltage drops when the current consumption of the MCU is increased significantly. This happens e.g. when returning from a stand-by mode to a run mode, especially when the MCU is run with a high clock frequency. Due to the low core voltage used in the 16FX Family, the voltage must be better stabilized than is necessary for the 16LX Family. The table below shows the values to always ensure reliable operation. For lower values for the 16FX Family, please refer to the datasheet.

	16LX	16FX
C-Pin capacitances	≥100 nF	4.7 µF ceramic, e.g. X7R

3 Peripherals

This chapter describes the differences of the on-chip peripherals.

If an input pin of a resource is used, the input mode of this pin must be enabled using the corresponding Port Input Enable Register PIER.

Note: The register settings of any used peripheral should be checked when porting software of either Family to the other Family.

Note: The register names of multiple instances of each peripheral are distinguished by a trailing instance number, e.g. the control register of Reload Timer 0 is named TMCSR0. If a peripheral exists more than 10 times in any device of the 16LX family, the count was hexadecimal. For the 16FX family, this has changed to a decimal count. In addition, if there are more than 10 instances of a peripheral, the trailing number has always 2 digits, e.g. for the IO Ports, the port data register of port 0 has changed its named from PDR0 (16LX) to PDR00 (16FX), PDRA (16LX) has changed to PDR10 (16FX).

Note: The names of the bits within a register might have changed in the documentation and hence, the header files. Because the bit names are always used in conjunction with the register name, the scheme has changed slightly. In the 16LX Family, the bits of the IO port registers also mentioned the port name, e.g. pin 2 of port 5 of the PDR was referenced as PDR5_P52. In the 16FX Family, this has changed to PDR5_P2, as it is already clear which port is referenced by the register name.

3.1 16-Bit Reload Timer

The 16-Bit Reload Timer of the 16FX Family features an additional prescaler with factor ½. This prescaler can be enabled by the TMCSR_FSEL register bit. Please note that the compatibility setting to the 16LX Family is

TMCSR_FSEL = 1

which disables the additional prescaler.

The 16FX Family Reload-Timer uses the Peripheral Clock 1. The 16LX Family Reload-Timer uses the Core Clock.

	16LX	16FX
Clock Source	Core Clock	Peripheral Clock 1
Internal Clock Prescaler	/2, /8, /32	/2, /4, /8, /16, /32, /64
External Trigger Prescaler	n/a	/1, /2
TMCSR Compatibility Setting	n/a	TMCSR_FSEL = 1, i.e. (TMCSR | 0x1000)
Event Input pin Enable	n/a	PIER register

3.2 16-Bit I/O Timer

The 16-Bit I/O Timer of the 16FX Family features an additional prescaler with factor ½. This prescaler can be enabled by the TCCS_FSEL register bit. Please note that the compatibility setting to the 16LX Family is

TCCS_FSEL = 1

which disables the additional prescaler.

The 16FX Family I/O Timer uses the Peripheral Clock 1. The 16LX Family I/O Timer uses the Core Clock.

	16LX	16FX
Clock Source	Core Clock	Peripheral Clock 1
Prescaler	/1, /2, /4, /8, /16, /32, /64, /128	/1, /2, /4, /8, /16, /32, /64, /128, /256
Compatibility Setting	n/a	TCCS_FSEL = 1, i.e. (TCCS | 0x4000)

3.3 Input Capture Unit (ICU)

The ICU of the 16LX and 16FX Families are nearly the same. Please note that the ICU is part of the 16-bit I/O Timer and the remarks there also apply. Furthermore, note that the input pin must be enabled by setting the corresponding bit in the PIER registers.

	MB90340	MB96340	MB90390	MB96380
Input enable	n/a	PIER register	n/a	PIER register
ICU channels at I/O Timer 0	0/1/2/3	0/1/2/3	0/1	0/1
ICU channels at I/O Timer 1	4/5/6/7	4/5/6/7	2/3/4/5	6/7

For the possible inputs of the ICUs, please refer to the following table.

	MB90340	MB96340	MB90390	MB96380
ICU0	IN0 UART0	IN0 UART0	IN0	IN0 UART0
ICU1	IN1 UART1	IN1 UART1	IN1 UART3	IN1 UART1
ICU2	IN2	IN2	IN2	n/a
ICU3	IN3	IN3	IN3	n/a
ICU4	IN4	IN4	IN4	n/a
ICU5	IN5	IN5	IN5 UART3	n/a
ICU6	IN6 UART2	IN6 UART2	n/a	IN6 UART2
ICU7	IN7 UART3	IN7 UART3	n/a	IN7

3.4 Output Compare Unit (OCU)

The Output Compare Unit (OCU) of 16LX and 16FX Family have the same behavior and same programming interface.

3.5 PPG

The PPG of the 16FX Family is a completely new peripheral that supersedes the PPG of the 16LX Family. The 16FX PPG can be configured to fulfill the same function as the 16FX PPG. The new PPG is the same as in the Cypress MB91460 Series MCUs. Please refer to the Hardware Manual for programming information of the new PPG.

The 16FX Family PPG uses the Peripheral Clock 1. The 16LX Family PPG uses the Core Clock.

	16LX	16FX
Clock Source	Core Clock	Peripheral Clock 1
External Trigger	n/a	1 per channel
External Trigger input pin enable	n/a	PIER register

3.6 I/O Ports

Several new registers have been introduced. For compatibility between 16LX and 16FX devices, please note the introduction of the Port Input Enable Register PIER. In the 16LX Family, it is sufficient to select the data direction as Input via the Data Direction Register DDR. **In the 16FX Family, it is required to also set the respective bit of the PIER register to enable the input.**

With the 16FX Family, it is possible to read the actual level at which a pin is held either by an internal or an external driver. For this, the External Pin State Register EPSR has been introduced.

The 16LX and 16FX Families offer different input level selections. The different available levels are shown in the following table.

	16LX	16FX
CMOS hysteresis 0307 High = 0.7 x VDD Low = 0.3 x VDD	P12, P44, 45, P46, P47, P50, P82, P83	All ports
Automotive hysteresis High = 0.8 x VDD Low = 0.5 x VDD	All Ports	All ports
TTL	Ports 0, 1, 2, 3 High = 2.0 V Low = 0.8 V	All ports High = 2.1 V Low = 0.8 V
CMOS hysteresis 0208 High = 0.8 x VDD Low = 0.2 x VDD	All ports except P12, P44, 45, P46, P47, P50, P82, P83	All ports

The default input level of the 16LX Family depends on the mode selected by the Mode pins. The default level of the 16FX Family is CMOS hysteresis 0307 level.

	16LX	16FX
Port Input Enable	n/a	PIER register
Direct read from port pin	Not available	EPSR register
Default Input Level: ▫ Internal Vector Fetch Mode ▫ External Vector Fetch Mode	▫ Flash Mode: CMOS ▫ Other: Automotive ▫ TTL	CMOS hysteresis 0307
Input Level Select Registers	ILSR0, ILSR1	PILR, EPILR
Input Level Selection for	Port	Pin

The following table shows the settings for the different levels. As an example, Port 0 is used.

	16LX	16FX
CMOS hysteresis 0307	ILSR = 0x0001	PILR00 = 0x00 EPILR00 = 0x00
Automotive hysteresis	ILSR = 0x0000	PILR00 = 0xFF EPILR00 = 0x00
TTL	ILSR = 0x1000	PILR00 = 0x00 EPILR00 = 0xFF

3.7 CAN

The 16LX Family featured the Cypress CAN (F/G/I-CAN, depending on the device). With the 16FX Family, the Bosch CAN (C_CAN) is introduced to the 16 Bit microcontrollers. The register set has changed completely. Please refer to the Hardware Manual for programming information of the C_CAN.

The 16FX Family C_CAN uses the Peripheral Clock 2. The 16LX Family CAN controller uses the Core Clock.

	16LX	16FX
Clock Source	Core Clock	Peripheral Clock 2
CAN Controller	F/G/I-CAN (Cypress IP)	C-CAN (Bosch IP)
CAN1 can be connected to pins of CAN0	On some devices (e.g. MB90390, MB90340)	No
CAN3 can be connected to pins of CAN2	On some devices (e.g. MB90390)	No

3.8 Interrupts

In the 16FX Family, each interrupt source has its own interrupt vector, while in the 16LX Family, several interrupt sources may share an interrupt vector. This results in a much higher number of interrupt vectors in the 16FX Family, e.g. the MB96340 Series has 88 interrupt vectors while the MB90340 Series has only 42. In both families, the interrupt vector table is located by default at the highest location in the Flash area (in the 16FX MCUs, it may be relocated using the TBR register). Due to this change, several other details of the interrupt controller have changed as well:

- Each interrupt vector consumes 4 Byte of (Flash-) ROM. The interrupt vector table of the MB96300 Super Series allows for up to 255 interrupts vectors. The emulation MCU MB96V300 usually contains vectors for all supported resources of planned devices. On final devices, vectors of non-existent resources have been removed (disabled on emulation system). Hence, only the actually available interrupts on a device have an interrupt vector available. To avoid having gaps in the interrupt vector table for non-existing interrupts, the interrupt vectors are joined together and numbered consecutively. **NOTE: The interrupt numbers of the same resource change from one Series to another within the 16FX Family! The interrupt numbers are different between 16LX and 16FX Families! Please refer to the datasheet for the correct interrupt numbers.**
- The interrupt controller of the 16FX family allows assigning one of 8 priorities to each interrupt vector, while the 16LX Family allowed assigning the priorities only to couples of interrupt vectors. The priorities are assigned using an ICR register. These registers are memory mapped in both Families. With the high number of available interrupt vectors in the 16FX Family, having an own register for each interrupt vector would cost too much IO space. Hence, there is only one 16-Bit wide ICR register, which consists of an index part to specify the desired interrupt vector and a configuration part to set the configuration.

	16LX	16FX
Shared interrupts	Yes	No
Number of Interrupt Control Registers (ICR)	16	1
Selection of ICR	Use the correct ICR	Write correct index into ICR
Interrupt Priorities	8	8
Minimum ISR start time	24 cycles (CLKB)	10 cycles (CLKB)
Minimum ISR return time	15 cycles (CLKB)	9 cycles (CLKB)
Interrupt Vector Table location	0xFFFF54 (for Dual-operation Flash devices, a different, fixed address may be selected)	TBR (default: 0xFFFC00)

3.9 EI2OS/uDMA/DMA

The 16LX Family offers the selection of 2 different data transfer peripherals: the EI2OS and the uDMA. For the 16FX Family, these have been combined to the new DMA. The programming model has only changed slightly.

	16LX		16FX
	EI2OS	uDMA	DMA
Descriptor	RAM located	Memory-mapped, outside RAM area, through window register DDWR	Memory-mapped, outside RAM area
Control Register in Descriptor	ISCS	DMACS	DMACS
Buffer pointer update	Increment only	Increment only	Increment or Decrement Compatibility Setting: Increment: DMACS_BPD = 0
Channel Selection	ICR_ICS	DCSR	DISEL
Enable	ICR_ISE	DER	DER

	16LX		16FX
	EI2OS	uDMA	DMA
Channels	16	16	Up to 16 (device dependent)
Interrupt Selection	ICR	DCSR	DISEL
Data transfer end indication	ICR_S	DSR_DTE	DSR_DTE
End cause	ICR_S	DSSR_STP	DSSR_STP
Concurrent use of interrupts and EI2OS/uDMA/DMA of shared ICR	No	Yes	Yes

3.10 LIN-USART

The LIN-USART of the 16FX Family is same as the one of the 16LX Family, with some extensions that can be enabled using the newly introduced register ESIR. This ESIR register defaults to the same mode as the 16LX Family used.

The 16FX Family LIN-USART uses the Peripheral Clock 1 as its clock source. The 16LX Family LIN-USART uses the Core Clock.

	16LX	16FX
Clock Source	Core Clock	Peripheral Clock 1

3.11 A/D Converter (ADC)

The 16FX Family features the same ADC as the 16LX Family, with few modifications. The default setting of the pin mode changed from ADC mode (16LX) to General Purpose I/O mode (16FX). Furthermore, the naming of the Analog Digital converter Enable Register (ADER) changed from referencing the port number (e.g. ADER5 for ADC pins on port 5) to numbering from the bottom up (ADER0 for ADC channels 0 – 7).

The 16FX Family ADC uses the Peripheral Clock 1 as its clock source. The 16LX Family ADC uses the Core Clock.

	16LX	16FX
Clock Source	Core Clock	Peripheral Clock 1
Default Analog Enable Setting	ON	OFF
ADER numbering	Port dependent	Bottom-up
Analog Input Enable Channel 0 – 7 Channel 8 – 15 Channel 16 – 23	 ADER6 = 0xFF ADER5 = 0xFF ADER7 = 0xFF	 ADER0 = 0xFF ADER1 = 0xFF ADER2 = 0xFF

3.12 External Interrupts

The function of the External Interrupts is the same in the 16LX and 16FX Families. Due to the different clock tree, a few specification differences were necessary. These are shown in the following table.

	16LX	16FX
Edge-triggered interrupt minimum pulse duration	5 clock cycles	200 ns

3.13 I2C Interface

The function of the I2C interface is the same in the 16LX and 16FX Families. In the 16LX Family, the I2C interface uses the Core Clock. In the 16FX Family, the I2C interface uses the Peripheral Clock 1.

	16LX	16FX
Clock Source	Core Clock	Peripheral Clock 1

3.14 ROM Mirror

The ROM Mirror in the 16LX Family mirrors a ROM area from bank 0xFF to bank 0x00. The area size depends on the Series and is either 32 KB or 48 KB. In the 16FX Family, the mirror size is always 32 KB and may be split in a ROM area and a RAM area. The ROM area can be selected from banks 0xF0 to 0xFF. The RAM area is always mirrored from bank 0x01. Also, the ROM area size is selectable as 8 KB, 16 KB, 24 KB, or 32 KB. The remaining size up to 32 KB is the mirrored from RAM in bank 0x01.

	16LX	16FX
Mirror size	32 KB or 48 KB, depending on Series	8 KB, 16 KB, 24 KB, or 32 KB, selectable
ROM Mirror source	Bank 0xFF	Selectable from bank 0xF0 to 0xFF
RAM Mirror source	n/a	Bank 0x01
Compatibility setting Mirror on	ROMM = 0x01	ROMM = 0xF7
Compatibility setting Mirror off	ROMM = 0x00	ROMM = 0x00

3.15 Sound Generator

The Sound Generator of the 16FX Family allows selecting between 256 and 384 counts of the PWM generator. This selection can be made by the SGCR_FSEL register bit. Please note that the compatibility setting to the 16LX Family is

SGCR_FSEL = 1

which selects 256 counts.

The 16FX Family Sound Generator uses the Peripheral Clock 2 as its clock source. The 16LX Family Sound Generator uses the Core Clock.

	16LX	16FX
Clock Source	Core Clock	Peripheral Clock 2
PWM counts	256	256 or 384
Compatibility Setting	n/a	SGCR_FSEL = 1, i.e. SGCR | 0x0400

3.16 Flash memory

3.16.1 Flash memory sectors

The Flash macros of the 16LX and 16FX Families differ. In the 16LX Family, the regular Flash sector layout is with different sector sizes of 8 KB, 16 KB, and 32 KB in the bank FF, and sector size of 64 KB in the other banks. Exceptions are the Dual-Operation Flash and the Compact Flash. The Flash is located downwards continuously starting at the highest memory location (with few exceptions). In the 16FX Family, the Flash sectors have only two different sizes: 8 KB and 64 KB. The 64 KB sized-sectors are located downwards continuously starting at the highest memory location. The 8 KB sectors are located upwards starting at address 0xDF0000. If a Satellite Flash (successor of the Dual-Operation Flash) is available, these sectors are of 8 KB size and are located upwards starting at address 0xDE0000.

	16LX	16FX
Sectors in bank FF (Regular Flash)	1x 16 KB 2x 8 KB 1x 32 KB	1x 64 KB
Sectors in bank FF (Dual-Operation Flash)	4x 4 KB 2x 16 KB 4x 4 KB	n/a
Sector in bank FF (Compact Flash)	1x 64 KB	n/a
Sectors in banks E0 – FE	1x 64 KB (if available)	1x 64 KB (if available)
Sectors in bank DF	n/a	4x 8 KB
Sectors in bank DE (Satellite Flash)	n/a	4x 8 KB

3.16.2 Sector erase

The sectors of a Flash macro may be erased individually by using a sector erase. The command sequence allows specifying one or more sectors to be erased. After specifying a sector, there is a period of 50 µs within which one can specify the next sector. After this wait period, the actual sector erase is started. The hardware sequence flag DQ3 informs whether the period has expired.

While the period has not expired, the 16LX Family MCUs show the other flags (e.g. DQ5, DQ7) as if the erase had already started.

While the period has not expired, the 16FX Family MCUs show the other flags should not be considered.

	16LX	16FX
Sector Erase wait period ongoing	All hardware sequence flags may be checked	Check DQ3

3.17 Delayed Interrupt

The Delayed Interrupt Module has the same behavior in the 16LX and 16FX Families. In the 16LX Family, the interrupt number is always the highest available number, e.g. interrupt number 42 in the MB90340 Series. In the 16FX Family, the Delayed Interrupt has the fixed interrupt number 12. In both cases, the Delayed Interrupt has lowest priority of concurrently requested interrupts with the same ICR setting.

	16LX	16FX
Interrupt Number	Highest available	12
Interrupt Priority	Lowest	Lowest

3.18 Reset behavior

The 16LX Family has 4 different reset causes, namely the External Reset, the Power-on Reset, the Software Reset, and the Watchdog Reset. These are discussed in the following sections.

3.18.1 External reset

The External Reset must be asserted for a minimum time, which depends on the operating state of the MCU. After release of the External Reset, the 16LX Family starts operation using the Main Clock, while the 16FX Family waits for 764 RC clock cycles and then starts using the RC clock with 2 MHz.

	16LX	16FX
Minimum assertion time in normal operation	500 ns	500 ns
Minimum assertion time in Stop mode, Sub Clock mode, Sub Sleep Mode, Watch mode	Oscillation startup time of oscillator + 100 µs	500 ns
Oscillation stabilization wait time	n/a	64 RC clock cycles
Reset extension time	n/a	700 RC clock cycles
CPU clock	Main Clock (external oscillation frequency / 2)	RC clock (nom. 2 MHz)
RAM content	Maintained	Maintained (except 0x007FFC – 0x007FFF)

3.18.2 Power Reset

The Power Reset is either a Power-On Reset or a Low Voltage Reset. The 16LX Family has to wait for the oscillation stabilization wait time of the Main Clock. The 16FX Family starts after 764 RC clock cycles using the RC clock with 2 MHz as the clock source.

	16LX	16FX
Oscillation stabilization wait time / Reset extension time	2^{16} Oscillation clock cycles	764 RC clock cycles
CPU clock	Main Clock (external oscillation frequency / 2)	RC clock (nom. 2 MHz)
RAM content	undefined	undefined

3.18.3 Software Reset

A Software Reset can be requested in both 16LX and 16FX Family. The register layout changed. Also, the CPU clock setting after reset is different.

	16LX	16FX
Reset request	LPMCR:RST = 0	RCR:SRSTG = 1
Oscillation stabilization wait time / Reset extension time	n/a	64 RC clock cycles
CPU clock	Main Clock (external oscillation frequency / 2)	RC clock (nom. 2 MHz)
RAM content	Maintained	Maintained (except 0x007FFC – 0x007FFF)

3.18.4 Watchdog Reset

The Watchdog Reset occurs when the watchdog is not triggered in time. The CPU clock after reset differs between 16LX and 16FX Family. Therefore, also the oscillation stabilization times differ.

	16LX	16FX
Oscillation stabilization wait time / Reset extension time	Depends on CKSCR setting	64 RC clock cycles
CPU clock	Main Clock (external oscillation frequency / 2)	RC clock (nom. 2 MHz)
RAM content	Maintained	Maintained (except 0x007FFC – 0x007FFF)

3.19 Low-power Modes

The 16LX and 16FX Families offer different standby modes. The following table gives an overview over the different modes.

		16LX	16FX
Run	Intermittent mode	CPU: reduced clock supply Peripherals: full clock supply	Divider of clocks CLKB, CLKP1, CLKP2
Standby Modes	Sleep Mode	CPU: no clock supply Peripherals: clock supply	CPU: no clock supply Peripherals: clock supply
	Timer Mode	CPU, Peripherals: no clock supply Timebase Timer, Watch Timer: clock supply	CPU, Peripherals: no clock supply PLL Timer, Main Timer, Sub Timer, RC Timer: clock supply, if corresponding clock is enabled
	Watch Mode	CPU, Peripherals: no clock supply Watch Timer: clock supply	
	Stop Mode	No clock supplied, all oscillators disabled	No clock supplied, all oscillators disabled

3.20 Clock Timers

The 16LX Family MCUs implement a Timebase Timer that uses the external oscillator for the Main Clock as its source clock. Devices that also feature a Sub Clock offer also a Watch Timer.

The 16FX Family offers different Source Clock Timers with similar functionality instead: the Main Clock Timer, the Sub Clock Timer, and the RC Clock Timer. The RC Clock Timer is a new resource due to the newly introduced RC Clock.

The following tables show the differences between the Timers of 16LX and 16FX Families.

Timebase/Main Clock Timer	16LX	16FX
Clock Source	External Main oscillator frequency	
Available Timer intervals	2^{11}, 2^{13}, 2^{15}, 2^{18}	2^{8}, 2^{9}, 2^{10}, 2^{11}, 2^{12}, 2^{13}, 2^{14}, 2^{15}, 2^{16}, 2^{17}, 2^{18}, 2^{19}, 2^{20}, 2^{21}, 2^{22}, 2^{23}
Counter clear causes	Power-on reset STOP mode Clock mode transition Timebase Timer Reset bit	Power reset RSTX falling edge Main oscillator disable Main Clock stop detection reset Main Clock Timer Reset bit

Watch/Sub Clock Timer	16LX	16FX
Clock Source	Sub Clock	External Sub Clock oscillator
Available Timer Intervals	2^{8}, 2^{9}, 2^{10}, 2^{11}, 2^{12}, 2^{13}, 2^{14}, 2^{15}	2^{10}, 2^{11}, 2^{12}, 2^{13}, 2^{14}, 2^{15}, 2^{16}, 2^{17}
Counter clear causes	Power-on reset Hardware Standby Stop mode Watch Timer clear bit	Power reset RSTX asserted Sub oscillator disable Sub clock stop detection reset Sub Clock Timer Reset bit

3.21 Watchdog

The Watchdog in the 16LX Family implements only 2 bit counter and uses the Timebase Timer or Watch Timer as prescalers. The 16FX Family implements a 24 bit counter and uses any of the available source clocks as input. Also, the watchdog timer clear behavior has changed.

	16LX	16FX
Counter width	2 bit	24 bit
Clock source	Timebase Timer, Watch Timer	RC Cock, Main Clock, Sub Clock
Activation	WDTC:WTE = 0	WDTCP = watchdog clear value
Timer clear	WDTC:WTE = 0	If activated by WDTCP = 0x00, clear with WDTCP = 0x00 If activated by writing any other value to WDTCP, clear by writing alternately the complementary data that was used to activate the watchdog.

3.22 External Bus Interface

Both Families offer a 24 bit address range for the External Bus. Due to differences in the memory map and added functionality in the 16FX Family, some points have to be considered when migrating from 16LX to 16FX.

	16LX	16FX
External Bus area start address	Device dependent	0x100000
External Bus area end address	ROM/Flash memory start address	0xDDFFFF (devices with Satellite Flash Memory) 0xDEFFFF (devices without Satellite Flash Memory)
Bus Clock prescaler	1	1, 2, 4, 8, 16, 32, 64, 128
Automatic Wait Cycles	0, 1, 2, 3 (separate for IO range, low, and high range)	0, 1, 2, 3, 4, 8, 16, 32 (separate for Chip Select areas 0 – 5)
Address Line Enable	A16 – A23	A00 – A23
Data Bus Width	8 bit, 16 bit (separate for IO range, low, and high range)	8 bit, 16 bit (separate for Chip Select areas 0 – 5)
Address Bus driven while no access is in progress	Yes (shows last address)	No, it is put in High-Z state It can be set to drive selectable data by setting the DDRxx registers to output and setting the desired value in the PDRxx registers

3.23 Real Time Clock (RTC)

The Real Time Clock (RTC) increments the time in steps of 1 second. The input clock for the RTC is fixed to the main oscillator for the 16LX Family. In the 16FX Family, all different source clocks (RC Clock, Main Clock, Sub Clock) can be selected as inputs.

	16LX	16FX
Clock Source	Main oscillator	RC Clock, Main Clock, Sub Clock

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	SWWI	10/25/2006	V1.0 MWi; 1st Release.
			03/05/2007	V1.1 PHu; changed 16FX PLL multipliers, requirements for C-pin; add link to MCU website.
			07/26/2007	V1.2 PHu; add general remarks about technology change; remarks about external bus interface
			07/30/2007	V1.3 PHu; update external interrupt input timing
			08/01/2007	V1.4 PHu; CAN1/3 cannot be relocated
			08/31/2007	V1.5 PHu; some clarifications
			08/31/2007	V1.6 PHu; RAM status after resets updated; address line status in between accesses clarified
			10/18/2007	V1.7 PHu; add information about DQ3 flag
*A	5860575	SWWI	08/23/2017	Migrated Spansion document from MCU-AN-300026-E-V17 to Cypress format.

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