Migration guide for Macronix OctaFlash family to Infineon SEMPER™ flash with HYPERBUS™ interface family

About this document

Scope and purpose

AN218664 provides guidelines for migration from the Macronix OctaFlash family to the Infineon SEMPER™ flash with HYPERBUS™ interface family. It describes the similarities and differences in the configuration of address spaces and transaction codes to facilitate the migration.

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1 Introduction

This application note provides guidelines for software migration from the Macronix 3.0-V MX25LM-G / MX66LM-G and 1.8-V MX25UM-G / MX66UM-G OctaFlash family to the Infineon 3.0-V S26HL-T and 1.8-V S26HS-T SEMPER™ flash.

The Infineon S26HS-T / S26HL-T SEMPER™ flash family is a high-speed CMOS, MIRRORBIT™ NOR flash devices that are compliant with the JEDEC eXtended SPI (JESD251 xSPI) specification. SEMPER™ flash is designed for functional safety in automotive systems with development according to the ISO 26262 standard to achieve ASIL-B compliance and ASIL-D readiness.

The Infineon SEMPER™ flash family and the Macronix OctaFlash family have similar hardware pin configurations but different software transaction sets. Infineon SEMPER™ flash adopts the transaction set of traditional parallel NOR (PNOR) flash memory devices such as the Infineon S29GL-S family. The HYPERBUS™ controller integrated in the host system translates software accesses to the HYPERBUS™ signal protocol. This makes the electrical signaling and the bus protocol differences between HYPERBUS™ and PNOR transparent to the software. As a result, you can use traditional PNOR software such as the Infineon low level driver for NOR flash, which supports the SEMPER™ flash with the HYPERBUS™ interface transaction set.

In addition to the HYPERBUS™ transaction set, SEMPER™ flash family supports a set of legacy SPI instructions, which allow legacy bootloaders to use the SPI single I/O interface to read out data from SEMPER™ flash, and then configure the controller to switch to the HYPERBUS™ signal protocol.

The SEMPER™ flash replaces the Macronix OctaFlash family with the software migration guidelines provided in this application note. This application note maps the software features such as address spaces, data protection, and transaction sets for accessing the flash memory array or registers. In terms of the hardware interface, Infineon SEMPER™ flash supports the following features whereas OctaFlash does not.

- **Hybrid burst:** This is a new type of Burst mode that combines one wrapped burst with a linear burst.
- **RSTO# output:** This output indicates when power-on-reset (POR) occurs within SEMPER™ flash.

2 Performance and features comparison

Table 1 Performance and feature comparison

Parameter		Infineon SEMPER™ HYPERBUS™	Macronix OctaFlash
Data retention		25-year[1]	20-year typical
Endurance (program/erase cycles)		1.280 M minimum[1] (256-KB sectors) 300k minimum (4-KB sectors)	100k minimum
Functional safety compliance		ASIL-B compliant, ASIL-D ready	No
Error correcting code		1-bit error correction, 2-bit error detection	1-bit error correction
Memory check-value calculation (CVC)		Yes	No
Interface cyclic redundancy check (CRC)		CRC32	CRC1
Endurance flex architecture		Yes	No
AutoBoot		Yes	Yes
SafeBoot (initialization) failure recovery		Yes	No
Configuration corruption detection		Yes	No
JEDEC SPI reset method		Yes	No
Blank check		Yes	No
Sector erase status indicator		Yes	No
Program/erase suspend/resume		Yes / Yes	Yes / Yes
Configurable output drive strength		Yes	Yes
Secure silicon region (OTP)		1 KB	1 KB
Burst wrap lengths		8, 16, 32, 64 bytes	16, 32, 64 bytes
Write Status Register time	Typ	44 ms	-
	Max	357.5 ms	40 ms
Page buffer size		256 byte / 512 bytes	256 bytes
Page program time	Typ	480 µs / 570 µs	150 µs
	Max	1700 µs / 1700 µs	750 µs
Sector erase time (4 KB)	Typ	42 ms	25 ms
	Max	335 ms	400 ms
Sector erase time (64 KB)	Typical	N/A	220 ms
	Max	N/A	2000 ms
Sector erase time (256 KB)	Typical	773 ms	N/A
	Max	2677 ms	N/A
Chip erase time (512 Mb)	Typical	201 s	150 s
	Max	696 s	300 s
Chip erase time (1 Gb)	Typical	398 s	150 s

1 See the datasheet for details on cycling and data retention specification.

Parameter			Infineon SEMPER™ HYPERBUS™	Macronix OctaFlash
		Max	1381 s	300 s
Temperature range			Industrial (-40°C to +85°C) Industrial Plus (-40°C to +105°C) AEC-Q100 grade 3 (-40°C to +85°C) AEC-Q100 grade 2 (-40°C to +105°C) AEC-Q100 grade 1 (-40°C to + 125 °C)	Industrial (-40°C to +85°C)
Packages	BGA 24 (5 ball × 5 ball) 6 × 8 mm (512 Mb) BGA 24 (5 ball × 5 ball) 8 × 8 mm (1 Gb)		Yes Yes	Yes
	16-pin SOIC 300 mil		No	Yes

3 Signal description

3.1 Data Strobe (DS)

The Infineon S26HS-T / S26HL-T SEMPER™ flash family and the Macronix OctaFlash family support the Data Strobe (DS or DQS) signal that toggles to synchronize the data output during the read operation in OPI mode. The Infineon S26HS-T / S26HL-T SEMPER™ flash family supports an optional single tristate-to-LOW cycle pre-drive on DS before read data output, while the Macronix OctaFlash family supports an optional single toggle pre-cycle on DS before read data output.

3.2 System Interrupt (INT#) and Error Corrected signal (ECS#)

The Infineon S26HS-T / S26HL-T SEMPER™ flash family and the Macronix OctaFlash family have an open-drain output signal on the same location in the BGA package (A5) that is connected to the interrupt pin in the host system. In the Infineon S26HS-T / S26HL-T SEMPER™ flash family, System Interrupt (INT#) can be used to notify the 1-bit and/or 2-bit ECC error detection and the busy-to-ready status transition. In the Macronix OctaFlash family, the Error Corrected signal (ECS#) is used for 1-bit and/or 2-bit ECC error detection only.

4 Electrical characteristics

4.1 DC characteristics

Table 2 and Table 3 show the DC characteristics comparison for the 512 Mb devices. See the S26HS-T_ datasheet for test conditions applicable to the parameters listed in the tables.

Table 2 DC characteristics (1.8 V parts)

Parameter		S26HS512T / S26HS01GT	MX25UM51245G MX66UM1G45G
Operating voltage range		1.7 V to 2.0 V	1.65 V to 2.0 V
Standby current @ 85°C	Typical	11 µA	20 µA 40 µA
	Max	113 µA / 160 uA	100 µA 300 µA
Deep power down current @ 85°C	Typical	1.3 µA	3 µA 6 µA
	Max	18 µA 24 µA	50 µA 80 µA
Octal DDR read current	Typical	156 mA @ 200 MHz	55 mA @ 200 MHz 110 mA @ 200 MHz
	Max	173 mA / 198 mA @ 200 MHz	80 mA @ 200 MHz 160 mA @ 200 MHz
Page program current	Typical	50 mA	30 mA
	Max	58 mA / 66 mA	40 mA
Write Status Register current	Typical	50 mA	20 mA
	Max	55 mA / 66 mA	40 mA 80 mA
Erase current	Typical	50 mA	30 mA
	Max	55 mA / 66 mA	40 mA

Table 3 DC characteristics (3 V parts)

Parameter		S26HL512T / S26HL01GT	MX25LM51245G MX66LM1G45G
Operating voltage range		2.7 V to 3.6 V	2.7 V to 3.6 V
Standby current @ 85°C	Typical	14 µA	35 µA 70 µA
	Max	126 µA / 160 µA	180 µA 350 µA
Deep power down current @ 85°C	Typical	2.2 µA	25 µA 50 µA
	Max	18 µA	80 µA

Parameter		S26HL512T / S26HL01GT	MX25LM51245G MX66LM1G45G
		26 µA	140 µA
Octal DDR read current	Typical	75 mA @ 166 MHz	40 mA @ 166 MHz 80 mA @ 133 MHz
	Max	130 mA @ 166 MHz	60 mA @ 166 MHz 120 mA @ 133 MHz
Page program current	Typical	50 mA	30 Ma
	Max	58 mA / 66 mA	40 mA
Write Status Register current	Typical	50 mA	20 mA
	Max	55 mA / 66 mA	40 mA
Erase current	Typical	50 mA	30 mA
	Max	55 mA / 66 mA	40 mA

4.2 AC Ccharacteristics

Table 4 and **Table 5** show the AC characteristics comparison for the 512-Mb devices. See the appropriate product **S26HL-T/HS-T datasheet** for test conditions applicable to the parameters listed in the tables.

Table 4 AC characteristics (1.8 V parts)

Parameter			S26HS512T S26HS01GT	MX25UM51245G MX66UM1G45G
Clock frequency for OPI mode		Max	200 MHz	200 MHz
CS# HIGH time	Read	Min	7.5 ns	10 ns
	Program / erase	Min	50 ns	40 ns
CS# active setup time		Min	4 ns	4.5 ns
CS# active hold time (relative to CK in Mode 0)		Min	4 ns	3 ns
Data in setup time		Min	0.5 ns	0.5 ns
Data in hold time		Min	0.5 ns	0.5 ns
Clock transition output valid (15-pF load)		Max	5.45 ns	5 ns 5.5 ns
Data strobe valid		Max	5.45 ns	5 ns 5.5 ns
Data strobe transition to data valid (15-pF load)		Max	0.4 ns	0.6 ns 0.65 ns
Data strobe transition to data invalid (15-pF load)		Max	0.4 ns	0.8 ns 0.85 ns

Table 5 AC characteristics (3 V parts)

Parameter			S26HL512T S26HL01GT	MX25LM51245G MX66UM1G45G
Clock frequency for OPI mode		Max	166 MHz	133 MHz
CS# HIGH time	Read	Min	7.5 ns	10 ns
	Program / erase	Min	50 ns	40 ns
CS# active setup time		Min	4 ns	4.5 ns
CS# active hold time (relative to CK in Mode 0)		Min	4 ns	3 ns
Data in setup time		Min	0.6 ns	0.8 ns
Data in hold time		Min	0.6 ns	0.8 ns
Clock transition output valid (15 pF load)		Max	7.25 ns	6 ns 7 ns
Data strobe valid		Max	7.25 ns	8 ns 7 ns
Data strobe transition to data valid (15 pF load)		Max	0.4 ns	0.8 ns
Data strobe transition to data invalid (15 pF load)		Max	0.4 ns	1 ns 0.8 ns

5 Address space maps

The SEMPER™ flash with HYPERBUS™ interface family has a set of address spaces as listed in **Table 6**.

Table 6 Address spaces

Address space	Description	OctaFlash equivalent
Flash memory array	The main non-volatile memory array used for data storage.	Flash memory array
Serial flash discoverable parameter (SFDP)	Factory-programmed memory array used for Infineon device characteristics information.	Serial flash discoverable parameter (SFDP)
Secure silicon region (SSR)	The 1024-byte one-time programmable (OTP) non-volatile memory area used for Infineon factory-programmed and customer-programmable permanent data.	Secured OTP
Persistent protection bit (PPB)	The non-volatile memory array with one bit for each sector. When programmed, each bit protects the related sector from erasure and programming.	Solid Protection bit (SPB)
PPB lock bit	The volatile register bit used to enable or disable programming and erasure of the PPB bits.	SPB Lock Down bit (SPBLKDN), but it is one-time programmable
Password	The OTP nonvolatile array used to store a 64-bit password, which enables changing the state of the PPB Lock bit when using Password mode sector Pprotection.	Password
Dynamic protection bit (DYB)	The volatile array with one bit for each sector. When set, each bit protects the related sector from erasure and programming.	Dynamic Protection bit (DPB)
Status or Peripheral Registers	The register used to hold the status of the Embedded Algorithm and read/write of other registers.	Status Registers and Configuration Registers

To access each address space, the SEMPER™ flash with HYPERBUS™ interface family provides a method called “Address Space Overlay” (ASO). ASO requires explicit address space switching by issuing ASO entryor exit transactions beforeor after accessing each address space except flash memory array and Status or Peripheral Registers address space. Each ASO replaces (overlays) either the sector selected by the transaction that enters the ASO or the entire flash device address range, depending on the ASO entry transaction.

5.1 Flash memory array

5.1.1 OctaFlash array

The Macronix OctaFlash family has a uniform architecture. The device consists of uniform 64-KB blocks that have sixteen 4-KB sectors each. In OctaFlash, a sector is 4 KB in size and a block is64 KB. The SEMPER™ flash family has no block concept but only has sectors, 256 KB in size, or 4 KB in parameter sectors. **Table 7** shows a comparison of sector address maps for 512 Mb devices.

5.1.2 HYPERBUS™ array

The SEMPER™ flash default configuration is a uniform sector architecture with a sector size of 256 KB. A user configuration option is available to overlay the bottom sector or top sector with thirty-two 4-KB parameter sectors or sixteen parameter sectors to the bottom and top sectors. The existence and location of the parameter sectors is changed by writing to Non-volatile Configuration Registers (CFR1N[9:8], CFR2N[2]).

- Thirty-two 4-KB sectors grouped to the bottom, while the remaining sectors are 256 KB (default)
- Thirty-two 4-KB sectors grouped to the top, while the remaining sectors are 256 KB
- Thirty-two 4-KB sectors equally split between top and bottom, while the remaining sectors are 256 KB
- Uniform 256-KB sectors

Table 7 shows all sector combinations thata HYPERBUS™ device may have and a comparison of OctaFlash sector address maps for 512 Mb devices.

Table 7 Sector address map comparison

Address range	InfineonSEMPER™				Macronix OctaFlash	
	CFR1N[9:8] = 00 CFR2N[2] = 0	CFR1N[9:8] = 01 CFR2N[2] = 0	CFR2N[2] = 1	CFR1N[9] = 1	Sector	Block
0000000h – 0000FFFh	0 (4 KB)	0 (256 KB)	0 (4 KB)	0 (256 KB)	0 (4 KB)	0 (64 KB)
0001000h – 0001FFFh	1 (4 KB)		1 (4 KB)		1	
0002000h – 0002FFFh	2 (4 KB)		2 (4 KB)		2	
0003000h – 0003FFFh	3 (4 KB)		3 (4 KB)		3	
0004000h – 0004FFFh	4 (4 KB)		4 (4 KB)		4	
0005000h – 0005FFFh	5 (4 KB)		5 (4 KB)		5	
0006000h – 0006FFFh	6 (4 KB)		6 (4 KB)		6	
0007000h – 0007FFFh	7 (4 KB)		7 (4 KB)		7	
…	…		…		…	
000F000h – 000FFFFh	15 (4 KB)		15 (4 KB)		15	

Address range	InfineonSEMPER™				Macronix OctaFlash	
	CFR1N[9:8] = 00 CFR2N[2] = 0	CFR1N[9:8] = 01 CFR2N[2] = 0	CFR2N[2] = 1	CFR1N[9] = 1	Sector	Block
0010000h – 0010FFFh	16 (4 KB)		16 (192 KB)		16	1
…	…				…	
001F000h – 001FFFFh	31 (4 KB)				31	
0020000h – 0020FFFh	32 (128 KB)				32	2
…					…	
002F000h – 002FFFFh					47	
0030000h – 0030FFFh					48	3
…					…	
003F000h – 003FFFFh					63	
0040000h – 0040FFFh	33 (256 KB)	1 (256 KB)	17 (256 KB)	1 (256 KB)	64	4
…					…	
004F000h – 004FFFFh					79	
0050000h – 0050FFFh					80	5
…					…	
005F000h – 005FFFFh					95	
0060000h – 0060FFFh					96	6
…					…	
006F000h – 006FFFFh					111	
0070000h – 0070FFFh					112	7
…					…	
007F000h – 007FFFFh					127	
…	…	…	…	…	…	…
3F80000h – 3F80FFFh	286 (256 KB)	254 (256 KB)	270 (256 KB)	254 (256 KB)	16256	1016
…					…	

Address space maps

Address range	InfineonSEMPER™				Macronix OctaFlash	
	CFR1N[9:8] = 00 CFR2N[2] = 0	CFR1N[9:8] = 01 CFR2N[2] = 0	CFR2N[2] = 1	CFR1N[9] = 1	Sector	Block
3F8F000h – 3F8FFFFh					16271	
3F90000h – 3F90FFFh					16272	1017
…					…	
3F9F000h – 3F9FFFFh					16287	
3FA0000h – 3FA0FFFh					16288	1018
…					…	
3FAF000h – 3FAFFFFh					16303	
3FB0000h – 3FB0FFFh					16304	1019
…					…	
3FBF000h – 3FBFFFFh					16319	
3FC0000h – 3FC0FFFh	287 (256 KB)	255 (128 KB)	271 (192 KB)	255 (256 KB)	16320	1020
…					…	
3FCF000h – 3FCFFFFh					16335	
3FD0000h – 3FD0FFFh					16336	1021
…					…	
3FDF000h – 3FDFFFFh					16351	
3FE0000h – 3FE0FFFh		256 (4 KB)			16352	1022
…		…			…	
3FEF000h – 3FEFFFFh		271 (4 KB)			16367	
3FF0000h – 3FF0FFFh		272 (4 KB)	272 (4KB)		16368	1023
…		…	…		…	
3FF8000h – 3FF8FFFh		280 (4 KB)	280 (4 KB)		16376	
3FF9000h – 3FF9FFFh		281 (4 KB)	281 (4 KB)		16377	
3FFA000h – 3FFAFFFh		282 (4 KB)	282 (4 KB)		16378	

Address range	InfineonSEMPER™				Macronix OctaFlash	
	CFR1N[9:8] = 00 CFR2N[2] = 0	CFR1N[9:8] = 01 CFR2N[2] = 0	CFR2N[2] = 1	CFR1N[9] = 1	Sector	Block
3FFB000h – 3FFBFFFh		283 (4 KB)	283 (4 KB)		16379	
3FFC000h – 3FFCFFFh		284 (4 KB)	284 (4 KB)		16380	
3FFD000h – 3FFDFFFh		285 (4 KB)	285 (4 KB)		16381	
3FFE000h – 3FFEFFFh		286 (4 KB)	286 (4 KB)		16382	
3FFF000h – 3FFFFFFh		287 (4 KB)	287 (4 KB)		16383	

The same principle applies to 1-GB devicesThe only difference is the total number of uniform sectors.

5.2 Device identification (ID) and serial flash discoverable parameters (SFDP)

The SEMPER™ flash with has two methods to identify the type of flash memory: Device identification (ID) and SFDP.

The device identification (ID), traditionally referred to as Autoselect in parallel NOR, contains the JEDEC manufacturer ID, device ID, and some configuration and protection status information from the flash memory. The host system uses the ID to select the appropriate driver software for the specific flash device.

The ID transaction and transaction codes are different (see the transactions in **Table 8**), but they are combined into a single address space and appear in a single overlay. Accessing the ID will display the combined ID address map. The ID address map appears within and overlays the flash memory array data of the sector selected by the address used in the ID transaction. While the ID ASO is entered, the content of all other sectors is undefined.

The OctaFlash family has an SFDP, a set of parameter tables that contain device characteristics that are used for identification. The SFDP can be adjusted by the system software to accommodate multiple memory devices.

The SEMPER™ flash also supports the read SFDP transaction in legacy SPI mode, which is used by the bootloader to automatically detect the device information.

Table 8 lists the ID address map for the SEMPER™ flash family. For details of the ID and SFDP field definitions, see the datasheet.

Table 8 Device ID

Byte	S26HS512T / S26HL512T S26HS01GT / S26HL01GT	MX25UM512G / MX25LM512G MX66UM1G45G / MX66LM1G45G
1	34h	C2h
2	7Bh / 6Ah	80h / 85h
3	1Ah 1Bh	3Ah 3Bh

6 Data protection

6.1 Secure Silicon Region (SSR)

The Infineon SEMPER™ flash family and the Macronix OctaFlash family have 1024-byte OTP address space, referred to as the “Secure Silicon Region (SSR)” by SEMPER™ flash and the “secured OTP” by Macronix OctaFlash. This memory space is used to provide an additional system security by holding a unique device serial number that is set by the factory or system user. The SEMPER™ flash SSR provides a larger user-programmable address space than the OctaFlash Secured OTP as well as individually lockable regions.

6.1.1 OctaFlash Secured OTP

The OctaFlash secured OTP region’s lowest 512 address bytes are available for programming; the highest 512 address bytes are Macronix factory-programmed. The OTP region is programmed or read by first entering the Secured OTP mode with the enter security OTP transaction. Normal procedures are used for programming or reading, and then the Secured OTP mode is exited with the exit security OTP transaction (see **Table 11** and **Table 12** for the list of transactions). The user-programmable secured OTP address space is locked by writing the WRSCUR (Write Security Register) transaction to set the user lock-down bit1 as '1'. The factory-programmable secured OTP address space is locked in the factory in the Security Register bit0. After the OTP is locked by the factory or a user, the corresponding address range cannot be reprogrammed.

Table 9 OctaFlash Secured OTP address map

Address range	Contents
xxx000 - xxx1FF	Available for user programming
xxx200 - xxx3FF	Programmed by Macronix

6.1.2 SEMPER™ flash Secure Silicon Region (SSR)

The SEMPER™ flash 1024-byte SSR is divided into 32 individually lockable, 32-byte aligned and length regions. The lowest 16 address bytes are Infineon factory-programmed. The next four higher bytes are the SSR Lock bytes, where each bit in an SSR Lock byte corresponds to an SSR region. You can program the SSR Lock bytes to lock the corresponding SSR regions individually to prevent further programming (see the datasheet for more details).

The next higher 12 bytes of the lowest address region are Reserved for Future Use (RFU). These bits can be programmed, but future Infineon devices uses SSR Lock bits to protect a larger SSR space. The remaining regions are available for the user to program additional permanent data. The SSR region is programmed or read by entering the SSR ASO with the SSR entry transaction, programming or reading through the normal procedures, and then exiting with the SSR exit transaction (see **Table 11** and **Table 12**). The SSR TLSSRP (CFR1N[10]) Configuration Register bit is set to '0' to protect the entire SSR memory by preventing further programming. The SSR transaction provides the same functionality as the OctaFlash WRSCUR transaction.

Table 10 SEMPER™ flash Secured Silicon Region (SSR) address map

Region	Byte address range (Hex)	Contents	Initial delivery state
Region 0	0	LSB of Infineon-programmed random number.	Infineon-programmed random number
	…	…	
	000F	MSB of Infineon-programmed random number.	
	0010-0013	Region locking bits. Byte 10 [bit 0] locks region 0 from programming when = 0. … Byte 13 [bit 7] locks region 31 from programming when = 0.	All bytes = FF
	0014 - 001F	Reserved for Future Use (RFU).	All bytes = FF
Region 1	0020 - 003F	Available for user programming.	All bytes = FF
Region 2	0040 - 005F	Available for user programming.	All bytes = FF
…	…	Available for user programming.	All bytes = FF
Region 31	03E0 - 003FF	Available for user programming.	All bytes = FF

6.2 Block lock protection

The OctaFlash supports the block lock protection feature that allows you to protect memory areas by writing BP0-BP3 bits in the Status Register. The SEMPER™ flash family does not support block lock protection; instead use the advanced sector protection features.

6.3 Advanced sector protection (ASP)

While OctaFlash supports the block lock protection feature that allows you to protect memory areas by writing BP0-BP3 bits in the Status Register, the SEMPER™ flash family supports the advanced sector protection (ASP) feature. This feature allows sectors to be individually protected by the corresponding volatile protection bits (DYB bits) or nonvolatile protection bits (PPB bits). The SEMPER™ flash DYB and PPB bits are assigned to each sector throughout the memory; when either a DYB or PPB bit is ‘0’, the corresponding sector is protected from program and erase operations.

The OctaFlash family supports a similar protection feature that is compatible with ASP (DPB as volatile protection bits and SPB as non-volatile protection bits). The OctaFlash family DPB bits are also assigned to each sector, but the SPB bits are assigned to each sector in the bottom and top 64 KB of the memory and to each 64-KB block in the remaining memory. The sector or block is protected when either of the DPB or SPB bits is ‘1’. The OctaFlash family also supports the Gang lock/unlock feature that can protect/unprotect the entire flash memory array.

The SEMPER™ flash has a PPB temporary protection selection bit (PPLV[0]) to protect the PPB bits, which provides the same functionality as the OctaFlash SPB Lock Down bit (SPBLKDN). The OctaFlash SPBLKDN bit is in the OTP Lock Register; when it is locked as ‘0’, all SPB bits are permanently locked from program and erase operations. Since PPLV[0] bit is not in an OTP region, it has greater flexibility and added features. The PPLV[0] bit is managed by persistent protection or password protection:

- **Persistent protection** sets the PPLV[0] bit to '1' during POR or a hardware reset to unprotect the PPB bits. A transaction can clear the PPLV[0] bit to '0' to protect the PPB bits. If there is no persistent protection transaction to set the PPLV[0] bit back to '1', it will remain '0' until the next Power-OFF or a hardware reset.
- **Password protection** clears the PPLV[0] bit to '0' during POR or a hardware reset, locking the PPB bits. A 64-bit password is permanently programmed and hidden. This transaction is used to provide a password for comparison with the hidden password. If the passwords match, the PPLV[0] bit is set to '1' to unprotect the PPB bitsand thetransaction is used to clear the PPB Lock bit to '0'.

The selection of persistent protection or password protection is made in the Advanced Sector Protection Register (ASPO) and is, therefore, a permanent selection. The features and register set of the S26HL-T ASPO[3:0] register can be read by the sector address (SA) protection status read transaction. The data returned from the SA protection status read transaction indicates whether the target sector is protected in bits '0' to '3'.

- **Bit 0:** Indicates whether the sector is protected (0 = protected, 1 = unprotected)
- **Bit 1:** Protected using the sector's DYB bit (0 = protected, 1 = unprotected)
- **Bit 2:** Protected using the sector's PPB bit (0 = protected, 1 = unprotected)

7 Read flash memory array

The flash memory array is the primary and default address space that is selected during Power ON, after a hardware reset, or after a transaction reset. The typical HYPERBUS™ controller integrated in the host system, maps the SEMPER™ flash memory array within the system memory area. Reading from the address where the SEMPER™ flash is mapped returns the data from the SEMPER™ flash. In general, the software does not need to consider the HYPERBUS™ signal protocol, but the HYPERBUS™ controller must be set to either a wrapped or linear burst type for every read transaction. The length of a wrapped burst can be configured via CFR1N[1:0] or CFR1V[1:0]. **AN99195** describes burst configuration and read performance optimization.

The OctaFlash family has read transactions based on the bus width and Addressing mode. It also has a set burst length transaction that allows configuring both burst type and length. See **Table 11** and **Table 12** for the transaction comparison.

The SEMPER™ flash family supports single I/O reads in the legacy SPI boot Interface mode. It allows the bootloader to use legacy SPI transactions to access the boot code, and write to the Configuration Register to switch to SEMPER™ Flash Interface mode after the boot process. As a result, if the bootloader uses a single I/O SPI read transaction to boot up the system, there is no need to modify the bootloader code for the migration from OctaFlash family to the SEMPER™ flash family.

8 Program flash memory array

The SEMPER™ flash HYPERBUS™ family supports two methods of programming: word or write buffer programming. Write buffer programming allows a buffer size of up to 512 bytes to be programmed in an operation. Word programming is used to program a single word to the flash memory array. Write buffer programming is recommended because it is more efficient and faster than word programming.

The OctaFlash family is programmed on a 256-B-page basis with the page program operation, similar to the SEMPER™ flash HYPERBUS™ write buffer programming.

Code Listing 1 shows an example C code for initiating write buffer programming for the SEMPER™ flash (if necessary, a volatile keyword is added). See **Table 11** and **Table 12** for the transaction comparison.

Code Listing 1 Write buffer programming example for the SEMPER™ flash

```
UINT16 *src = source_of_data;               /* address of source data */
UINT16 *dst = first_destination_addr;       /* flash destination address */
UINT16 wc = words_to_program -1;            /* word count (minus 1) */
*( (UINT16 *)base_addr + 0x555 ) = 0x00AA; /* write unlock cycle 1 */
*( (UINT16 *)base_addr + 0x2AA ) = 0x0055; /* write unlock cycle 2 */
*( (UINT16 *)sector_address ) = 0x0025;     /* write buffer load command */
*( (UINT16 *)sector_address ) = wc;         /* write word count (minus 1) */
for (i=0;i<=wc;i++)
{
*dst++ = *src++;
}
*( (UINT16 *)sector_address ) = 0x0029;     /* write confirm command */
```

9 Erase flash memory array

The SEMPER™ flash family supports sector erase on 256-KB sectors and chip erase, while the OctaFlash family memory supports sector erase on 4-KB sectors, block erase on 64-KB blocks, and chip erase. SEMPER™ flash does not have a dedicated transaction for erasing 4-KB parameter sectors; the sector erase transaction sequence can be used to target the appropriate parameter sector addresses.

Code Listing 2 shows an example C code for initiating SEMPER™ flash sector erase (if necessary a volatile keyword is added). See **Table 11** and **Table 12** for transaction comparison.

Code Listing 2 Sector erase example

```
*( (UINT16 *)base_addr + 0x555 ) = 0x00AA; /* write unlock cycle 1 */
*( (UINT16 *)base_addr + 0x2AA ) = 0x0055; /* write unlock cycle 2 */
*( (UINT16 *)base_addr + 0x555 ) = 0x0080; /* write setup command */
*( (UINT16 *)base_addr + 0x555 ) = 0x00AA; /* write additional unlock cycle
1 */
*( (UINT16 *)base_addr + 0x2AA ) = 0x0055; /* write additional unlock cycle
2 */
*( (UINT16 *)sector_address ) = 0x0030;    /* write sector erase command */
```

9.1 Blank check

The SEMPER™ flash family supports the blank check transaction that is used to confirm whether the selected flash memory array sector is fully erased. No similar transaction is supported in the OctaFlash family. The blank check transaction replaces the traditional procedure of reading each flash memory array bit in a sector to verify that they are all 1s. Using the blank check transaction before issuing a sector erase transaction saves time, if most of the sectors to be erased are blank. This is likely the case during the programming phase of the product manufacture process. See **Table 11** and **Table 12** for transaction comparison.

9.2 Erase status evaluation

The SEMPER™ flash family supports the erase status evaluation transaction that can be used to detect erase operations that failed due to loss of power, reset, or a failure during an erase operation. No similar transaction is supported in the MX25LM/MX25LM OctaFlash family. See **Table 11** and **Table 12** for transaction comparison.

10 Status Register

The SEMPER™ flash family has a single, read-only 16-bit Status Register (STRV), while the OctaFlash family has a Status Register and a Security Register. See sections 5.0 through 5.2.11 as well as 5.3 through 5.3.6 within the SEMPER™ **S26HL-T/HS-T datasheet** for all register bit assignments and detailed descriptions of the bits. The SEMPER™ flash Status Register and the OctaFlash Security Registers both contain bits dedicated to program suspend, program status, erase suspend, and erase status.

The SEMPER™ flash Status Register has the following additional dedicated bits:

Dedicated bit	Function	OctaFlash equivalent
Sector erase success/failure status flag (STRV[0])	Indicates whether the most recent sector erase transaction was successful.	Not supported
Sector protection (lock) error flag (STRV[1])	Indicates whether a sector is locked by the lock bits in the advanced sector protection region.	Not supported
Write buffer abort status flag (STRV[3])	Indicates an error in the write buffer program transaction sequence.	Not supported
Device ready/busy status flag (STRV[7])	Indicates whether the device is busy with an embedded algorithm.	Write in Progress bit in the Status Register

The OctaFlash Security Register and Status Register have the following additional dedicated bits:

Dedicated bit	Function	SEMPER™ flash equivalent
Write protection selection	Indicates whether the device is under Block Lock mode or an Advanced Sector Protection mode.	Not supported; uses the Advanced Sector Protection mode instead.
OTP indicator	Indicates whether the factory-programmed ID address space in the OTP region is programmed.	Uses a random, factory-programmed ID number programmed into the lowest 16 address bytes.
Lock-down secured OTP	Locks the entire secured OTP region if the bit is programmed.	Not supported; use the SSR Freeze bit located in the Configuration Register instead.
Write in Progress bit	Indicates whether the device is busy with a write transaction.	Not supported; uses the Device Ready bit instead.
Write Enable Latch bit	Must be set before any instruction which changes the device content.	Not required.
Block Protect bits	For Block Protection mode	Not supported; use the Advanced Sector Protection mode instead.

See **Table 11** and **Table 12** for transaction comparison.

11 Deep power down

The SEMPER™ flash family supports deep power - down (DPD). In DPD mode, current consumption is driven to the lowest level. DPD is entered using the enter deep power-down transaction. Exiting DPD mode is accomplished with the assertion of CS# during any read or write operation or a hardware reset. There is no dedicated transaction to exit DPD.

The OctaFlash family also supports deep power down (DP) and a transaction for entering DP. Exiting the DP is accomplished by issuing a release from deep power down (RDP), read electronic signature (RES), or software reset transaction. See **Table 11** and **Table 12** for transaction comparison.

12 SEMPER™ flash new features

12.1 Endurance flex architecture (wear-leveling)

Endurance flex architecture allows partitioning of the main memory array into regions, which are configured to either high-endurance or long-retention. The endurance flex architecture implements wear-leveling in high-endurance regions where programor erase cycles are spread evenly across all the sectors that are part of the wear-leveling pool. This greatly improves the reliability of the device by avoiding premature wear-out of an individual sector.

Architecturally, the endurance flex architecture's wear-leveling algorithm is based on a mapping of logical sectors to physical sectors. During the lifetime of the part, this mapping is changed to maintain a uniform distribution of programor erase cycles over all physical sectors. The logical to physical mapping information is stored in a dedicated flash array, which is updated when sectors are swapped. Sector swaps occur when an erase transaction is given.

The endurance flex architecture’s high-endurance region requires a minimum set of 20 sectors. To attain flexibility between configuring long-retention and/or high-endurance regions, a four-pointer architecture is provided. The factory default setting designates all sectors as high-endurance, a part of the wear-leveling pool with all pointers disabled. The four pointers are used to form a maximum of five regions, where each is configured as either long-retention or high-endurance. The pointers are one-time programmable and must be configured during the initial device setup.

Data is updated frequently and stored in high-endurance partitions to enable the highest number of program/erase cycles and longest device lifespan. Boot code is infrequently updated and is stored in long-retention partitions to enable high-reliable 25-year retention.

Note that the 4-KB sectors are not part of the endurance flex architecture. Only the main array 256-KB sectors are included.

See the **S26HL-T/HS-T datasheet** and the endurance flex architecture application note for more information.

12.2 Data integrity check

The data integrity check (DIC) transaction sequence causes the device to perform a cyclic redundancy check (CRC) calculation over a user-defined address range. The DIC process calculates the check-value on the data contained at the starting address through the ending address.

See the **S26HL-T/HS-T datasheet** for more information.

12.3 Interface cyclic redundancy check

Interface cyclic redundancy check transactions are provided to perform a hardware accelerated CRC calculation over the interface.

See the **S26HL-T/HS-T datasheet** for more information.

12.4 Sector erase count

The SEMPER™ flash with HYPERBUS™ interface family has a new transaction that allows the software to check the sector erase count. The command outputs the number of erase cycles for the sector of the given address. Each sector's erase cycle count information is stored in counters in a dedicated flash array, which record the number of erase cycles performed on that sector. The sector erase count sequence outputs the number of erase cycles for the sector of the given address.

See the **S26HL-T/HS-T datasheet** for more information.

12.5 ECC error address trap

A register is provided to capture the data unit address where an ECC error is first encountered during a read of the flash array. The Error Lower Address Register and Error Upper Address Register contain the address that was accessed when the error was detected. The failing bits may not be located at the exact address indicated in the registers but will be located within the aligned 16-byte data unit where the error was detected. If the errors are found in multiple data units during a single read operation, the address of the first failing data unit address is captured in the Error Lower and Upper Address registers.

See the datasheet for more information.

12.6 Error detection counter

A counter is provided to keep track of the number of 1-bit or 2-bit errors that occur as data units, are read from the flash array. The errors recognized in the main array will cause the error detection counter to increment. The counter is set to '0' on POR, a hardware reset, or with the ECC Clear command.

See the **S26HL-T/HS-T datasheet** for more information.

12.7 SafeBoot

Power ON initialization failure or corrupt registers render the device unusable. If it is not a catastrophic failure, such as the firmware getting permanently corrupted, it is potentially possible to recover the device. The SafeBoot feature uses Status Register polling sequence to detect Power-ON failure or Register Corruption has occurred.

See the **S26HL-T/HS-T datasheet** for more information on the SafeBoot process.

12.7.1 Power-On detection

During the device initialization process a failure mayoccur and make the device unusable. A hardware reset initiated by the master controller (host) can potentially recover the device. SEMPER™ flash family devices provide a failure signature (0x61) in its Status Register upon detecting an initialization breakdown. The host must go through the Status Register polling process to determine if a hardware reset is needed to re-initialize the device.

See the **S26HL-T/HS-T datasheet** for more information.

12.7.2 Configuration corruption detection

A WRR or WRAR command sequence to nonvolatile configuration registers may get interrupted by a brown out or a hardware reset; this will corrupt the configuration data. The S26HL-T family device detects a corrupted configuration and enters a default mode where the device is accessed, by providing a configuration corruption signature in its Status Register. The host detects this to initiate reprogramming of the nonvolatile configuration registers' data.

See the **S26HL-T/HS-T datasheet** for more information.

13 Transaction summary

The SEMPER™ flash is operated in the HYPERBUS™ interface or serial peripheral interface (SPI). The OctaFlash family can be operated in Octal Peripheral Interface (OPI) mode or Serial Peripheral Interface (SPI) mode. The transaction comparison for these interfaces are shown in the following sections.

13.1 SEMPER™ flash with HYPERBUS™ Interface vs OctaFlash OPI Interface transaction

Table 11 summarizes the supported Octal transactions for each device. Pertinent differences will be discussed in subsequent sections. The SEMPER™ flash family has a new definition of transaction names for easier recognition of the transaction operation.

13.1.1 SEMPER™ flash and OctaFlash OPI transaction comparison

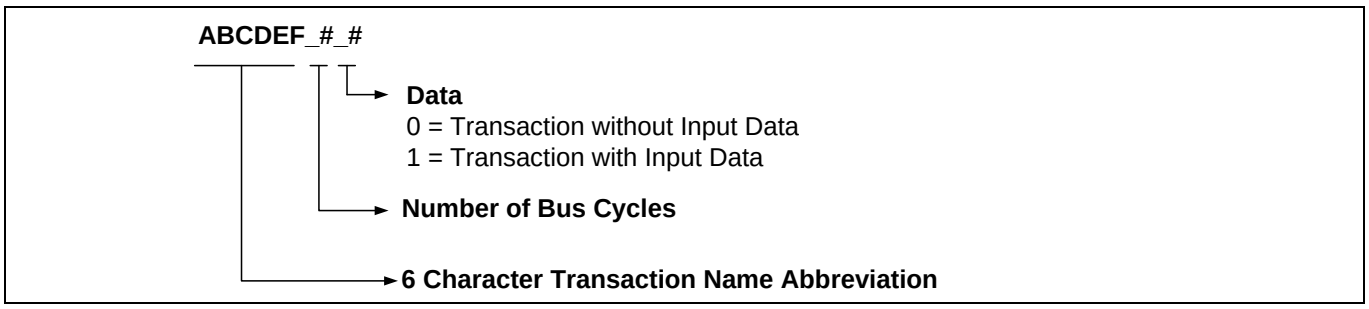

Figure 1 SEMPER™ flash transaction name decoder

Table 11 SEMPER™ flash and OctaFlash OPI transaction comparison

Function	Transaction name		Description	Supported	
	SEMPER™ flash	Macronix OctaFlash		SEMPER™ flash	Macronix OctaFlash
Identification	IDSFE1_3_1 IDSFE2_1_1	N/A	Identification ASO entry	Yes	No
	RDIDSF_1_1	RDID	Read Identification Register	Yes	Yes
		RDSFDP	Read Serial flash discovery parameters	Yes	Yes
		N/A	Read Unique Identification Register	Yes	No
	ASOEXT_1_1	N/A	Identification ASO exit	Yes	No
Register Access	PGVCR*_4_0 PGNCR*_4_0 ERNC12_3_0	WRSR WRCF WRCR2	Program / Erase / Write Registers (Status and Configuration Registers)	Yes	Yes
	N/A	WREN WRDI	Write enable / write disable	Note[2]	Yes

2 HYPERBUS™ uses two enable bus cycles, AAh and 55h, to protect from inadvertent program and erase transactions.

Transaction summary

Function	Transaction name		Description	Supported	
	SEMPER™ flash	Macronix OctaFlash		SEMPER™ flash	Macronix OctaFlash
	RDVCR*_4_0 RDNCR*_4_0	RDSR1	Read Status and Configuration Registers	Yes	Yes
	CLVSTR_1_0	CLSR1	Clear Status Register Failure Flags	Yes	No
	ENSPIM_3_0	N/A	Enter SPI mode	Yes	No
	PRNPOR_4_0 RDNPOR_4_0	N/A	Program / Read POR Timer Register	Yes	No
	PGVINC_4_0 RDVINC_4_0 RDVINS_4_0	N/A	Program / Read Interrupt Configuration and Status Registers	Yes	No
	Note [3]	SBL	Set burst length	Yes	Yes
Read array	RDMARY_1_0	READ*B FAST_READ*B	Read memory array	Yes	Yes
Program array	PGWORD_4_0 LDBUFR_6_0 PGBFCM_1_0 RSTWBA_3_0	PP*B	Program memory array	Yes	Yes
Erase	ERCHIP_6_0	CE	Erase chip	Yes	Yes
	ERSCTR_6_0	SE*B BE*B	Sector erase	Yes	Yes
	BLKCHK_1_0	N/A	Blank check	Yes	No
	EVERST_1_0	N/A	Evaluate erase status	Yes	No
Suspend and resume	SPERSE_1_0	PGM/ERS Suspend	Suspend erase	Yes	Yes
	SPPROG_1_0		Suspend program	Yes	Yes
	RSERSE_1_0	PGM/ERS Resume	Resume erase	Yes	Yes
	RSPROG_1_0		Resume program	Yes	Yes
Secure Silicon Region	SSRENT_3_1	ENSO	Secure Silicon Region ASO entry	Yes	Yes
	RD_SSR_1_1	READ*B FAST_READ*B	Read secure Silicon Region	Yes	Yes
	PG_SSR_4_1	PP*B	Program Secure Silicon Region word	Yes	Yes
	LDBSSR_5_1		Load secure Silicon Region buffer	Yes	No

3 To set wrap length, use the Program Register transaction PGNCR1_4_0 to write to Configuration Register 1 bits [1:0].

Transaction summary

Function	Transaction name		Description	Supported	
	SEMPER™ flash	Macronix OctaFlash		SEMPER™ flash	Macronix OctaFlash
	PG_SSR_4_1		Program secure Silicon Region buffer	Yes	Yes
	RSWSSR_3_1	N/A	Reset write to buffer abort status flag	Yes	No
	ASOEXT_1_1	EXSO	Secure Silicon Region ASO exit	Yes	Yes
Array protection	ASPENT_3_1	N/A	Advance sector protection ASO entry	Yes	No
	PGOASP_2_1	WRSCUR	Program Advanced Sector Protection Register	Yes	Yes
	RDOASP_1_1	RDSCUR	Read Advance Sector Protection Register	Yes	Yes
	ASOEXT_1_1	N/A	Advanced sector protection ASO exit	Yes	No
Password	PWDENT_3_1	N/A	Password ASO entry	Yes	No
	PGNPWD_2_1	WRPASS	Program password	Yes	Yes
	RDNPWD_1_1	RDPASS	Read password	Yes	Yes
	ULNPWD _7_1	PASSULK	Unlock password	Yes	Yes
	ASOEXT_1_1	N/A	Password ASO Entry	Yes	No
Persistent Protection bits	PPBENT_3_1	N/A	Persistent Protection bits ASO entry	Yes	No
	PGNPPB_2_1	WRSPB	Program Persistent Protection bits	Yes	Yes
	ERNPPB_2_1	ESSPB	Erase Persistent Protection bits	Yes	Yes
	RSWPPB_3_1	N/A	Reset write to buffer abort status flag	Yes	No
	RDNPPB_1_1	RDSPB	Read Persistent Protection bits	Yes	Yes
	PRTSTS_2_1	N/A	Sector protection status	Yes	No
	ASOEXT_1_1	N/A	Persistent Protection bits ASO exit	Yes	No
PPB lock	PPLENT_3_1	N/A	Persistent protection lock ASO entry	Yes	No
	CLVPPL_2_1	WRLR	PPB Lock bit clear	Yes	Yes
	RDVPPL_1_1	RDLR	PPB Lock bit read	Yes	Yes
	ASOEXT_1_1	N/A	Persistent Protection lock ASO exit	Yes	No
Dynamic Protection bits	DYBENT_3_1	N/A	Dynamic Protection bits ASO entry	Yes	No

Transaction summary

Function	Transaction name		Description	Supported	
	SEMPER™ flash	Macronix OctaFlash		SEMPER™ flash	Macronix OctaFlash
	STVDYB_2_1	WRDPD	Set Dynamic Protection bits	Yes	Yes
	CLVDYB_2_1		Clear Dynamic Protection bits	Yes	Yes
	RDVDYB_1_1	RDDPB	Read Dynamic Protection bits	Yes	Yes
	ASOEXT_1_1	N/A	Dynamic Protection bits ASO exit	Yes	No
Interface CRC	ICRCEN_3_1	N/A	Interface CRC Register ASO entry	Yes	No
	RDICRC_1_1	N/A	Read Volatile Interface CRC Register	Yes	No
	ASOEXT_1_1	N/A	Interface CRC Register ASO exit	Yes	No
Data integrity CRC	DICREN_3_1	N/A	Data Integrity CRC Register ASO entry	Yes	No
	LDSTAD_1_1	N/A	Load start address	Yes	No
	LDENAD_1_1	N/A	Load end address	Yes	No
	SP_DIC_1_1	N/A	Suspend data integrity CRC	Yes	No
	RDCMRY_1_1	N/A	Read memory array during DIC suspend	Yes	No
	RS_DIC_1_1	N/A	Resume data integrity CRC	Yes	No
	RDDICL_2_1	N/A	Read Data Integrity CRC Register Lower Word	Yes	No
	RDDICU_2_1	N/A	Read Data Integrity CRC Register Upper Word	Yes	No
	ASOEXT_1_1	N/A	Interface CRC Register ASO exit	Yes	No
AutoBootN	ATBNEN_3_1	N/A	AutoBoot ASO entry	Yes	No
	PGNATB_2_1	WRFBR	Program AutoBoot Register	Yes	Yes
	RDATBN_1_0	RDFBR	Read AutoBoot Register	Yes	Yes
	ASOEXT_1_1	N/A	AutoBoot ASO exit	Yes	No
Endurance Flex	ENX_EN_3_1	N/A	Endurance Flex pointer ASO entry	Yes	No
	PGOENX_2_1	N/A	Program Endurance Flex Registers	Yes	No
	RDOENX_1_1	N/A	Read Endurance Flex Registers	Yes	No

Transaction summary

Function	Transaction name		Description	Supported	
	SEMPER™ flash	Macronix OctaFlash		SEMPER™ flash	Macronix OctaFlash
	ASOEXT_1_1	N/A	Endurance Flex pointer ASO exit	Yes	No
Reset	N/A	RSTEN	Resete	N/A	Yes
	SRASOE_1_0	RST	Software ereset	Yes	Yes
DPD	ENDPD_0_0	DPD	Enter Deep Power-Down mode	Yes	Yes
	Note [4]	RES	Release from Deep Power-Down mode	Yes	Yes

13.1.2 SEMPER™ flash and OctaFlash SPI transaction comparison

Table 12 summarizes the supported SPI transactions for each device. Pertinent differences will be discussed in subsequent sections. The SEMPER™ flash family has new definition of transaction names for easier recognition of the transaction operation.

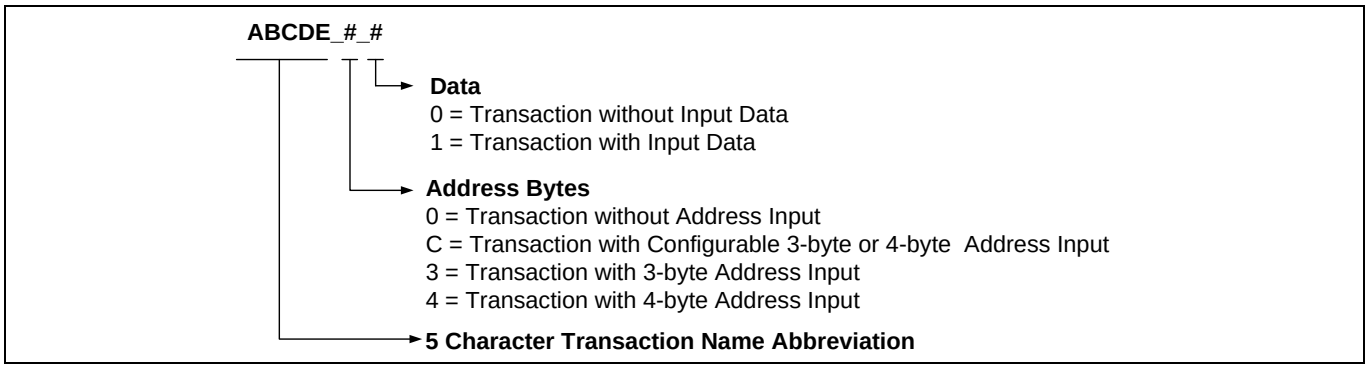

Figure 2 SEMPER™ flash SPI transaction name decoder

4 To exit Deep Power-Down Mode, toggle CS# LOW.

Transaction summary

Table 12 SEMPER™ flash and OctaFlash SPI transaction comparison

Function	Transaction name		Description	Command code	
	SEMPER™ HYPERBUS™	Macronix OctaFlash		SEMPER™ HYPERBUS™	Macronix OctaFlash
Identification	RDIDN_0_0	RDID	Read Identification Register	9F	9F
	RSFDP_3_0	RDSFDP	Read serial flash discovery parameters	5A	5A
	RDUID_0_0	N/A	Read Unique Identification Register	4C	N/A
Register Access	WRENB_0_0	WREN	Writee (non-volatile)	06	06
	WRDIS_0_0	WRDI	Write disable	04	04
	RDSR1_0_0	RDSR	Read Status Register 1-1	05	05
	RDSR2_0_0	N/A	Read Status Register-2	07	N/A
	RDECC_4_0	N/A	ECC read	18	N/A
	CLECC_0_0	N/A	Clear ECC Register(s)	1B	N/A
	CLPEF_0_0	N/A	Clear program and erase failure flags	30 /82	N/A
	RDARG_4_0	RDCR	Read Any Register	65	71
	WRARG_4_1	WRCR	Write any Register	71	72
	N/A	SBL	Set burst length	Note [5]	C0
Read array	RDAY1_C_0	READ3B	Read normal	03	03
	RDAY1_4_0	READ4B	Read normal (4-byte)	13	13
	N/A	FAST_READ3B	Fast read	N/A	0B
	RDAY2_4_0	FAST_READ4B	Fast read (4-byte)	0C	0C
Program array	N/A	PP3B	Program page	N/A	02
	PRPGE_4_1	PP4B	Program page (4-byte)	12	12
	ER004_4_0	SE4B	Parameter sector erase 4 KB (4-byte)	21	21
	ERCHP_0_0	CE	Chip erase	60 / C7	60 / C7
	EVERS_4_0	N/A	Evaluate erase status	D0	N/A
	N/A	SE2	Sector erase 256 KB	N/A	D8
	ER256_4_0	BE4B	Sector erase 256 KB (4-Byte)	DC	DC

5 To set Wrap Length, use Write Any Register transaction WRARG_C_1 to write to Configuration Register 4 bits [1:0].

Transaction summary

Function	Transaction name		Description	Command code	
	SEMPER™ HYPERBUS™	Macronix OctaFlash		SEMPER™ HYPERBUS™	Macronix OctaFlash
Erase / program / DIC suspend / resume	SPEPD_0_0	PGM/ERS Suspend	Erase / program / DIC suspend	75 / 85	B0
	RSEPD_0_0	PGM/ERS Resume	Erase / program / DIC resume	30 / 7A / 8A	30
Secure Silicon Region	PRSSR_4_1	N/A	Program secure Silicon Region	42	N/A
	RDSSR_4_0	N/A	Read secure Silicon Region	4B	N/A
Array protection		WRSCUR	Advanced Sector Protection Register program / write		2F
	WRPLB_0_0	N/A	PPB Lock bit write	A6	N/A
	RDPLB_0_0	N/A	PPB Lock bit read	A7	N/A
	RDDYB_4_0	RDDPB	DYB read	E0	E0
	WRDYB_4_1	WRDPB	DYB write	E1	E1
	RDPPB_4_0	RDSPB	PPB read	E2	E2
	PRPPB_4_0	WRSPB	PPB program	E3	E3
	ERPPB_0_0	ESSPB	PPB erase / clear	E4	E4
	PWDUL_0_1	PASSULK	Password unlock - 1	E9	29
	Note [6]	PASSRD	Password read	N/A	27
	Note [7]	WRPASS	Password program	N/A	28
CRC	DICHK_4_1	N/A	Data integrity check	5B	N/A
Reset	SRSTE_0_0	RSTEN	Reset enable	66	66
	SFRST_0_0	RST	Software reset	99	99
DPD	ENDPD_0_0	DPD	Enter Deep Power-Down mode	B9	B9
	Note [8]	RES	Release from Deep Power-Down mode	N/A	AB

6 To read the password, use the Read Any Register transaction RDARG_4_0.

7 To program the password, use the Write Any Register transaction WRARG_4_1.

8 To exit Deep Power-Down Mode, toggle CS# LOW.

14 Summary

The Infineon SEMPER™ flash family adopts the transaction set of traditional PNOR flash memory devices, such as the Infineon S29GL-S family. The typical HYPERBUS™ controller integrated in the host system translates the software accesses to the HYPERBUS™ signal protocol. Furthermore, the SEMPER™ flash family also supports a legacy SPI mode that allows existing bootloaders to read out the memory contents using single I/O SPI transactions. Therefore, the SEMPER™ flash HYPERBUS™ family is compatible with the Macronix OctaFlash family in terms of physical interface and software functionalities. You can transition from Macronix OctaFlash to SEMPER™ flash with these software migration guidelines.

Related documents

NOR flash documents

[1] SEMPER™ flash family datasheet.:

- **002-12337** – S26HS256T/ S26HS512T / S26HS01GT / S26HL256T / S26HL512T / S26HL01GT, 256-Mb (32-MB), 512-Mb (64-MB), 1-Gb (128-MB) HS-T (1.8-V), HL-T (3.0-V) SEMPER™ flash with HYPERBUS™ interface

[2] Programmer's guide

- **001-99195** – Programmer's guide for Infineon HYPERFLASH™ family:

[3] Endurance flex architecture application note:

- **002-18481** – Endurance flex explained - Wear-leveling techniques and usage in Infineon's SEMPER™ flash devices

Revision history

Document version	Date of release	Description of changes
**	2018-03-30	New application note.
*A	2018-12-03	Combined the 1.8 V AN218665 Application note. Updated Sector Mapping section. Added section Performance and Feature Comparison. Added section Signal Description. Added section Electrical Characteristics.
*B	2019-12-09	Added 1 Gb devices.
*C	2021-02-26	Migrated to Infineon template.
*D	2022-07-15	Updated the parameters in Table 1 to Table 5 to align with the S26HL-T datasheet. Removed transaction name “PGNINC_4_0” from Table 11. Removed transaction name “PRASP_0_1” from Table 12.

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