Migration Guide for 45-nm S25HS-T SEMPER™ Flash Quad SPI from 65-nm S25FS-S Quad SPI Flash

About this document

Scope and purpose

AN218550 discusses the new features of the Infineon S25HS-T SEMPER™ Flash Quad SPI family and software considerations the designer should make when migrating from the Infineon 65-nm S25FS-S Quad SPI 1.8-V Flash family.

Intended audience

The document is intended for software developers who are writing low-level drivers, setup software, or application software for the S25HS-T devices.

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1 Introduction

As a flash user, you may already be familiar with the basic operations in SPI flash devices: Read, Program, and Erase. The S25HS-T SEMPER™ Flash Family (S25HS512T and S25HS01GT) provides many other features to satisfy the diverse needs of different users. This document is not intended to repeat the basic operations described in the datasheet, but to point out some important information in the datasheet that might be overlooked by users. You should first seek to understand the datasheet before reading this document, especially if you are not familiar with Infineon SPI devices in general. The document is intended for software developers who are writing low-level drivers, setup software, or application software for the S25HS-T devices.

This migration guide discusses new features of the S25HS-T SEMPER™ Flash Family and software considerations the designer should make when migrating from the S25FS-S family. The S25HS-T is a 1.8-V, flash memory device based on 45-nm advanced MIRRORBIT™ technology.

2 Sector architecture

The sector architecture in the S25HS-T SEMPER™ Flash family is very flexible. It provides both large “normal” sectors and small “parameter” sectors. Large sectors are 256 KB and parameter sectors are 4 KB in size. A small set of 32 parameter sectors can be located at the lowest (bottom) or highest (top) address of a device or split with 16 parameter sectors both top and bottom. Parameter sectors can also be removed from the address space of the device so that all sectors are uniform in size. The S25FS-S family only provides eight parameter sectors available at the top or bottom of the memory array.

To erase these two types of sectors, small parameter sectors and uniform size sectors, S25HS-T provides two sets of transactions:

- Parameter 4-KB Erase. Two transactions are provided: 20h (ER004_C_0) for use with 3- or 4-byte addressing; 21h (ER004_4_0) for use with 4-byte addressing.
- 256-KB Uniform Sector Erase. Two transactions are provided: D8h (ER256_C_0) for use with 3- or 4-byte addressing; DCh (ER256_4_0) for use with 4-byte addressing.

To erase parameter sectors, you need to use the ER004_C_0 or ER004_4_0 transaction. To erase uniform sectors, you need to use the ER256_C_0 or ER256_4_0 transaction.

Configuration Register-1 non-volatile bit 6 (CFR1V[6]) equal to 1 defines the contiguous logical location of the parameter sectors; the sectors are split with half at the highest and half at the lowest memory address space when (CFR1V[6]) equals to 1. When (CFR1V[6]) is equal to 0, the parameter sectors are contiguous in memory and their logical location of the parameter sectors is selected by CFR1V[2].

Configuration Register-1 non-volatile bit 2 (CFR1V[2]) equal to 0 overlays the parameter sectors at the bottom of the lowest address uniform sector. CFR1V[2] equal to 1 overlays the parameter sectors at the top of the highest address uniform sector.

There is a configuration option to remove the 4 KB parameter sectors from the address map so that all sectors are uniform size. Configuration Register-3 volatile bit 3 (CFR3V[3]) equal to 0 selects the hybrid sector architecture with 4 KB parameter sectors. CFR3V[3]=1 selects the uniform sector architecture without parameter sectors.

Table 1 to **Table 7** show all sector combinations an S25HS512T and S25FS512S devices may have.

Table 1 S25HS512T sector address map (256 KB uniform sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
256	256	SA00	00000000h-0003FFFFh	Sector Starting Address
		:	:	
		SA255	03FC0000h-03FFFFFFh	— Sector Ending Address

Note: Configuration: CFR3N[3]=1.

Table 2 S25HS512T sector address map (Bottom thirty-two 4 KB sectors and 256 KB uniform sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
4	32	SA00	00000000h-00000FFFh	

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
		:	:	Sector Starting Address — Sector Ending Address
		SA31	0001F000h-0001FFFFh	
128	1	SA32	00020000h-0003FFFFh	
256	255	SA33	00040000h-0007FFFFh	
		:	:	
		SA287	03FC0000h-03FFFFFFh	

Note: Configuration: CFR3N[3]=0, CFR1N[6]=0, CFR1N[2]=0. This is the default configuration.

Table 3 S25HS512T sector address map (Top thirty-two 4 KB sectors and 256 KB uniform sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
256	255	SA00	0000000h-003FFFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA254	03F80000h-03FBFFFFh	
128	1	SA255	03FC0000h-03FDFFFFh	
4	32	SA256	03FE0000h-03FE0FFFh	
		:	:	
		SA287	03FFF000h-03FFFFFFh	

Note: Configuration: CFR3N[3]=0, CFR1N[6]=0, CFR1N[2]=1.

Table 4 S25HS512T sector address map (Bottom sixteen and top sixteen 4 KB sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
4	16	SA00	00000000h-00000FFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA15	0000F000h-0000FFFFh	
192	1	SA16	00010000h-0003FFFFh	
256	254	SA17	00040000h-0007FFFFh	
		:	:	
		SA270	03F80000h-03FBFFFFh	
192	1	SA271	03FC0000h-03FEFFFFh	
4	16	SA272	03FF0000h-03FF0FFFh	
		:	:	
		SA287	03FFF000h-03FFFFFFh	

Note: Configuration: CFR3N[3]=0, CFR1N[6]=1.

Table 5 S25FS512S sector address map (Bottom eight 4 KB sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
4	8	SA00	00000000h-00000FFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA7	00007000h-00007FFFh	
224	1	SA8	00008000h-0003FFFFh	
256	255	SA9	00040000h-0007FFFFh	
		:	:	
		SA263	03FC0000h-03FFFFFFh	

Table 6 S25FS512S sector address map (Top eight 4 KB sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
256	255	SA00	00000000h-00000FFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA254	03F80000h-03FBFFFFh	
224	1	SA255	03FC0000h -03FF7FFFh	
4	8	SA256	03FF8000h-03FF8FFFh	
		:	:	
		SA263	03FFF000h-03FFFFFFh	

Table 7 S25FS512S sector address map (256 KB uniform sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Notes
256	256	SA00	00000000h-0003FFFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA255	03FC0000h-03FFFFFFh	

Table 1 to **Table 7** show the sector architectures of S25HS512T and S25FS512S devices. Some of the configurations show a mid-size sector due to the memory overlay. You should make sure the address associated with the Sector Erase transaction is correct.

The same principle will apply to S25HS01GT devices. The only difference is the total number of uniform sectors.

In the S25HS-T SEMPER™ Flash family devices, you have an option to enable the blank check feature during an erase. By default, when an erase transaction is issued, the sector is unconditionally erased. However, if the blank check feature is enabled, by turning ON the Bit 5 of the Configuration Register 3 (CFR3x[5]), the device will first check if the last erase was successfully completed on this sector (using the Evaluate Erase Status transaction described in the next section) and the sector is all blank. If so, it returns successful erase status. This dramatically reduces the erase time. If the blank check finds any '0' values in the array, the erase operation starts immediately.

This blank check feature is very useful, especially in the manufacturing environment where often the devices being programmed are new. However, to make sure the programming is successful, most manufacturer software will perform an erase regardless. With the blank check feature enabled, the erase time will be improved dramatically while erasing a non-blank sector.

3 Addressing schemes

For devices that are 128 Mb or less, an address length of 3 bytes is sufficient to address the whole device. For devices that are of higher densities, an address length of 4 bytes is needed. To accommodate these different address length requirements, the S25HS-T and S25FS-S family devices provide two alternatives:

- A set of transactions that always require a 4-byte address. These transactions can be used to access up to 32 Gb of memory. The transactions include all read transactions, page program transactions, erase transactions, and DYB/PPB protection transactions.
- A 4-byte addressing mode for 3-byte address transactions. This mode is controlled by the ADRBYT bit (Bit 7) in Configuration Register 2 (CFR2x[7]). When this bit is set to ‘1’, all standard 3-byte address transactions require 4-byte addressing. The default of this bit is ‘0’, that is, the 3-byte addressing scheme.

Note that when ADRBYT bit is set to 4-byte addressing mode, all standard 3-byte transactions require 4-byte addresses, except RSFDP_3_0 (5Ah). This transaction always uses 3-byte addressing scheme, regardless of the current addressing mode as required by the JEDEC JESD216 (SFDP) standard.

4 Features comparison

The S25HS-T supports a superset of the S25FS-S feature set. **Table 8** summarizes the feature similarities and differences, which are discussed in detail in later sections.

Table 8 Feature comparison

		S25HS-T SEMPER™		S25FS-S			
		S25HS512T	**S25HS01GT**	**S25FS064S**	**S25FS128S**	**S25FS256S**	**S25FS512S**
Features	Technology	45-nm MIRRORBIT™		65-nm MIRRORBIT™			
	Density	512 Mb	1 Gb	64 Mb	128 Mb	256 Mb	512 Mb
	VCC	1.7 V to 2.0 V		1.7 V to 2.0 V			
	Temp range	– 40°C to + 85°C – 40°C to + 105°C – 40°C to + 125°C		– 40°C to + 85°C – 40°C to + 105°C – 40°C to + 125°C			
	Data Bus Width	SPI (x1), DIO (x2), QIO (x4), QPI (x4)					
	Erase Sector Size	4 KB / 256 KB		4 KB / 64 KB / 256 KB			4 KB / 256 KB
	Page Size	256 B / 512 B		256 B / 512 B			
	Burst Read/Wrap	Yes		Yes			
	Security Regions	32 x 32 B		32 x 32 B			
	Cycling Endurance	1.280 M Cycles min[1]	2.560 M Cycles min[1]	100 K Cycles min			
	Data Retention	25 Years[1]		20 Years			
	AutoBoot	Yes		No			
	ECC	Yes		Yes			
	Data Integrity Check (DIC)	Yes		No			
	Endurance Flex	Yes		No			
	SafeBoot	Yes		No			
Package	SOIC 8 (208 mil)	No	No	Yes	Yes	No	No
	SOIC 16 (300 mil)	Yes	Yes	No	No	Yes	Yes
	8 - Contact WSON (8x6 mm)	Yes	No	No	Yes	Yes	Yes

1. See datasheet for details on cycling and data retention specification.

Features comparison

		S25HS-T SEMPER™		S25FS-S			
		S25HS512T	**S25HS01GT**	**S25FS064S**	**S25FS128S**	**S25FS256S**	**S25FS512S**
	8 - Contact WSON (5x6 mm)	No	No	No	Yes	No	No
	BGA 24-ball (8x6 mm) (5x5 ball)	Yes	No	Yes	Yes	Yes	Yes
	BGA 24-ball (8x6 mm) (4x6 ball)	No	No	No	Yes	Yes	No
	BGA 24-ball (8x8 mm) (5x5 ball)	No	Yes	No	No	No	No
	LGA (5x6 mm)	No	No	Yes	No	No	No
Options	Reset#	Yes		Yes	No	No	No
	IO3/Reset#	Yes		Yes			
	Legacy Protection BP[x]	Yes		Yes			
	Security Protection	Advance Sector Protect (ASP)		ASP			
	Program Suspend / Resume	Yes		Yes			
	Erase Suspend / Resume	Yes		Yes			
	Parameter Table	Serial Flash Discoverable Parameters (SFDP)		SFDP			
	Status Register Protect	Yes		Yes			

5 New features

5.1 Endurance flex architecture (Wear-leveling)

Endurance flex architecture allows partitioning of the main memory array into regions which can be configured as either high-endurance or long-retention. Endurance flex implements wear-leveling in high-endurance regions where program/erase cycles are spread evenly across all sectors, which are part of the wear-leveling pool. This greatly improves the reliability of the device by avoiding premature wear-out of an individual sector.

Architecturally, Endurance flex's wear-leveling algorithm is based on a mapping of logical sectors to physical sectors. During the lifetime of the part, this mapping is changed to maintain a uniform distribution of program/erase cycles over all physical sectors. The logical to physical mapping information is stored in a dedicated flash array, which is updated when sectors are swapped. Sector swaps occur when an erase transaction is given.

Endurance flex's high-endurance region requires a minimum set of 20 sectors. To provide flexibility between configuring long-retention, high-endurance, or both regions, a four-pointer architecture is provided. The factory default setting designates all sectors as high-endurance as part of the wear-leveling pool with all pointers disabled. The four pointers can be used to form a maximum of five regions which can each be configured as either long-retention or high-endurance. The pointers are one-time-programmable and must be configured during the initial device setup.

Data that is frequently updated should be stored in high-endurance partitions to enable the highest number of program/erase cycles and longest device lifespan. Boot code which is infrequently updated should be stored in long-retention partitions to enable highly-reliable 25-year retention.

Note: *4-KB sectors are not part of the endurance flex architecture. Only the main array 256 KB sectors are included.*

See the datasheet and endurance flex application note for detailed definitions of endurance flex.

5.2 AutoBoot

SPI devices normally require 32 or more cycles of transaction and address shifting to initiate a read transaction. To read boot code from an SPI device, the host memory controller or processor must supply the read transaction from a hardwired state machine or from some host processor internal ROM code.

The AutoBoot feature allows the host memory controller to take boot code from an S25HS-T SEMPER™ flash family device immediately after the end of reset, without having to send a read transaction. This saves 32 or more cycles and simplifies the logic needed to initiate the reading of boot code.

See the datasheet for definitions of AutoBoot.

5.3 Data integrity check

The data integrity check transaction sequence causes the device to perform a cyclic redundancy check (CRC) calculation over a user defined address range. The CRC process calculates the check-value on the data contained at the starting address through the ending address.

See the datasheet for detailed definitions of data integrity check.

5.4 Sector erase count

The S25HS-T SEMPER™ flash family has a new transaction that allows the software to check the sector erase count. The transaction outputs the number of erase cycles for the sector of the given address. Each sector's erase cycle count information is stored in counters in a dedicated flash array which record the number of erase cycles performed on that sector. The sector erase count sequence outputs the number of erase cycles for the sector of the given address.

See the datasheet for detailed definitions of sector erase count.

5.5 ECC error address trap

A register is provided to capture the data unit address where an ECC error is first encountered during a read of the flash array. The Error Lower Address Register and Error Upper Address Register contain the address that was accessed when the error is detected. The failing bits may not be located at the exact address indicated in the registers but will be located within the aligned 16-byte ECC data unit where the error was detected. If errors are found in multiple data units during a single read operation, the address of the first failing data unit address is captured in the Error Lower and Upper Address registers.

See the datasheet for detailed definitions of ECC error address trap.

5.6 ECC error detection counter

A counter is provided to keep track of the number of 1-bit or 2-bit errors that occur as data units are read from the flash array. Only errors recognized in the main array will cause the error detection counter to increment. The counter will be set to 0 on POR, hardware reset, or with the ECC clear transaction.

The detailed definitions of the error detection counter can be found in the datasheet.

5.7 SafeBoot

Power on initialization failure or corrupt registers can render the device unusable. If it is not a catastrophic failure, such as, the firmware getting permanently corrupted, it is possible to potentially recover the device. The SafeBoot feature uses status register polling sequence to detect if there is a Power-On Failure or Register Corruption occurred.

See the datasheet for detailed definitions of the SafeBoot process.

5.7.1 Power on detection

During the device initialization process, a failure may occur and make the device unusable. A hardware reset initiated by the master controller (host) can potentially recover the device. S25HS-T family devices provide a failure signature (0x61) in its status register upon detecting an initialization breakdown. The host will need to go through a status register polling process to determine if a hardware reset is needed to re-initialize the device.

See the datasheet for detailed definitions of the bootup failure recovery process.

5.7.2 Configuration corruption detection

A WRR or WRAR transaction sequence to non-volatile configuration registers may get interrupted by a brown out or hardware reset; this will corrupt the configuration data. The S25HS-T family device can detect a corrupted configuration and enter a default mode where the device can be accessed, while providing a configuration corruption signature in its status register. The host can detect this to initiate reprogramming of the non-volatile configuration registers' data.

See the datasheet for detailed definitions of the configuration corruption detection process.

6 Transaction set comparison

Table 9 summarizes the supported transactions for each device. Pertinent differences will be discussed in subsequent sections. The SEMPER™ flash family has new definition of transaction names for easier recognition of the transaction operation.

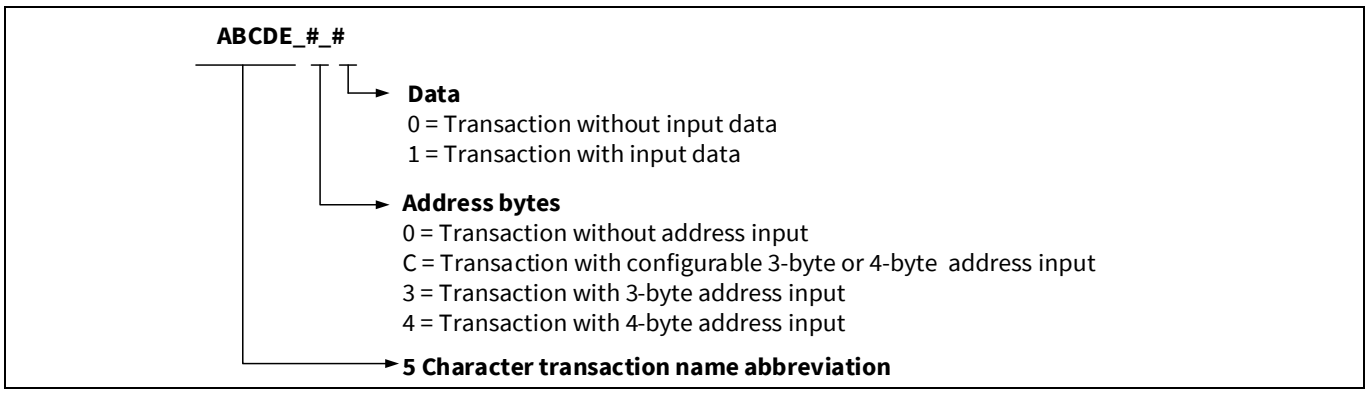

Figure 1 SEMPER™ flash transaction name decoder

Table 9 Transaction set comparison

Function	Transaction name		Description	Command code	
	S25HS-T SEMPER™	S25FS-S		S25HS-T SEMPER™	S25FS-S
Array protection	PRASP_0_1	ASPP	Advanced Sector Protection Register Program / Write	2F	2F
	WRPLB_0_0	PLBWR	PPB Lock Bit Write	A6	A6
	RDPLB_0_0	PLBRD	PPB Lock Bit Read	A7	A7
	RDDYB_4_0	4DYBRD	DYB Read (4-Byte)	E0	E0
	WRDYB_4_1	4DYBWR	DYB Write (4-Byte)	E1	E1
	RDPPB_4_0	4PPBRD	PPB Read (4-Byte)	E2	E2
	PRPPB_4_0	4PPBP	PPB Program (4-Byte)	E3	E3
	ERPPB_0_0	PPBE	PPB Erase / Clear	E4	E4
	PWDUL_0_1	PASSU1	Password Unlock - 1	E9	E9
	RDDYB_C_0	DYBRD	DYB Read	FA	FA
	WRDYB_C_1	DYBWR	DYB Write	FB	FB
	RDPPB_C_0	PPBRD	PPB Read	FC	FC
	PRPPB_C_0	PPBP	PPB Program / PPB Write	FD	FD
	Note[2]	**PASSRD**	**Password Read**	**N/A**	**E7**
	PRPWD_0_1	PASSP	Password Program / Password Write	E8	E8
CRC	**DICHK_4_1**	**N/A**	**Data Integrity Check**	**5B**	**N/A**
Erase / program /	SPEPD_0_0	EPCS	Erase / Program / DIC Suspend	75	75
	SPEPA_0_0	EPS		85	85

2. To read the password, use the Read Any Register transaction RDARG_C_0.

Transaction set comparison

Function	Transaction name		Description	Command code	
	S25HS-T SEMPER™	**S25FS-S**		**S25HS-T SEMPER™**	**S25FS-S**
DIC suspend / resume			Erase / Program Suspend Alternate	B0	B0
	RSEPD_0_0	EPCR	Erase / Program / DIC Resume	7A	7A
	RSEPA_0_0	EPR	Erase / Program Resume Alternate	8A	8A
				30	30
Erase array	ER004_C_0	P4E	Parameter Sector Erase 4 KB	20	20
	ER004_4_0	4P4E	Parameter Sector Erase 4 KB (4-Byte)	21	21
	SEERC_C_0	**N/A**	**Sector Erase Count**	**5D**	**N/A**
	ERCHP_0_0	BE	Chip Erase	60	60
	ERCHP_0_0	BE	Chip Erase	C7	C7
	EVERS_C_0	EES	Evaluate Erase Status	D0	D0
	ER256_C_0	SE2	Sector Erase 256 KB	D8	D8
	ER256_4_0	4SE2	Sector Erase 256 KB (4-Byte)	DC	DC
Identification	**RDUID_0_0**	**N/A**	**Read Unique Identification Register**	**4C**	**N/A**
	RSFDP_3_0	RSFDP	Read Memory Discovery Parameters	5A	5A
	RDIDN_0_0	RDID	Read Identification Register	9F	9F
	RDQID_0_0	RDQID	Quad Read Identification Register	AF	AF
Secure silicon region	PRSSR_C_1	OTPP	Program Secure Silicon Region	42	42
	RDSSR_C_0	OTPR	Read Secure Silicon Region	4B	4B
Program array	PRPGE_C_1	PP	Program Page	02	02
	PRPGE_4_1	4PP	Program Page (4-Byte)	12	12
Read array	RDAY1_C_0	READ	Read Normal	03	03
	RDAY1_4_0	4READ	Read Normal (4-Byte)	13	13
	RDAY2_C_0	FAST_READ	Fast Read	0B	0B
	RDAY2_4_0	4FAST_READ	Fast Read (4-Byte)	0C	0C
	RDAY4_C_0	DIOR	Read Dual I/O	6B	BB
	RDAY4_4_0	4DIOR	Read Dual I/O (4-Byte)	6C	BC
	RDAY2_C_0	**N/A**	**Read Quad Output**	**0B**	**N/A**
	RDAY2_4_0	**N/A**	**Read Quad Output (4-Byte)**	**0C**	**N/A**
	RDAY4_C_0	QIOR	Read Quad I/O	6B	EB
	RDAY4_4_0	4QIOR	Read Quad I/O (4-Byte)	6C	EC
	RDAY5_C_0	DDRQIOR	Read Double Data Rate Quad I/O	EB	ED
	RDAY5_4_0	4DDRQIOR	Read Double Data Rate Quad I/O (4-Byte)	EC	EE

Transaction set comparison

Function	Transaction name		Description	Command code	
	S25HS-T SEMPER™	S25FS-S		S25HS-T SEMPER™	S25FS-S
Register access	WRREG_0_1	WRR	Write Register (Status & Configuration)	01	01
	WRDIS_0_0	WRDI	Write Disable	04	04
	RDSR1_0_0	RDSR1	Read Status Register 1-1	05	05
	WRENB_0_0	WREN	Write Enable (Non-volatile)	06	06
	RDSR2_0_0	RDSR2	Read Status Register-2	07	07
	WRAUB_0_1	**N/A**	**AutoBoot Register Write**	**15**	**N/A**
	RDECC_4_0	4ECCRD	ECC Read (4-Byte)	18	18
	RDECC_C_0	ECCRD	ECC Read	19	19
	CLECC_0_0	**N/A**	**Clear ECC Register(s)**	**1B**	**N/A**
	CLPEF_0_0	CLSR1	Clear Program and Erase Failure Flags	30	30
		CLSR2	Clear Program and Erase Failure Flags	82	82
	RDCR1_0_0	RDCR1	Read Configuration Register-1	35	35
	RDDLP_0_0	DLPRD	Read Data Learning Pattern	41	41
	PGDLP_0_1	PNVDLR	Program Data Learning Register	43	43
	WRDLP_0_1	WVDLR	Write Data Learning Register	4A	4A
	WREV_0_0	**N/A**	**Write Enable (Volatile)**	**50**	**N/A**
	RDARG_C_0	RDAR	Read Any Register	65	65
	WRARG_C_1	WRAR	Write any Register	71	71
	EN4BA_0_0	4BAM	Enter 4-byte address mode	B7	B7
	EX4BA_0_0	**N/A**	**Exit 4-byte address mode**	**B8**	**N/A**
	Note[3]	**SWL2**	**Set Wrap Length**	**N/A**	**C0**
Reset	SRSTE_0_0	RSTEN	Reset Enable	66	66
	SFRST_0_0	RST1	Software Reset	99	99
	SFRSL_0_0	RST2	Legacy Software Reset	F0	F0
DPD	ENDPD_0_0	DPD	Enter Deep Power-Down Mode	B9	B9
	Note[4]	**RES**	**Release from Deep Power-Down Mode**	**N/A**	**AB**

3. To Set Wrap Length, use the Write Any Register transaction WRARG_C_1 to write to Configuration Register 4 bits [1:0].

4. To exit Deep Power-Down Mode, toggle CS# LOW.

7 Page programming, data alignment, and ECC

The S25HS-T SEMPER™ flash family supports page programming with page sizes of either 256 or 512 bytes, depending on the value of Bit 4 of Configuration Register 3 (CFR3x[4]). The page size is the maximum amount of data that can be entered in one program transaction. You may program from 1-byte up to the maximum page size. If the data entered crosses the page address boundary, the data pointer is wrapped back to the beginning of the page thus, the previously written data in the buffer may be overwritten.

Many applications store data in multiples of 512 bytes. Programming data to the flash is most efficient when writing in buffer-size lengths and aligned increments. Although smaller writes are allowed, software should be modified to program data in full, address aligned, buffer increments.

For smaller or misaligned data writes, it is important to note that internally, data is programmed in address aligned groups of 16 bytes. For optimal flash performance and reliability, data should be programmed in multiples of full 16-byte aligned groups, up to the buffer size. While multiple program operations within a page are not best practice for S25HS-T devices, they are allowed for compatibility with legacy SPI devices.

For example, a simple flash file system may write two 512-byte file sectors, each with 12 bytes of metadata. Programming this data sequentially causes several misalignments, as shown in **Table 10**.

Table 10 Misaligned data storage

Order	First	Second	Third	Fourth
Size	512 bytes	12 bytes	512 bytes	12 bytes
Byte offset	0	512	524	1036

Data written	Initial 512 bytes			12 bytes	512 bytes				12 bytes	Not written
Internal groups	Group 0	…	Group 31	Group 32	Group 33	…	Group 63	Group 64	Group 65	Group 66

Instead, the writes should be rearranged to maximize programming performance. In **Table 2**, sector data is written from the bottom of flash, and metadata is written from the top. The ‘S’ indicates four bytes that are skipped and left unused. Group ‘N’ is the last group in the device. M is the size of the flash device in bytes.

Table 11 Aligned data storage

Order	First	Second	Third	Fourth
Size	512 bytes	12 bytes	512 bytes	12 bytes
Byte offset	0	M - 16	512	M - 32

Data written	Initial 512 bytes			512 bytes			Not Written	12 bytes	S	12 bytes	S
Internal groups	Group 0	…	Group 31	Group 32	...	Group 63		Group N-1		Group N	

7.1 Automatic ECC

Each 16-byte aligned, and 16-byte length programming block has an error correction code (ECC) value. The data block plus ECC form a data unit. In combination with error detection and correction (EDC) logic, the ECC is used to detect and correct any single bit error found during a read access. When data is first programmed within a data unit, the ECC value is set for the entire data unit. If the same data unit is programmed more than once, the ECC value is changed to disable the EDC function. A sector erase is needed to again enable Automatic ECC on that programming block. The 16-byte programming block is the smallest program granularity on which Automatic ECC is enabled.

When a data unit has Automatic ECC disabled, EDC is not done on data read from the data unit location. If 2-bit ECC error detection is enabled, single byte programming and bit walking in which the same data unit is programmed more than once is not allowed within the same data unit and will result in a Program Error.

See the datasheet for detailed definitions of Automatic ECC.

7.2 Evaluate erase status (EES)

The S25HS-T SEMPER™ flash family has a transaction that allow the software to check if an erase operation was interrupted by a power disruption, a hardware reset, or software reset. Users can first issue this transaction, D0h, with a particular sector address; then read the Bit 2 of the Status Register 2 (STR2x[2]) to check if the last erase on this sector was successfully completed.

Most flash file systems have software mechanisms to detect if an erase is interrupted by a power loss. In that case, it is necessary to re-erase the same sector to ensure the integrity of the flash array. With this new EES transaction, the file system software, or its block driver, can easily check the integrity of the sectors after each power up.

See the datasheet for detailed definitions of evaluate erase status.

8 Status and Configuration registers

The S25HS-T SEMPER™ flash family provides many control and customization abilities to users, through a series of Status and Configuration registers. Most of these registers have two versions: non-volatile and volatile. The register value in a non-volatile register will be retained after a power cycle. The register value in a volatile register is reset back to the same value as its non-volatile counterpart upon device power up.

The existence of a volatile version of the registers provides users the ability to test settings in the early product development phase before programming the value to the non-volatile registers. Some of the bits in non-volatile registers are One Time Programmable (OTP) bits, thus the changes are not reversible. The volatile version of the registers also allows for overriding the value loaded during reset from the non-volatile register.

See the datasheet for detailed definitions of Status and Configuration registers. This document points out some useful information for software developers.

Table 12 Register set comparison/matching

Register	Type	S25HS-T SEMPER™	S25FS-S
Status Register-1	Non-volatile	Yes	Yes
	Volatile	Yes	Yes
Status Register-2	Volatile	Yes	Yes
Configuration Register-1	Non-volatile	Yes	Yes
	Volatile	Yes	Yes
Configuration Register-2	Non-volatile	Yes	Yes
	Volatile	Yes	Yes
Configuration Register-3	Non-volatile	Yes	Yes
	Volatile	Yes	Yes
Configuration Register-4	Non-volatile	Yes	Yes
	Volatile	Yes	Yes
ECC Status Register	Volatile	Yes	No[5]
ECC Data Unit Status	Volatile	Yes	Yes
Advanced Sector Protection Register	Non-volatile	Yes	Yes
ASP Password Register	Non-volatile / OTP	Yes	Yes
ASP PPB Lock Register	Volatile	Yes	Yes
ASP PPB Access Register	Non-volatile	Yes	Yes
ASP DYB Access Register	Volatile	Yes	Yes
Data Learning Registers	Non-volatile	Yes	Yes
	Volatile	Yes	Yes
AutoBoot Register	Non-volatile	Yes	No
Memory Array Data Integrity Check Register	Volatile	Yes	No
Sector Erase Count Register	Volatile	Yes	No
ECC Address Trap Register	Volatile	Yes	No

5 The ECC Status Register for S25HS-T has a different function than the S25FS-S Register. The S25HS-T has the ECC Data Unit Status, which is the same function as the S25FS-S ECC Status Register. See the datasheet for more details.

Register	Type	S25HS-T SEMPER™	S25FS-S
ECC Error Detection Counter Register	Volatile	Yes	No
Endurance flex architecture Selection Registers	OTP	Yes	No

There are two ways to access Status and Configuration registers:

- Traditional method. These transactions exist in older Infineon SPI devices:
  - Using WRREG_0_1 (01h) to write to STR1N, and CFR1N;
  - Using RDSR1_0_0 (05h), RDSR2_0_0 (07h), or RDCR1_0_0 (35h) to read STR1V, STR2V, or CFR1V.

Note that the WRREG_0_1 transaction writes to the non-volatile version of the registers while the read transactions read from the volatile version of the registers. When writing to the non-volatile registers, the volatile version will be updated automatically.

- The preferred method is to use the Read or Write any register transactions to access any registers.
  - WRARG_C_1 (71h) to write to any register
  - RDARG_C_0 (65h) to read any register

To use these transactions, the register addresses in **Table 13** need be used.

Table 13 Register address map

Function	Register type	S25HS-T SEMPER™		S25FS-S	
		Volatile component address (Hex)	Non-volatile component address (Hex)	Volatile component address (Hex)	Non-volatile component address (Hex)
Device status	Status Register 1	00800000	00000000	00800000	00000000
	Status Register 2	00800001	N/A	00800001	N/A
Device configuration	Configuration Register 1	00800002	00000002	00800002	00000002
	Configuration Register 2	00800003	00000003	00800003	00000003
	Configuration Register 3	00800004	00000004	00800004	00000004
	Configuration Register 4	00800005	00000005	00800005	00000005
Endurance flex architecture	Endurance flex Arch. Selection Register 0 [7:0]	N/A	00000050	N/A	N/A
	Endurance flex Arch. Selection Register 0 [15:8]	N/A	00000051	N/A	N/A
	Endurance flex Arch. Selection Register 1 [7:0]	N/A	00000052	N/A	N/A
	Endurance flex Arch. Selection Register 1 [15:8]	N/A	00000053	N/A	N/A
	Endurance flex Arch. Selection Register 2 [7:0]	N/A	00000054	N/A	N/A
	Endurance flex Arch. Selection Register 2 [15:8]	N/A	00000055	N/A	N/A

Function	Register type	S25HS-T SEMPER™		S25FS-S	
		Volatile component address (Hex)	Non-volatile component address (Hex)	Volatile component address (Hex)	Non-volatile component address (Hex)
	Endurance flex Arch. Selection Register 3 [7:0]	N/A	00000056	N/A	N/A
	Endurance flex™ Arch. Selection Register 3 [15:8]	N/A	00000057	N/A	N/A
	Endurance flex Arch. Selection Register 4 [7:0]	N/A	00000058	N/A	N/A
	Endurance flex Arch. Selection Register 4 [15:8]	N/A	00000059	N/A	N/A
Error correction	ECC Status Register	00800089	N/A	N/A	N/A
	ECC Count Register [7:0]	0080008A	N/A	N/A	N/A
	ECC Count Register [15:8]	0080008B	N/A	N/A	N/A
	ECC Count Register [23:16]	0080008C	N/A	N/A	N/A
	ECC Count Register [31:24]	0080008D	N/A	N/A	N/A
	ECC Address Trap Register [7:0]	0080008E	N/A	N/A	N/A
	ECC Address Trap Register [15:8]	0080008F	N/A	N/A	N/A
	ECC Address Trap Register [23:16]	00800040	N/A	N/A	N/A
	ECC Address Trap Register [31:24]	00800041	N/A	N/A	N/A
AutoBoot	AutoBoot Register [7:0]	00800042	00000042	N/A	N/A
	AutoBoot Register [15:8]	00800043	00000043	N/A	N/A
	AutoBoot Register [23:16]	00800044	00000044	N/A	N/A
	AutoBoot Register [31:24]	00800045	00000045	N/A	N/A
Data Learning	Data Learning Register [7:0]	00800010	00000010	00800010	00000010
	Data Learning Register [15:8]	00800011	00000011	N/A	N/A
Erase Count	Sector Erase Count [7:0]	00800091	N/A	N/A	N/A
	Sector Erase Count [15:8]	00800092	N/A	N/A	N/A
	Sector Erase Count [23:16]	00800093	N/A	N/A	N/A
Data Integrity Check	DIC Register [7:0]	00800095	N/A	N/A	N/A
	DIC Register [15:8]	00800096	N/A	N/A	N/A
	DIC Register [23:16]	00800097	N/A	N/A	N/A
	DIC Register [31:24]	00800098	N/A	N/A	N/A
Protection & Security	Advanced Sector Protection Register [7:0]	N/A	00000030	N/A	00000030
	Advanced Sector Protection Register [15:8]	N/A	00000031	N/A	00000031

Function	Register type	S25HS-T SEMPER™		S25FS-S	
		Volatile component address (Hex)	Non-volatile component address (Hex)	Volatile component address (Hex)	Non-volatile component address (Hex)
	ASP PPB Lock Register (Persistent Protection Block)	0080009B	N/A	00800040	N/A
	ASP Password Register [7:0]	N/A	00000020	N/A	00000020
	ASP Password Register [15:8]	N/A	00000021	N/A	00000021
	ASP Password Register [23:16]	N/A	00000022	N/A	00000022
	ASP Password Register [31:24]	N/A	00000023	N/A	00000023
	ASP Password Register [39:32]	N/A	00000024	N/A	00000024
	ASP Password Register [47:40]	N/A	00000025	N/A	00000025
	ASP Password Register [55:48]	N/A	00000026	N/A	00000026
	ASP Password Register [63:56]	N/A	00000027	N/A	00000027

9 Order of execution

Some bits in the Configuration register are important to the sector architecture of the device. It is necessary to have these register bits set before any program or erase is done to the device. These bits are:

- TB4KBS (Bit 2) in CFR1N[2]: This bit determines where the parameter sectors are – bottom or top.
- SP4KBS (Bit 6) in CFR1N[6]: This bit determines if the parameter sectors are split between bottom and top overrides (Bit 2) if set. New feature for S25HS-T.
- UNHYSA (Bit 3) in CFR3N[3]: This bit determines if parameter sectors are Uniform or Hybrid Sector architecture .
- D8h_NV (Bit 1) in CFR3N[3]: This bit is RFU in S25HS-T SEMPER™ flash family we only have 256 KB sectors. On the S25FS-S family this bit determines the size of uniform sectors – 64 KB or 256 KB.

If you modify any of these bits after some program operations to the main array, the contents of the array are not guaranteed to still be there. Therefore, as a best practice, you should configure all these bits before accessing the flash array.

Some Status and Configuration register bits can be modified with the same transaction, but some bits have protection interactions with each other. For example, the WRREG_0_1 transaction can write both STR1x and CFRx in one transaction. The LBPROT bits are in STR1x[4:2] and the TLPROT bit is in CFR1x[0]. It is recommended in software to first set the LBPROT bits, then use a separate WRREG_0_1 transaction to set the TLPROT bit to protect the LBPROT bits. However, if the user issues the new LBPROT bit values and TLPROT bit value in the same transaction, it will still work because the device will act upon the current TLPROT value.

After you choose a protection mode for the device – Persistent Protection or Password Protection (the protection modes are discussed later in this document), CFR1N (except TLPROT and QUADIT), CFR2N, CFR3N, and CFR4N are protected. It is important to note that any modification in these registers must be done before choosing the protection mode.

10 Protection

10.1 Legacy bit protection

The Legacy bit protection in the S25HS-T SEMPER™ flash family works the same as S25FS-S SPI devices. The LBPROT bits protect part or all the flash memory depending on the values.

There are two versions of the LBPROT bits. The non-volatile version is in STR1N. The volatile version is in STR1V. When using RDSR1_0_0 (05h) transaction to read, it always reads the STR1V value. If the user wants to read the non-volatile version of the LBPROT bits, the RDARG_C_0 (65h) transaction should be used. The STR1NV value will be returned.

When using the WRREG_0_1 (01h) or WRARG_0_1 (71h) transaction to write LBPROT bits, depending on the LBPROT non-volatile value (in CFR1V), the transaction writes to the LBPROT bits in STR1N or STR1V.

10.2 Advanced sector protection (ASP) protection

There are two ASP modes in the S25HS-T SEMPER™ flash family: Persistent Protection and Password Protection. You can select one by programing Bit 1 or Bit 2 of the ASP register. Note that these two bits are mutually exclusive. If you try to program both bits to 0, the program transaction will result in an error and the previous setting will be retained.

After one of the modes is selected, most of the bits in Configurations registers are protected, as mentioned earlier in this document. So, it is important to program all the Configuration registers first before choosing the protection mode.

If the protection mode has not been selected, the device will function as if in Persistent Protection mode. Infineon strongly recommends that you explicitly select the desired mode so that malicious code cannot later change the protection behavior of the device.

11 Quad peripheral interface (QPI) operations

The S25FS-S family and the S25HS-T SEMPER™ flash family supports QPI mode in which all information, including the instruction code, is transferred in 4-bit width. In the datasheet, this is referenced as 4-4-4 transaction protocol, as the instruction, address, and data are all transferred in 4-bit width.

To operate in QPI mode, you will need to write to the QPI-IT (Bit 6) bit in CFR2x[6].

If you want to try out the QPI mode, it is suggested to use QPI-IT volatile bit in the CFR2V register. This is the volatile version of the QPI-IT bit and the device will reset back to normal mode after reset. Note that once QPI-IT volatile bit is set, the QUADIT bit (Bit 1) in CFR1V[1] will be set automatically. That indicates all I/O signals are used for information transfer, and the WP# and HOLD# functions are disabled. When QPI-IT volatile bit is reset back to 0, the QUADIT Bit in CFR1V[1] will remain 1. The user will need to reset it back to 0 if necessary. After the QPI mode has been tested thoroughly, the user can set QPI-IT bit to permanently run the device in QPI mode if desired.

Although with QPI-IT non-volatile bit set, you can still set QPI-IT volatile bit to 0 so the device reverts to normal mode, this is not a recommended operation because the device would always revert to QPI after reset.

12 Secured silicon region (SSR)

The S25HS-T SEMPER™ flash family provides 1024 bytes of Secured Silicon Region (SSR) area separated from the main flash array. The area is divided into 32, individually lockable, 32-byte aligned regions. (32 x 32 bytes = 1024 bytes)

The SSR is protected by the TLPROT bit in CFR1V[0]. If TLPROT is set, the SSR program transaction will be ignored. No error is reported.

The Region 0 of the SSR (first 32 bytes) is a special region. The first 16 bytes of Region 0 is reserved for Infineon to program in a Random Number that can be used as a unique device identification; for example, serial number. The next 4 bytes are the Lock Bits. Each lock bit controls the corresponding 32 SSR regions, from Region 0 to Region 31. Any attempt to program to the Random Number area will result in a program error. If a SSR region is locked by its lock bit, any attempt to program into the region will result in a program error.

13 Deep power-down mode

S25HS-T and S25FS-S family both support Deep Power-Down modes. The S25HS-T SEMPER™ flash family does not use the Release from Deep Power-Down transaction. Driving CS# low will release the S25HL-T SEMPER™ flash family from the Deep Power-Down mode. Release from deep power down will take the time duration of t_{EXDPD}.

14 DC parameters

Table 14 compares the DC parameters of S25HS-T and S25FS-S. While most parameter differences should not cause performance issues when migrating, it is highly recommended that users carefully review all the parameter differences for any potential impact.

Table 14 DC parameter comparison

Symbol	Parameter operating temperature range –40°C to +85°C	S25HS-T SEMPER™			S25FS-S			Units
		Min	Typ	Max	Min	Typ	Max	
Vcc	Supply voltage	1.7	1.8	2.0	1.7	1.8	2.0	V
Vcc (min)	V_{CC} (minimum operation voltage)	1.7	–	–	1.7	–	–	V
Vcc (cutoff)	V_{CC} (cutoff where reinitialization is needed)	1.5	–	–	1.5	–	–	V
V_{CC} (low)	V_{DD} (low voltage for initialization to occur)	0.7	–	–	0.7	–	–	V
V_{IL}	Input low voltage	-0.15 x Vcc	–	0.35 x Vcc	–0.5	–	0.3 x Vcc	V
V_{IH}	Input high voltage	0.65 x Vcc	–	1.15 x Vcc	0.7 x Vcc	–	Vcc +0.4	V
V_{OL}	Output low voltage	–	–	0.2	–	–	0.2	V
V_{OH}	Output high voltage	Vcc – 0.2	–	–	Vcc – 0.2	–	–	V
I_{LI}	Input leakage current	–	–	±2	–	–	±2	µA
I_{LO}	Output leakage current	–	–	±3	–	–	±2	µA
I_{CC1}	Active power supply current (READ) – Serial SDR 50 MHz	–	10	18	–	10	18	mA
	Active power supply current (READ) – QPI SDR 133 MHz	–	–	–	–	60	64	mA
	Active power supply current (READ) – QPI SDR 166 MHz	–	53	69	–	–	–	mA
	Active power supply current (READ) – QPl DDR 80 MHz	–	–	–	–	70	90	mA
	Active power supply current (READ) – QPI DDR 100 MHz	–	50	68	–	–	–	mA
I_{CC2}	Active power supply current (Page Program)	–	50	55	–	20	25	mA
I_{CC3}	Active power supply current (WRR or WRAR)	–	50	55	–	8	12	mA
I_{CC4}	Active power supply current (SE)	–	50	55	–	20	25	mA
I_{CC5}	Active power supply current (HBE, BE)	–	50	55	–	20	25	mA
I_{SB}	Standby current	–	11	113	–	70	100	µA

DC parameters

Symbol	Parameter operating temperature range –40°C to +85°C	S25HS-T SEMPER™			S25FS-S			Units
		Min	Typ	Max	Min	Typ	Max	
I_{DPD}	Deep power-down current	–	1.3	18	–	8	50	µA
I_{POR}	Power-on reset current	–	–	80	–	–	80	mA

15 Single data rate AC parameters

Table 15 and Table 16 compare the AC parameters of S25HS-T and S25FS-S. While most parameter differences should not cause performance issues when migrating, it is recommended that you carefully review all parameter differences for any potential impact.

Table 15 SDR AC parameter comparison

Symbol	Parameter operating temperature range –40°C to +125°C	S25HS-T SEMPER™			S25FS-S			Units
		Min	Typ	Max	Min	Typ	Max	
f_{CK}	CK clock frequency for READ and 4READ instructions	–	–	50	–	–	50	MHz
	SCK clock frequency for other Read transactions	–	–	166	–	–	133	MHz
P_{CK}	CK clock period	1/ f_{CK}	–	–	1/ f_{CK}	–	–	–
t_{CH}	Clock HIGH time	45% P_{CK}	–	55% P_{CK}	45% P_{CK}	–	55% P_{CK}	ns
t_{CL}	Clock LOW time	45% P_{CK}	–	55% P_{CK}	45% P_{CK}	–	55% P_{CK}	ns
t_{CS}	CS# HIGH time (Read instructions)	10	–	–	10	–	–	ns
	CS# HIGH time (Read instructions when reset features and Quad mode are both enabled and aborted transactions)	20	–	–	N/A	–	–	ns
	CS# HIGH time (Program/erase instructions)	50	–	–	50	–	–	ns
t_{CSS}	CS# active setup time ($f_{CK} \leq$ 50 MHz / $f_{CK} >$ 50 MHz)	5 / 4	–	–	2	–	–	ns
t_{CSH0}	CS# active hold time mode 0 (relative to CK)	3	–	–	3	–	–	ns
t_{CSH3}	CS# active hold time mode 3 (relative to CK)	6	–	–	3	–	–	ns
t_{SU}	Data in setup time ($f_{CK} \leq$ 50 MHz / $f_{CK} >$ 50 MHz)	5 / 2	–	–	2	–	–	ns
t_{HD}	Data in hold time ($f_{CK} \leq$ 50 MHz / $f_{CK} >$ 50 MHz)	5 / 2	–	–	3	–	–	ns
t_V	Clock LOW to output valid (30 pF loading)	2	–	8	–	–	8	ns
	Clock LOW to output valid (15 pF loading)	2	–	6	–	–	6	ns
t_{HO}	Output hold time	1.5	–	–	1	–	–	ns
t_{DIS}	CS# inactive to output disable time	–	–	8	–	–	8	ns
	CS# inactive to output disable time	–	–	20	–	–	–	ns

Single data rate AC parameters

Symbol	Parameter operating temperature range –40°C to +125°C	S25HS-T SEMPER™			S25FS-S			Units
		Min	Typ	Max	Min	Typ	Max	
	(When reset and Quad mode enabled)							
t_{DP}	CS# HIGH to deep power-down mode	10	–	–	–	–	3	µs
t_{RES}	Release from deep power-down mode to wakeup	–	–	430	–	–	30	µs
t_{PU} /t_{RPH}	Reset time	–	–	500	–	–	35	µs

Table 16 DDR AC parameter comparison

Symbol	Parameter operating temperature range –40°C to +125°C	S25HS-T SEMPER™			S25FS-S			Units
		Min	Typ	Max	Min	Typ	Max	
f_{CK}	CK clock frequency	–	–	102	–	–	80	MHz
P_{CK}	CK clock period	1/ f_{CK}	–	–	1/ f_{CK}	–	–	–
t_{CH}	Clock HIGH time	45% P_{CK}	–	55% P_{CK}	45% P_{CK}	–	55% P_{CK}	ns
t_{CL}	Clock LOW time	45% P_{CK}	–	55% P_{CK}	45% P_{CK}	–	55% P_{CK}	ns
t_{CS}	CS# HIGH time (Read instructions)	10	–	–	10	–	–	ns
	CS# HIGH time (Read instructions when reset features and Quad mode are both enabled and aborted transactions)	20	–	–	N/A	–	–	ns
	CS# HIGH time (Program/erase instructions)	50	–	–	50	–	–	ns
t_{CSS}	CS# active setup time (f_{CK} ≤ 50 MHz / f_{CK} > 50 MHz)	5 / 4	–	–	2	–	–	ns
t_{CSH0}	CS# active hold time mode 0 (relative to CK)	4	–	–	3	–	–	ns
t_{SU}	Data in setup time (f_{CK} ≤ 50 MHz / f_{CK} > 50 MHz)	5 / 2	–	–	1.5	–	–	ns
t_{HD}	Data in hold time (f_{CK} ≤ 50 MHz / f_{CK} > 50 MHz)	5 / 1.2	–	–	1.5	–	–	ns
t_V	Clock LOW to output valid (15 pF loading)	2	–	6	–	–	6	ns
t_{HO}	Output hold time	1.5	–	–	1	–	–	ns
t_{DIS}	CS# inactive to output disable time	–	–	8	–	–	6	ns
	CS# inactive to output disable time	–	–	20	–	–	–	–

Single data rate AC parameters

Symbol	Parameter operating temperature range –40°C to +125°C	S25HS-T SEMPER™			S25FS-S			Units
		Min	Typ	Max	Min	Typ	Max	
	(When reset and Quad mode enabled)							

16 Embedded algorithm performance

Table 17 compares the embedded algorithm performance parameters of S25HS-T and S25FS-S. While most parameter differences should not cause performance issues when migrating, it is recommended that you carefully review all parameter differences for any potential impact.

Table 17 Embedded algorithm performance parameter comparison

Symbol	Parameter operating temperature range –40°C to +125°C	S25HS-T			S25FS-S			Units
		Min	Typ	Max	Min	Typ	Max	
t_W	Non-volatile Register Write Time	–	44	357	–	240	750	ms
t_{PP}	Page Programming (256 bytes)	–	480	1700	–	360	2000	µs
	Page Programming (512 bytes)	–	570	1700	–	475	2000	µs
t_{SE}	Sector Erase Time (4-KB parameter sectors)	–	42	335	–	240	720	ms
	Sector Erase Time (256-KB Long Retention sectors)	–	773	2677	–	930	2900	ms
	Sector Erase Time (256-KB High Endurance sectors)	–	773	5869	–	–	–	ms
t_{CE}	Bulk Erase Time (512 Mb)	–	201	696	–	220	720	s
	Bulk Erase Time (1Gb)	–	398	1381	–	440	1440	s

17 Summary

This guide is intended as a supplement to the S25HS-T datasheet to further help you design your low-level drivers and application software when migrating to 45-nm S25HS-T Quad SPI SEMPER™ flash Quad SPI from 65-nm S25FS-S Quad SPI flash.

References

SPI NOR flash documents

[1] S25HS-T SEMPER™ flash family datasheet

- 002-12345 – S25HS256T / S25HS512T / S25HS01GT 256Mb / 512Mb / 1Gb SEMPER™ Flash, Quad SPI, 1.8V/ 3.0V

[2] S25FS-S family datasheet

- **002-00488** - S25FS512S, 512 Mb (64 MB) FS-S Flash, SPI Multi-I/O, 1.8 V

[3] Endurance flex application note

- 002-18481 - AN218481 - Endurance flex explained – Wear-leveling techniques and usage in Infineon SEMPER™ flash devices

Revision history

Document version	Date of release	Description of changes
**	2018-03-26	New application note
*A	2019-05-26	Update DC and AC Specifications
*B	2019-06-17	Updated Icc Deep Power down spec
*C	2021-02-25	Migrated to Infineon template
*D	2022-07-20	Updated with the latest information from S25HS-T datasheet

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