Automotive Power Management System Thermal Design

About this document

Scope and purpose

AN218263 explains the important points and provides examples for effective heat dissipation of a power management system with Cypress' Power management IC (PMICs).

Associated Part Family

S6BP20xA, **S6BP401A**, **S6BP50xA**

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1 Introduction

As more electronic components are used in vehicles, power consumption problem rises. Also, as the shape of printed circuit board (PCB) becomes increasingly complex and the available surface area continues to shrink, thermal considerations are becoming more important. Although Cypress' PMICs generally have high efficiency and low self-loss, heat generation due to self-loss is still a possibility. This application note explains how to examine heat generation and develop countermeasures for power supply design using Cypress' PMICs.

2 Heat generation and dissipation

Electronic components generate heat due to power consumed in order to function properly, and their temperature depends on conditions of the environment in which heat dissipates. Generally, heat dissipation is the process of heat escaping into its surroundings. A large difference in temperature between electronic components and their surroundings and a large surface area in contact with air are critical factors for high-efficiency heat dissipation.

Power systems with Cypress' PMICs are mainly composed of DC/DC converters, which have a higher conversion efficiency and lower power loss than an LDO. In recent years, as electronic parts are getting smaller, it is becoming harder to secure the surface area in contact with air that is necessary to achieve effective heat dissipation. Therefore, packages with exposed pad (EP) for substrate thermal bonding are becoming more common so that even small electronic parts can effectively dissipate heat. In general, large surface areas of the PCBs next to the enclosure and the method of radiating heat from EP are used. Cypress' automotive on-board PMICs have compact packages with EP, enabling efficient heat dissipation. **Table 1** shows some of Cypress' PMICs.

Table 1 PMICs lineup

Part Number	Main Applications	Package	Power Supply	Output Voltage / Supply Current
S6BP201A	Cluster, Body control, Advanced Driver Assistance System (ADAS)	16-pin TSSOP (plus Exposed Pad) 4.4 mm × 5.0 mm (Mold size)	1-ch Buck-boost	5.0 V / 1.0 A
S6BP202A				5.0 V / 2.4 A
S6BP203A				3.3 V / 2.4 A
S6BP401A	ADAS	40-pin QFN (plus Exposed Pad) 6.0 mm × 6.0 mm	4-ch Buck + 2-ch LDO	1.0 V~3.4 V / 0.2 A~3.0 A
S6BP501A	Cluster	32-pin QFN (plus Exposed Pad) 5.0 mm × 5.0 mm	2-ch Buck + 1-ch Boost	1.0 V~5.2 V / 1.3 A~1.4 A
S6BP502A				1.0 V~5.2 V / 1.3 A~2.0 A

For a detailed specification of each PMIC, see the datasheets (**S6BP201A**, **S6BP202A**, **S6BP203A**, **S6BP401A**, **S6BP501A**, **S6BP502A**).

3 Thermal design

Thermal design must ensure that the junction temperature does not exceed the rated temperature in power components (switching FET, coil) which are the main heat sources. A good understanding of the amount of heat dissipation of each part is crucial to thermal design. It is necessary to consider the self-generated heat of LDO and PMIC with built-in switching FETs.

Figure 1 shows a typical thermal design flow.

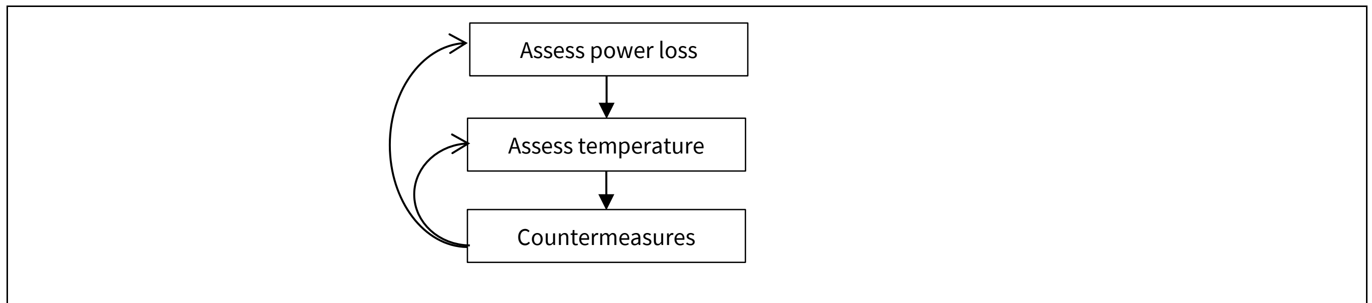


Figure 1 DC/DC converter thermal design

3.1 Power loss assessment

The easiest way to assess power loss is using the conversion efficiency data in the datasheet. The assessment method varies depending on the specific configuration of each PMIC.

3.1.1 Single-channel DC/DC converter with built-in FET (S6BP201A, S6BP202A, S6BP203A)

In this case, S6BP202A is used as an example for explanation. Schematic and conversion efficiency (VIN=12V) are shown in **Figure 2**.

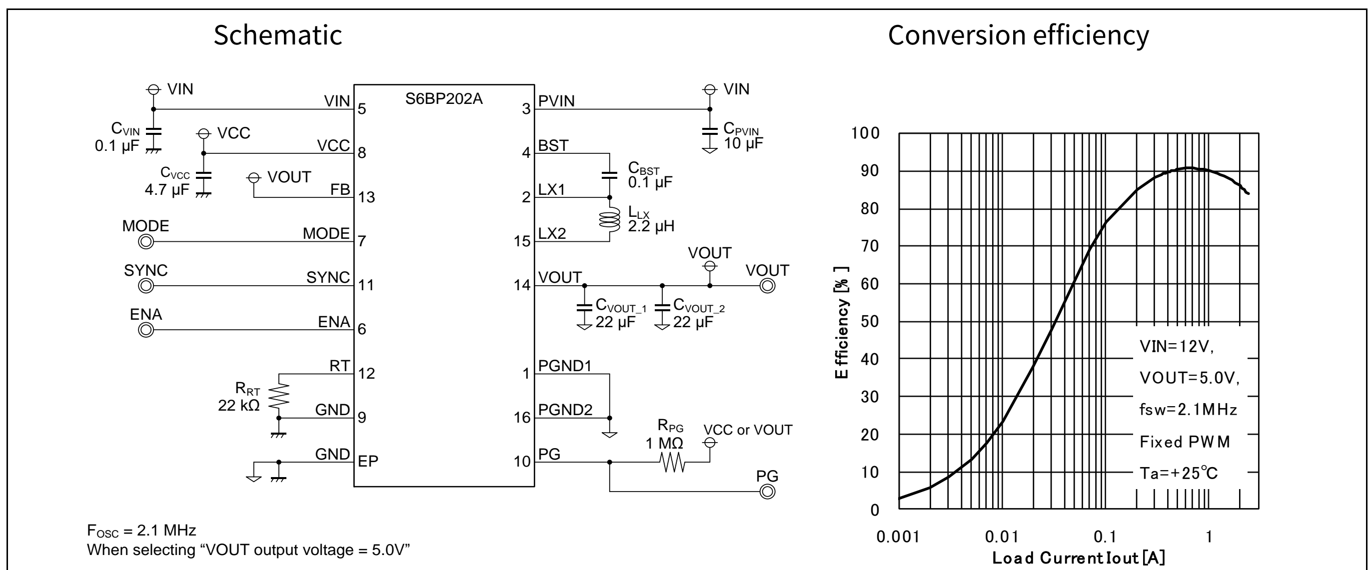


Figure 2 S6BP202A schematic, conversion efficiency

Refer to **S6BP202A** datasheet for detailed parts information.

Here, the main components that generate loss are S6BP202A with the built-in FET and coil (L_{LX}).

In this circuit, a ceramic capacitor is used. Ceramic capacitors have small equivalent series resistance (ESR) characteristics that result in very low loss, which can be ignored in this case. **Figure 3** shows a simplified diagram of power losses.

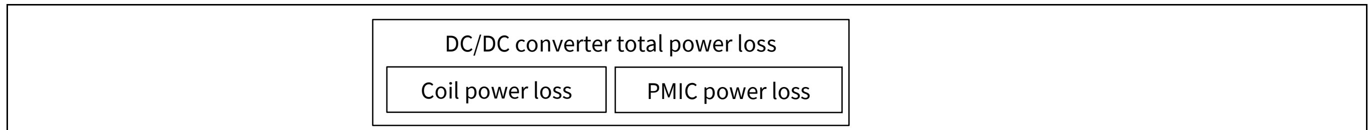


Figure 3 Relationship among power losses

Use the approach shown in **Figure 4** and **Equation 1** to calculate the PMIC power loss.

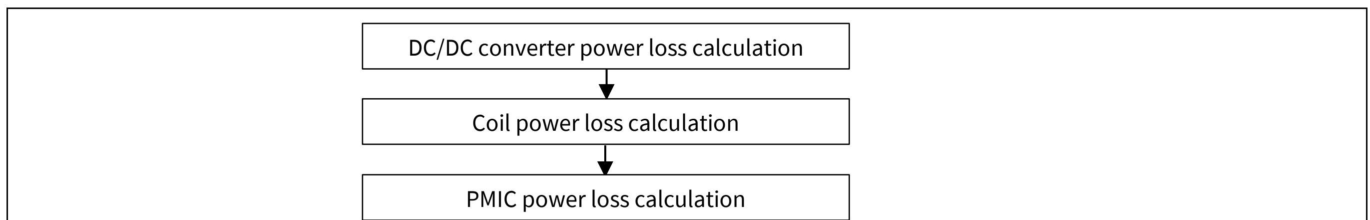


Figure 4 PMIC power loss calculation flow

Equation 1

$$P_{Loss} = V_{OUT} \times I_{OUT} \times (\frac{1}{\eta} - 1),$$

$$P_{Loss_L} = RDC \times I_{OUT}^2,$$

$$P_{Loss_PMIC} = P_{Loss} - P_{Loss_L}$$

Where:

P_{Loss_PMIC}: S6BP202A power loss (W)

P_{Loss}: DC/DC converter total power loss (W)

P_{Loss_L}: Coil power loss (W)

η_x: DC/DC converter's efficiency graph reading value

V_{OUT}: Output voltage (V)

I_{OUT}: Max load current (A)

RDC: Coil equivalent series resistance (Ω)

The following example shows the calculation of power loss for the **S6BP202A Evaluation Kit** (EVK). The EVK is used in the following conditions: V_{IN}=12 V, V_{OUT}=5 V, I_{OUT}=1 A, fsw=2.1 MHz, fixed PWM mode

$$P_{Loss} = 5V \times 1A \times (\frac{1}{0.9} - 1) = 0.556W$$

$$P_{Loss_L} = 14.6m\Omega \times 1A^2 = 0.015W$$

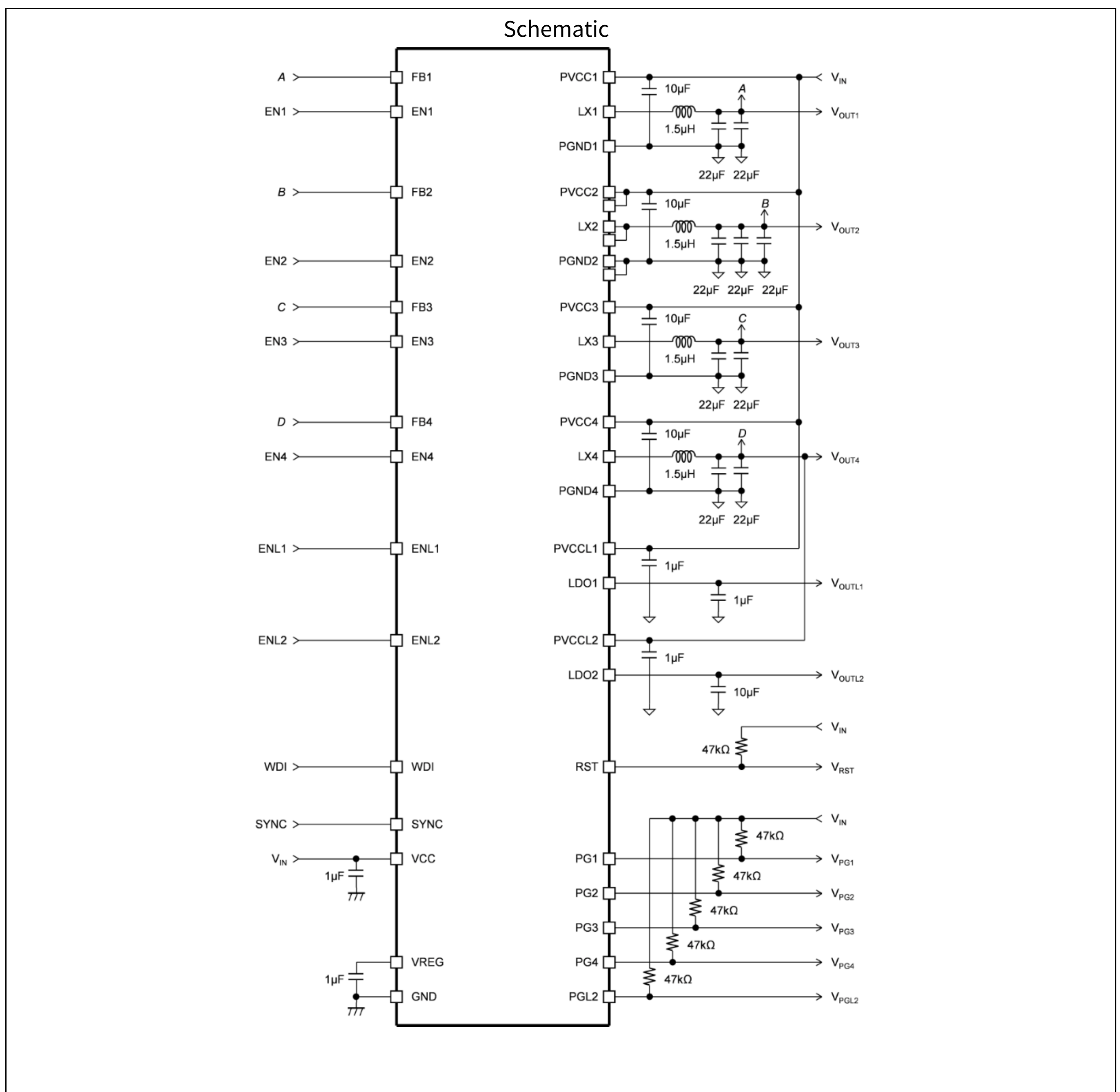
$$P_{Loss_PMIC} = 0.556W - 0.015W = 0.54W$$

Changing the coil leads to change in conversion efficiency. However, this does not significantly affect the PMIC loss. Therefore, the above conversion efficiency graph can be used.

The conversion efficiency of the EVK is measured and used as a reference value to evaluate other conditions.

3.1.2 Multi-channel DC/DC converter with built-in FET (S6BP401A)

Figure 5 shows the schematic and conversion efficiency (VIN=5 V) of S6BP401A.



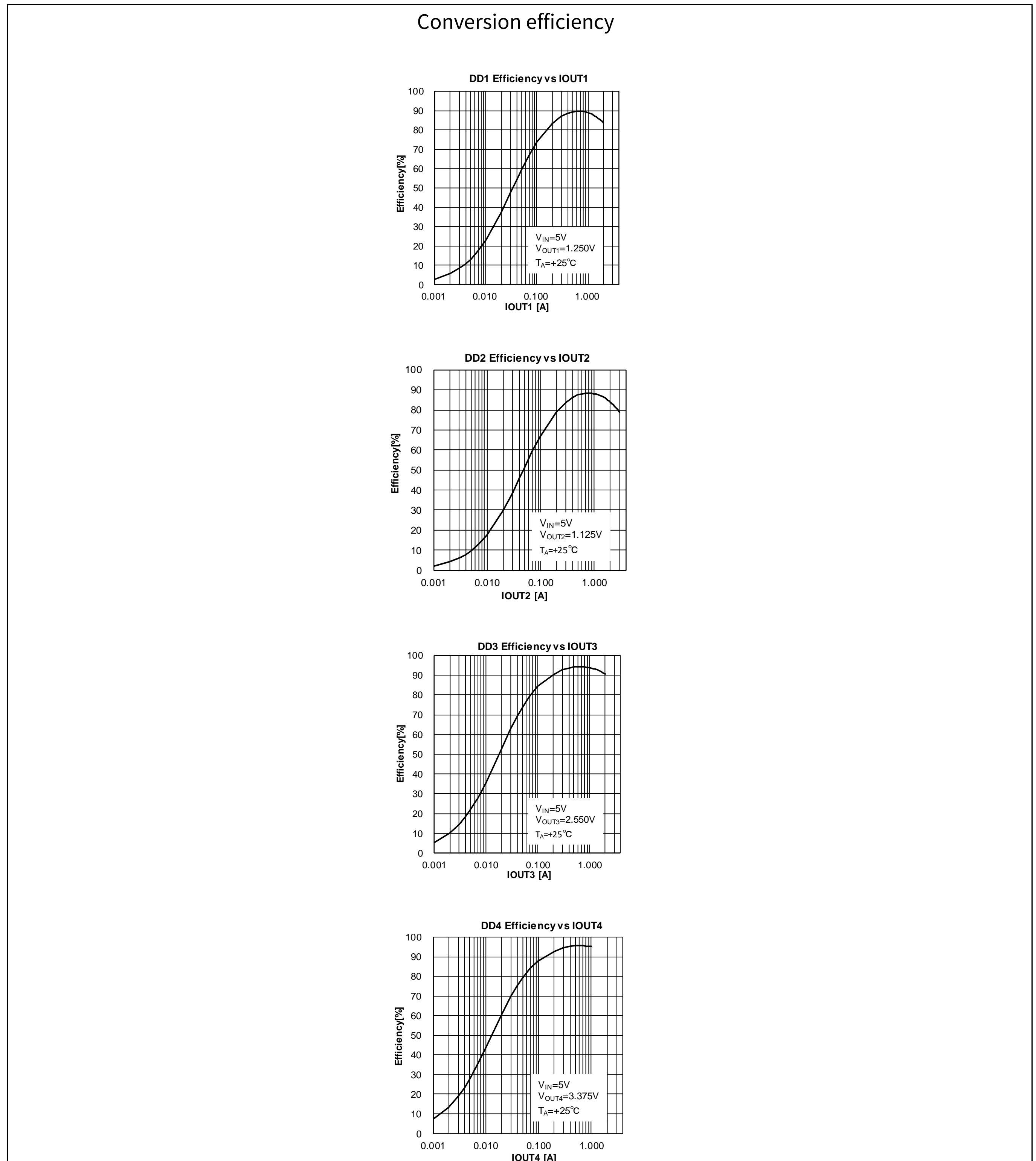


Figure 5 S6BP401A schematic, conversion efficiency

DD1, DD2, DD3, and DD4 are channel names of the DC/DC converter. See the **S6BP401A** datasheet for detailed parts information.

Here, main components that generate loss are S6BP401A with built-in FET and LDO, and coils (L1, L2, L3, L3). Calculation of power loss of this PMIC requires calculation of power losses of four DC/DC converters and two LDOs. **Figure 6** shows each power loss.

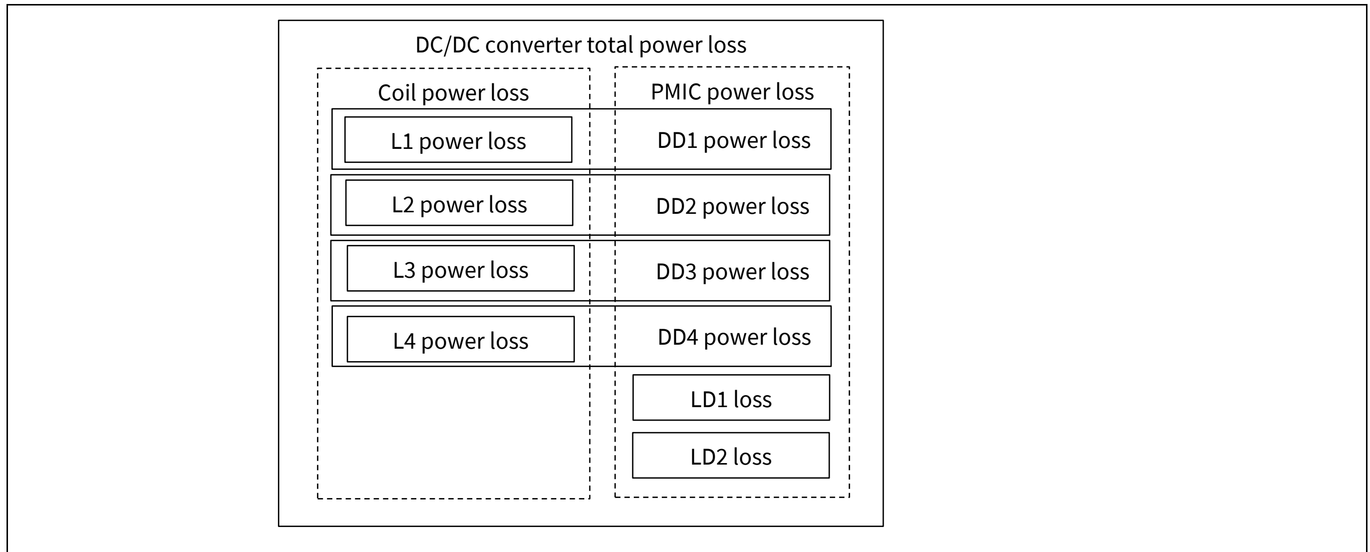


Figure 6 Relationship among power losses

Figure 7 shows the flow for calculating the PMIC power loss.

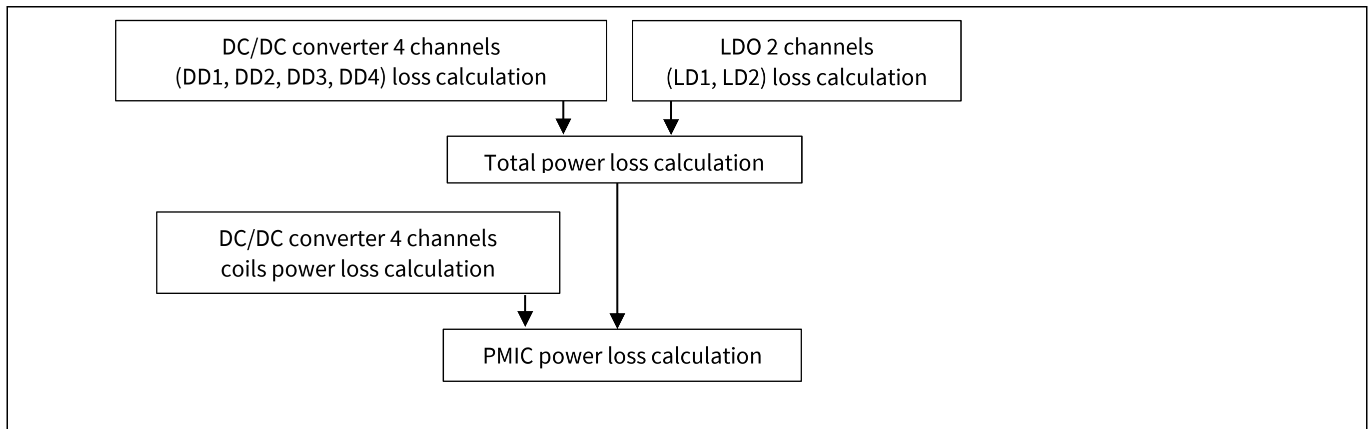


Figure 7 PMIC power loss calculation flow

DD1, DD2, DD3, and DD4 are the channel names of DC/DC converter. LD1 and LD2 are the channels names of built-in LDOs.

Equation 2

$$P_{Loss_DDx} = V_{OUTx} \times I_{OUTx} \times \left(\frac{1}{\eta x} - 1\right)$$

$$P_{Loss_LDx} = (V_{INLx} - V_{OUTLx}) \times I_{OUTLx}$$

$$P_{Loss} = P_{Loss_DD1} + P_{Loss_DD2} + P_{Loss_DD3} + P_{Loss_DD4} + P_{Loss_LD1} + P_{Loss_LD2}$$

$$P_{Loss_Lx} = RDC_x \times I_{OUTx}{}^2$$

$$P_{Loss_L} = P_{Loss_L1} + P_{Loss_L2} + P_{Loss_L3} + P_{Loss_L4}$$

$$P_{Loss_PMIC} = P_{Loss} - P_{Loss_L}$$

Where:

P_{Loss_PMIC}: S6BP401A power loss (W)

P_{Loss}: DC/DC converter, LDO total power loss (W)

P_{Loss_DDx} (here x=1,2,3 or 4): each DC/DC converter power loss (W)

P_{Loss_LDx} (here x=1or 2): each LDO loss (W)

P_{Loss_L}: Coils total power loss (W)

P_{Loss_Lx} (here x=1,2,3 or 4): each DC/DC converter coil power loss (W)

η_x (here x=1,2,3 or 4): each DC/DC converter efficiency graph reading value

V_{OUTx} (here x=1,2,3 or 4): each DC/DC converter output voltage (V)

I_{OUTx} (here x=1,2,3 or 4): each DC/DC converter max load current(A)

RDC_x (here x=1,2,3 or 4): each DC/DC converter coils equivalent series resistance (Ω)

V_{INLx} (here x=1 or 2): each LDO power-supply voltage (V)

V_{OUTLx} (here x=1 or 2): each LDO output voltage (V)

I_{OUTLx} (here x=1 or 2): each LDO max load current (A)

The following examples shows the calculation for **S6BP401A Evaluation Kit** (EVK).

Condition: V_{IN}=5 V, V_{OUT1}=1.250 V, I_{OUT1}=1 A, V_{OUT2}=1.125 V, I_{OUT2}=1 A, V_{OUT3}=2.550 V, I_{OUT3}=1 A, V_{OUT4}=3.375 V, I_{OUT4}=0.5 A, V_{OUTL1}=3.325 V, I_{OUTL1}=0.05 A, V_{OUTL2}=2.8 V, I_{OUTL2}=0.1 A

$$P_{Loss_DD1} = 1.250V \times 1A \times (\frac{1}{0.89} - 1) = 0.154W \quad , \quad P_{Loss_L1} = 13m\Omega \times 1A^2 = 0.013W$$

$$P_{Loss_DD2} = 1.125V \times 1A \times (\frac{1}{0.88} - 1) = 0.153W \quad , \quad P_{Loss_L2} = 13m\Omega \times 1A^2 = 0.013W$$

$$P_{Loss_DD3} = 2.550V \times 1A \times (\frac{1}{0.93} - 1) = 0.192W \quad , \quad P_{Loss_L3} = 13m\Omega \times 1A^2 = 0.013W$$

$$P_{Loss_DD2} = 3.375V \times 0.5A \times (\frac{1}{0.95} - 1) = 0.089W \quad , \quad P_{Loss_L4} = 13m\Omega \times 0.5A^2 = 0.003W$$

$$P_{Loss_LD1} = (5V - 3.325V) \times 0.05A = 0.084W$$

$$P_{Loss_LD1} = (5V - 2.800V) \times 0.1A = 0.22W$$

$$P_{Loss} = 0.154W + 0.153W + 0.192W + 0.089W + 0.084W + 0.22W = 0.872W$$

$$P_{Loss_L} = 0.013W + 0.013W + 0.013W + 0.003W = 0.042W$$

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$$P_{Loss_PMIC} = 0.872W + 0.042W = 0.83W$$

Conversion efficiency of EVK is measured and used as the reference value for evaluation of conditions different from the conversion efficiency graph.

3.1.3 Two-stage DC/DC converter (S6BP501A, S6BP502A)

Figure 8 shows the schematic and conversion efficiency (VIN=12V) of S6BP502A.

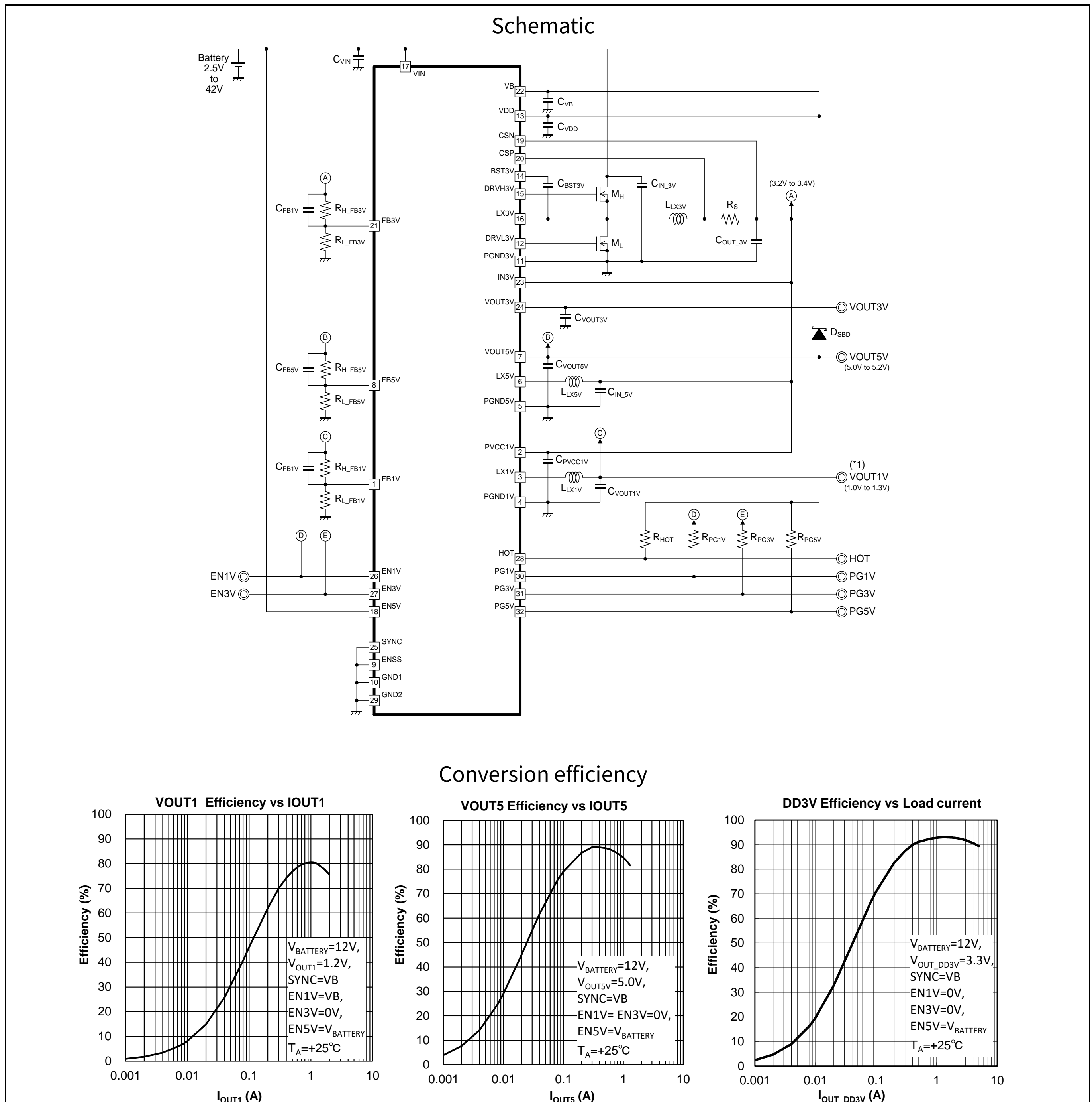

Figure 8 S6BP502A schematic, conversion efficiency

Refer to **S6BP501A, S6BP502A datasheet** for detailed parts information.

The following three components are the main sources for loss generation. The primary source is the external switching FETs (M_H, M_L) of the DC/DC converter (DD3V). The secondary source is the switching FETs of DC/DC converter channel (DD1V, DD5V) and S6BP502A with built-in output load switch (SW3V) for VOUT3. The tertiary source is the DC/DC converter's coils (L1, L2, L3). Because DD1V and DD5V are generated from DD3V, which is the primary DC/DC conversion channel, the power relationship becomes complicated. **Figure 9** shows the diagram of each power loss.

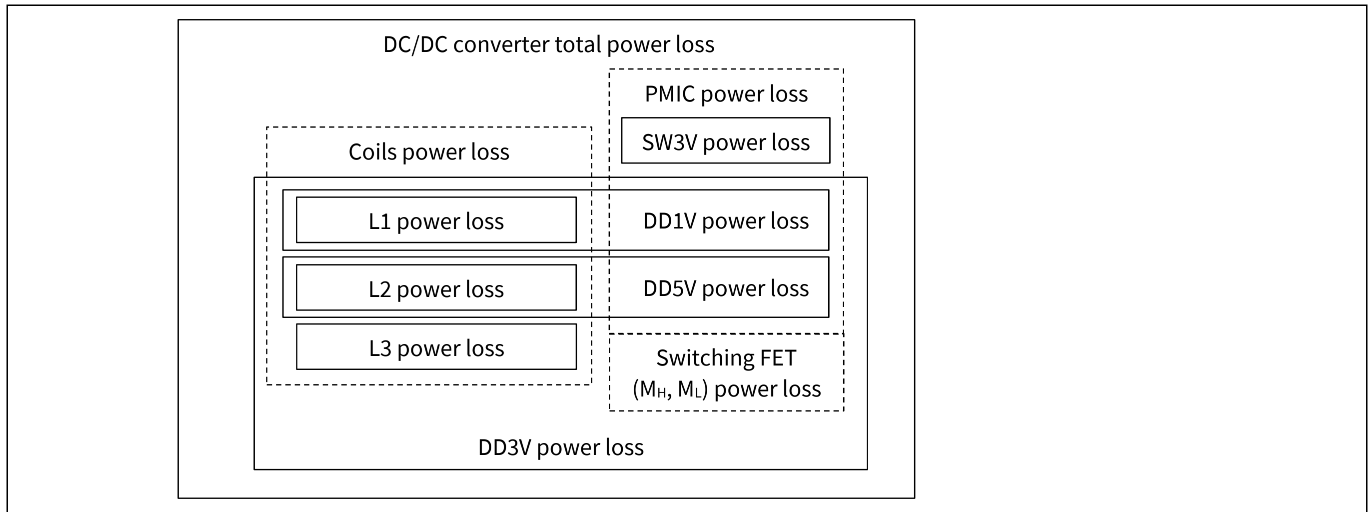

Figure 9 Relationship among power losses

To calculate the power loss of this PMIC, you need to calculate the power loss of DD1V, DD5V and load switch. Because the switching FET is external at DD3V channel, its power loss is not included when calculating PMIC's power loss. However, when calculating DD1V and DD5V conversion efficiency, it is necessary to consider the DD3V conversion efficiency. The PMIC's power loss can be calculated using flow and equation shown in **Figure 10**.

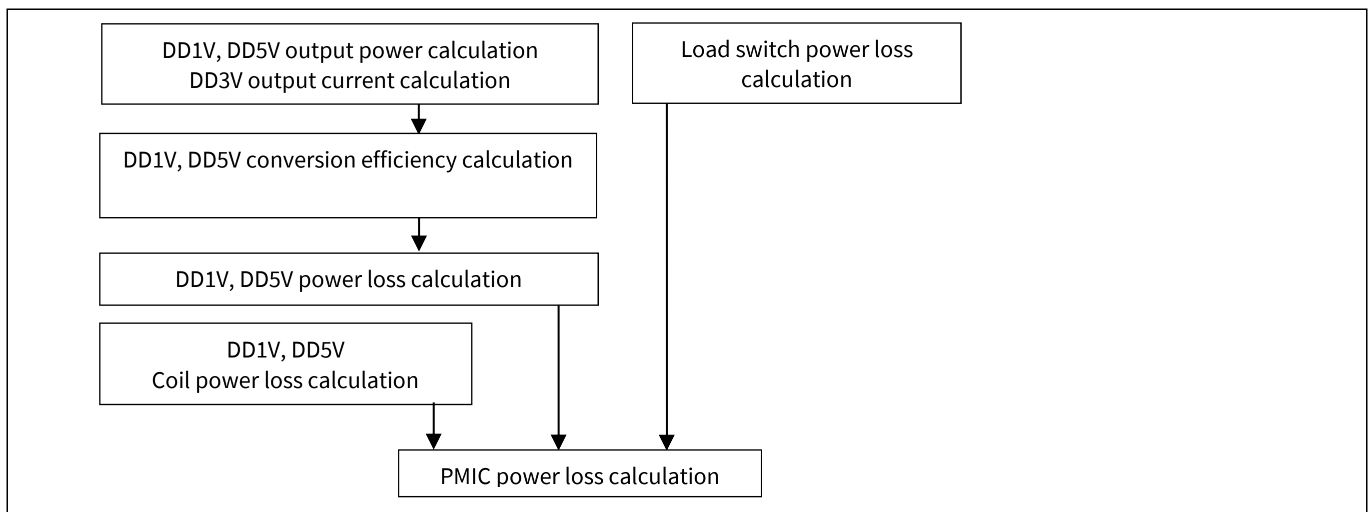

Figure 10 PMIC power loss calculation low

DD1V, DD3V, DD5V are channel names for DC/DC converter. SW3V is internal load switch.

Equation 3

$P_{OUT1} = V_{OUT1} \times I_{OUT1}$,

$P_{OUT5} = V_{OUT5} \times I_{OUT5}$,

$I_{OUT_DD3V} = \frac{P_{OUT1}}{V_{OUT_DD3V}}$ or $I_{OUT_DD3V} = \frac{P_{OUT5}}{V_{OUT_DD3V}}$,

$\eta_1 = \frac{\eta_{1graph}}{\eta_{3graph}}$, $\eta_5 = \frac{\eta_{5graph}}{\eta_{3graph}}$,

$P_{Loss_DDx} = V_{OUTx} \times I_{OUTx} \times (\frac{1}{\eta x} - 1)$

$P_{Loss_L1} = RDC_1 \times I_{OUT1}^2$,

$P_{Loss_L5} = RDC_5 \times (\frac{V_{OUT5} \times I_{OUT5}}{V_{OUT_DD3V}})^2$,

$P_{Loss_SW3V} = R_{ON_SW3V} \times I_{OUT3}^2$,

$P_{Loss_PMIC} = P_{Loss_DD5V} - P_{Loss_L5} + P_{Loss_DD1V} - P_{Loss_L1} + P_{Loss_SW3V}$

Where:

P_{Loss_PMIC}: S6BP502A power loss (W)

P_{OUT1}: DD1V output power (W)

P_{OUT5}: DD5V output power (W)

P_{OUT_DD3V}: DD3V output power (W)

V_{OUT_DD3V}: DD3V output voltage (V)

V_{OUT1}: DD1V output voltage (V)

V_{OUT5}: DD5V output voltage (V)

I_{OUT1}: DD1V output current (A)

I_{OUT5}: DD5V output current (A)

I_{OUT3}: VOUT3V output current (A)

η_{3graph}: DD3V conversion efficiency graph reading value

η_{1gragh}: VOUT1 conversion efficiency graph reading value

η_1: DD1V calculated power conversion efficiency

η_{5gragh}: VOUT5 conversion efficiency graph reading value

η_5: DD5V calculated power conversion efficiency

P_{Loss_DDx} (x=1 or 5): DD1V, DD5V DC/DC converter power loss(W)

P_{Loss_Lx} (x=1 or 5): DD1V, DD5V DC/DC converter coil power loss (W)

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P_{Loss_SW3V}: SW3V conduction loss (W)

RDC_x (x=1 or 5): DD1V, DD5V DC/DC converter coils equivalent series resistance (Ω)

R_{ON_SW3V}: SW3V ON resistance (Ω) =58 mΩ (typ.)

The following example shows the calculation for **S6BP502A Evaluation Kit** (EVK).

Condition: V_{IN}=12 V, V_{OUT1}=1.2 V, I_{OUT1}=2 A, V_{OUT5}=5 V, I_{OUT2}=1.3 A, V_{OUT3}=3.3 V, I_{OUT3}=1.9 A

$$P_{OUT1} = V_{OUT1} \times I_{OUT1} = 1.2V \times 2A = 2.4W,$$

$$I_{OUT_DD3V} = \frac{P_{OUT1}}{V_{OUT_DD3V}} = \frac{2.4W}{3.3V} = 0.72A$$

From 'DD3V Efficiency vs Load current' graph, DD3V conversion efficiency η_{3graph} at I_{OUT_DD3V}=0.72 A is=92%,

From 'VOUT1 Efficiency vs IOUT1' graph, DD1V conversion efficiency η_{1graph} at I_{OUT1}=2 A is 75%,

$$\eta_1 = \frac{\eta_{1graph}}{\eta_{3graph}} = \frac{75\%}{92\%} = 82\%,$$

$$P_{Loss_DD1} = V_{OUT1} \times I_{OUT1} \times (\frac{1}{\eta_1} - 1) = 1.2V \times 2A \times (\frac{1}{82\%} - 1) = 0.527W,$$

$$P_{Loss_L1} = RDC_1 \times I_{OUT1}^2 = 13m\Omega \times 2A^2 = 0.052W,$$

$$P_{OUT5} = V_{OUT5} \times I_{OUT5} = 5V \times 1.3A = 6.5W,$$

$$I_{OUT_DD3V} = \frac{P_{OUT5}}{V_{OUT_DD3V}} = \frac{6.5W}{3.3V} = 1.9A,$$

From 'DD3V Efficiency vs Load current' graph, DD3V conversion efficiency η_{3graph} at I_{OUT_DD3V}=1.9A is 93%,

From 'VOUT5 Efficiency vs IOUT5' graph, DD5V conversion efficiency η_{5graph} at I_{OUT5}=1.3A is 82%,

$$\eta_5 = \frac{\eta_{5graph}}{\eta_{3graph}} = \frac{82\%}{93\%} = 88\%,$$

$$P_{Loss_DD5} = V_{OUT5} \times I_{OUT5} \times (\frac{1}{\eta_5} - 1) = 5V \times 1.3A \times (\frac{1}{88\%} - 1) = 0.886W,$$

$$P_{Loss_L5} = RDC_5 \times (\frac{V_{OUT5} \times I_{OUT5}}{V_{OUT_DD3V}})^2 = 13m\Omega \times (\frac{5V \times 1.3A}{3.3V})^2 = 0.050W,$$

$$P_{Loss_SW3V} = R_{ON_SW3V} \times I_{OUT3}^2 = 58m\Omega \times 1.9A^2 = 0.209W,$$

$$P_{Loss_PMIC} = P_{Loss_DD5V} - P_{Loss_L5} + P_{Loss_DD1V} - P_{Loss_L1} + P_{Loss_SW3V}$$
$$= 0.886W - 0.050W + 0.527W - 0.052W + 0.209W = 1.52W$$

Conversion efficiency of EVK is measured and used as the reference value for evaluation of conditions different from the conversion efficiency graph.

3.2 Semiconductor component junction temperature

The temperature of semiconductor components such as PMIC is evaluated as the junction temperature. This section explains how to estimate the temperature of semiconductor components. It is common to use a thermal resistance model for this estimation. **Figure 11** shows the general thermal model.

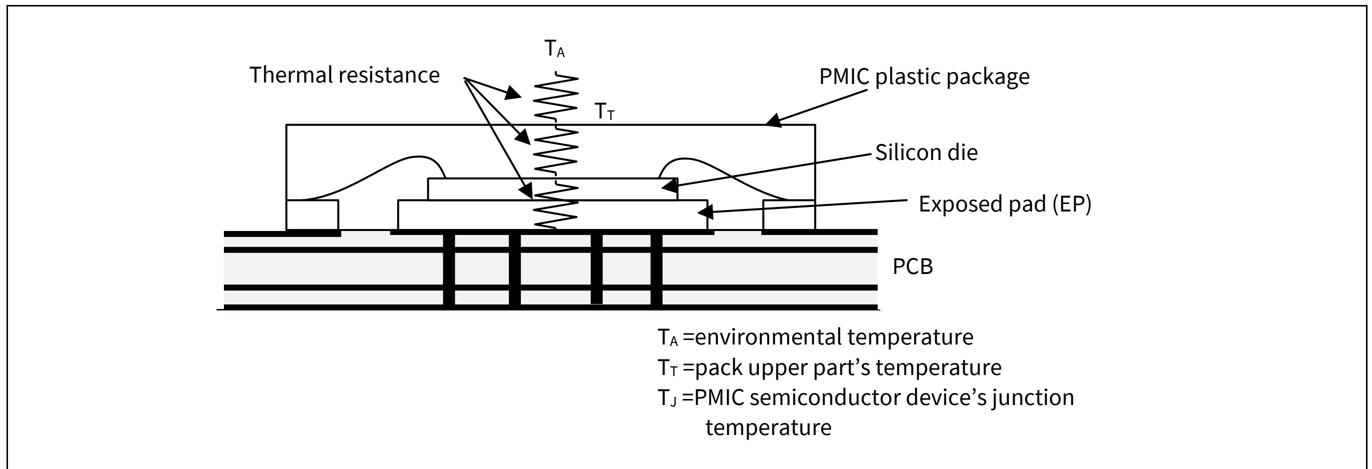

Figure 11 Thermal model

Calculate the junction temperature of the semiconductor device using **Equation 4** to confirm that the junction temperature does not exceed the rated value.

Equation 4

$$T_J = P_{Loss_PMIC} \times \theta_{JA} + T_A$$

Where:

T_J: PMIC junction temperature (°C)

T_A: environmental temperature (°C)

P_{Loss_PMIC}: PMIC power loss (W)

θ_{JA}: Thermal resistance from PMIC junction to environmental temperature (°C/W)

*Please refer to application note **AN201006** for detailed thermal resistance and temperature information.

Use **Equation 5** to calculate thermal resistance θ_{JA} if it is not specified in datasheet.

Equation 5

$$\theta_{JA} = \frac{T_{JMAX} - T_A}{P_D}$$

Where:

θ_{JA}: PMIC thermal resistance of junction to ambient temperature (°C/W)

T_{JMAX}: PMIC maximum junction temperature (°C)

T_A: Ambient temperature at which derating begins (°C) normally +25°C

P_D: PMIC allowed loss (W)

Below shows a calculation example of thermal resistance and junction temperature of **S6BP502A Evaluation Kit** (EVK).

Condition: V_{IN}=12 V, V_{OUT1}=1.2 V, I_{OUT1}=2 A, V_{OUT5}=5 V, I_{OUT2}=1.3 A, V_{OUT3}=3.3 V, I_{OUT3}=1.9 A

$$\theta_{JA} = \frac{T_{JMAX} - T_A}{P_D} = \frac{+150°\text{C} - 25°\text{C}}{4.28W} = 29°\text{C/W}$$

Under this condition, PMIC power loss is P_{LOSS_PMIC}=1.52 W (From **Equation 3** calculation example)

$$T_J = P_{Loss_PMIC} \times \theta_{JA} + T_A = 1.52W \times 29°\text{C/W} + 25°\text{C} = +69°\text{C}$$

This equation to calculate junction temperature can also be used to evaluate the heat generation of the external switching FET. When external switching FETs are selected for DD3V of S6BP501A,S6BP502, use the calculation formula described in 'DC/DC converter (DD3V) component selection' and 'switching FET (SWFET)' in application note **AN99435** for power loss calculation. To calculate the junction temperature, substitute the loss value and the thermal resistance value described in the switching FET data sheet.

Approximate heat can be analyzed by the method described in this section, but it is recommended to make a final judgment by temperature measurement.

3.3 Countermeasures

Thermal countermeasures are important when dealing with the board's heat dissipation. Especially for PMIC and switching FETs, thermal countermeasures are necessary. This section describes PCB layout for efficient heat dissipation.

3.3.1 Heat dissipation path on PCB

Most heat generated by the PMIC dissipates from the EP on the back of the package. **Figure 12** shows a typical flow as PMIC EP→ PCB via → PCB surface Cu plane → ambient air.

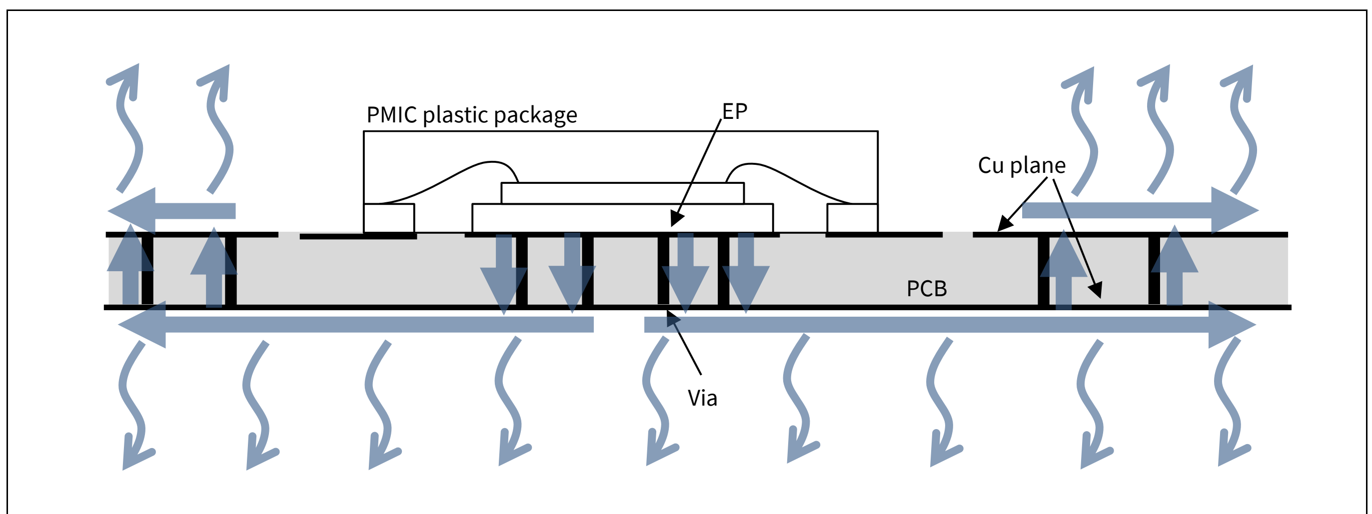

Figure 12 PCB heat dissipation flow (2-layer PCB)

Table 2 shows thermal conductivity and thermal resistance of epoxy resin containing FR4, which is often used as the PCB base material, and copper (Cu), which is often used as the PCB conductor.

Table 2 Thermal conductivity and thermal resistance

Item	Thermal conductivity (W/(m ×°C))	Thermal resistance (°C/W)	Note
Epoxy resin (base)	0.21	3000	2cm × 2cm square, horizontal heat conduction on 1.6-mm thick substrate
Cu (wiring)	398	70	2cm × 2cm square, horizontal heat conduction on 35-µm thick Cu plane

Table 3 shows the approximate value of each thermal resistance for heat dissipation path.

Table 3 Thermal resistances between PCB and ambient Air

Item	Thermal resistance (°C/W)	Note
Cu plane	70	2 cm × 2 cm square, horizontal heat conduction on 35-µm thick Cu plane
Via	0.025	Φ = 0.3mm / Cu plating thickness of 15-µm substrate thickness of 1.6 mm
Convective heat conduction	300	2 cm × 2 cm square / convection heat conduction into ambient air from substrate surface

From **Table 2** and **Table 3**, it is clear that heat conduction is mainly done through Cu, and thermal resistances of substrate and ambient air are important. This shows that plane connection by via, reducing Cu plane gap, and increasing the substrate effective area for heat dissipation are main methods for effective heat dissipation.

3.3.2 PCB layout for effective heat dissipation

EP foot pattern and ground plane are thermally coupled by vias. For a multilayer board with four or more layers, the inner layer is often used as the ground layer, thus it is actively used as a heat conduction route.

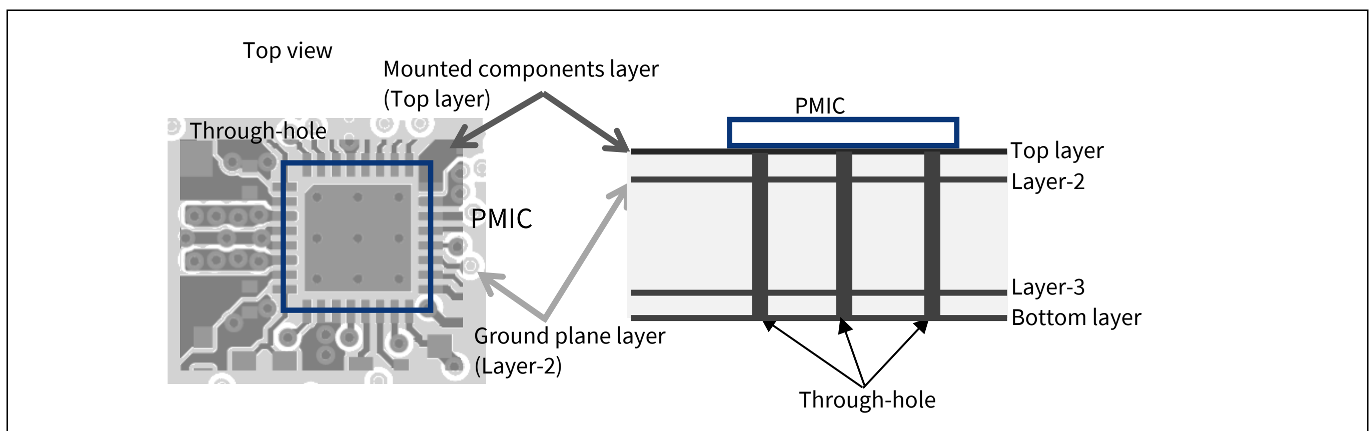

Figure 13 Example of via on surface of EP (S6BP502A)

When using a two-layer board, more care is required than using multilayer-board. This is because a two-layered board has no inner Cu plane, thermal resistance might be higher compared to a multilayer board. Furthermore, because both sides are usually used as wiring layers, it is difficult to have a Cu plane. Even if Cu plane is connected to the ground plane on the back of EP through vias, the ground plane will be divided by wirings. The plane gap caused by this wiring leads to a higher thermal resistance, thus a less effective heat dissipation. To achieve effective heat dissipation, it is recommended to have as much surface wiring as possible to avoid gaps caused by wiring on the back of the PCB, as **Figure 14** shows.

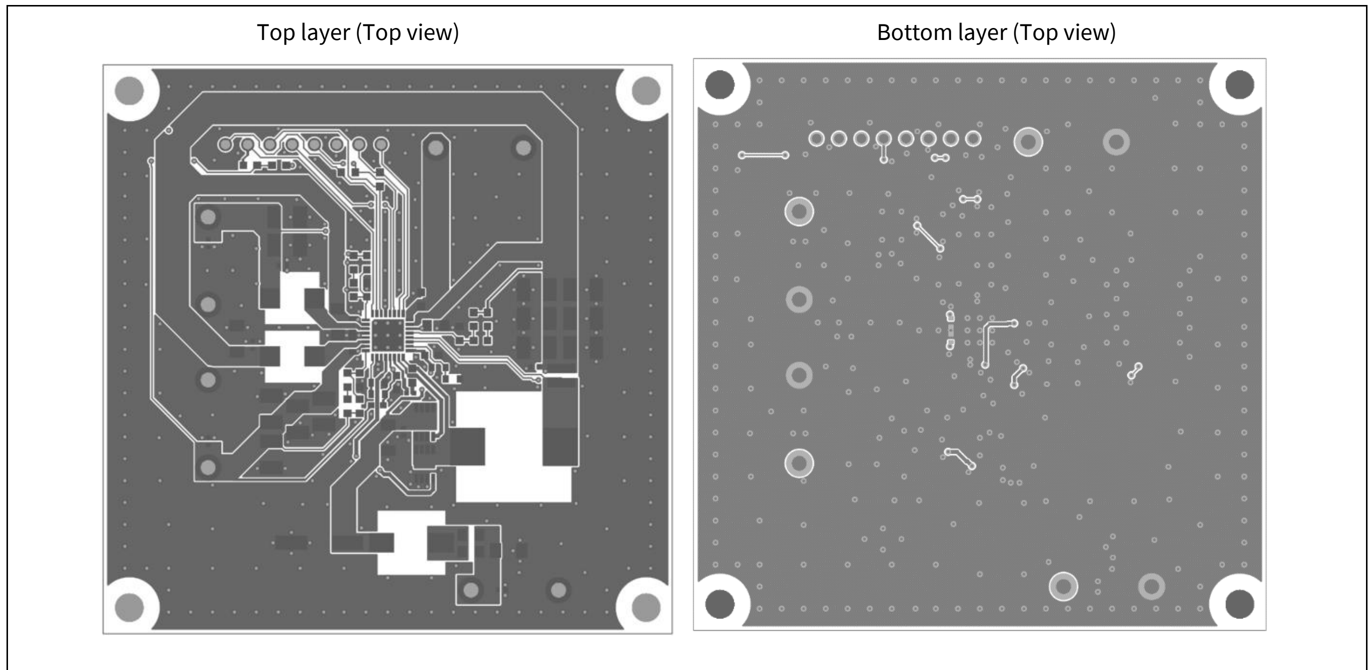

Figure 14 Layout example of 2-layer PCB (S6BP502A)

If wiring on the back of the PCB is inevitable, shorten the wiring as much as possible to ensure that the heat conduction route is not blocked by the wire gap. **Figure 15** shows examples of good and bad wiring on the back of the PCB for effective heat dissipation.

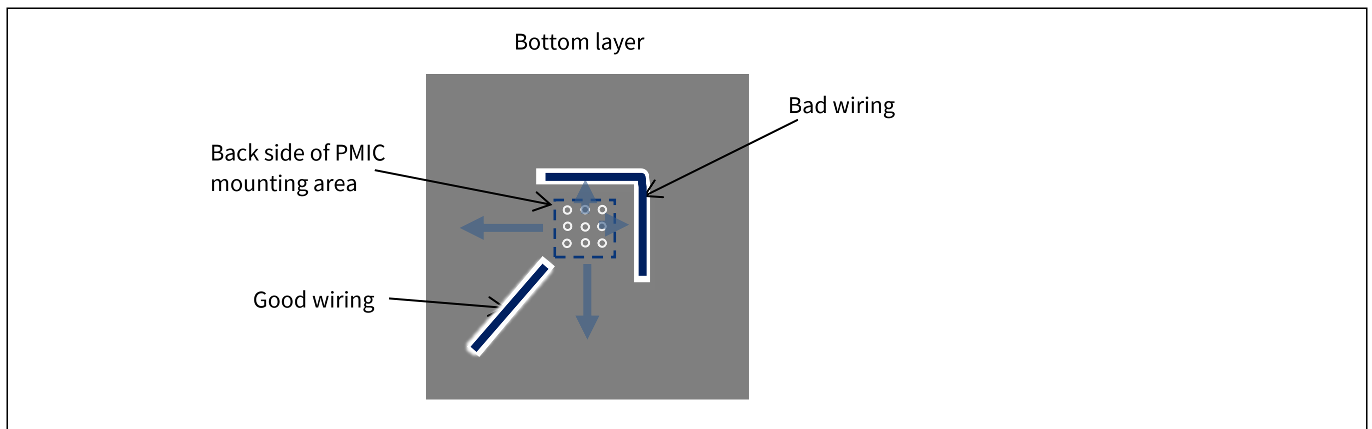

Figure 15 Wiring on the back of a 2-layer PCB (S6BP502A)

Even switching FETs may encounter heat generation problem. In this case, use FETs that have the packages with heat dissipation pad like the ones used in EVK. Similar to PMIC, layout is done to have efficient heat dissipation through the board. If there is insufficient heat dissipation with only the surface plane, it is possible to actively dissipate heat by routing heat to the back of the PCB using vias.

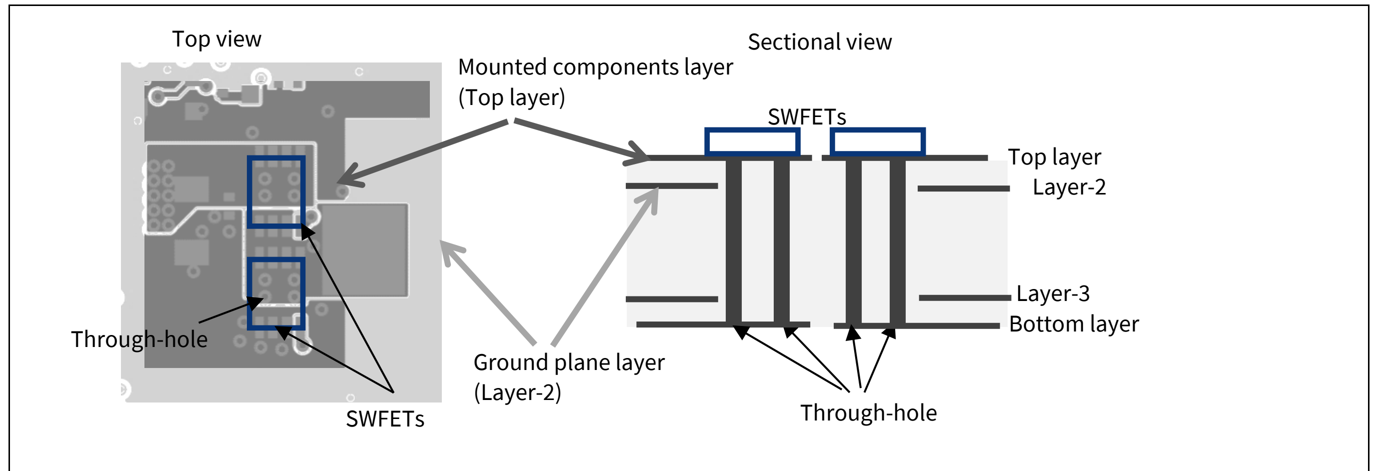

Figure 16 High-frequency current loop (Layer-2)

4 Example of component temperature distribution

Figure 17 shows an example of temperature distribution of S6BP502A EVK.

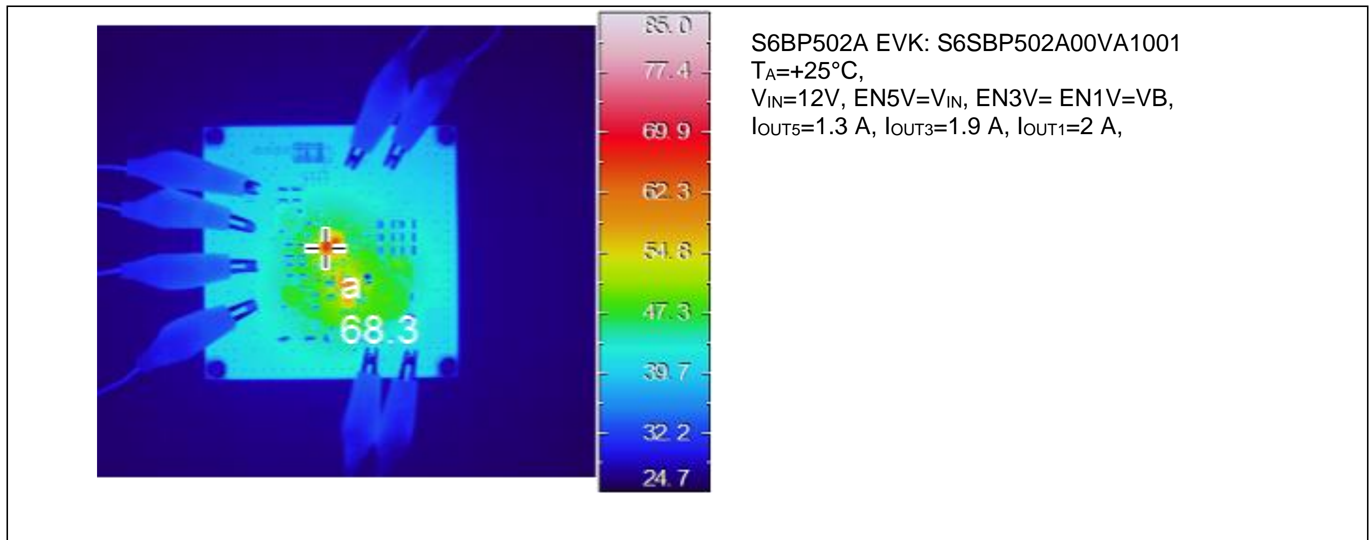

Figure 17 S6BP502A EVK temperature distribution

4.1 Relationship between junction temperature and package temperature

Cypress' automotive PMIC is equipped with an exposed pad (EP). Also, due to the small package size, most of the heat dissipates through the EP and PCB. In this case, Ψ_{JT}, which is the thermal resistance of the junction – package top, is very small. (For instance, Ψ_{JT} of S6BP502A is less than 0.3 °C/W, thus for a 1-W loss, the temperature difference is roughly 0.3°C. See the application note AN201006 for detailed information on thermal resistance Ψ_{JT}). The junction temperature can be estimated by simply checking the package top temperature.

5 Related documents

5.1 Application notes

- AN201006 – Thermal Considerations and Parameters
- AN99497 – Designing a Power Management System with S6BP201A, S6BP202A, and S6BP203A
- AN98649 – How to Design a Power Management System with S6BP401A
- AN99435 – Designing a Power Management System with S6BP501A and S6BP502A

5.2 Datasheets

- S6BP201A, ASSP 42V, 1A, Synchronous Buck-boost DC/DC Converter IC
- S6BP202A, ASSP 42V, 2.4A, Synchronous Buck-boost DC/DC Converter IC
- S6BP203A, ASSP 42V, 2.4A, Synchronous Buck-boost DC/DC Converter IC
- S6BP401A, Power Management IC for Automotive ADAS Platform
- S6BP501A/S6BP502A, 3ch DC/DC Converter IC for Automotive Cluster

5.3 Evaluation kit operation manual

- S6SBP201A1AVA1001, 1ch Buck-Boost DC/DC Converter IC for Automotive applications S6BP201A1A Evaluation Kit
- S6SBP202A1FVA1001, 1ch Buck-Boost DC/DC Converter IC for Automotive applications S6BP202A1F Evaluation Kit
- S6SBP203A8FVA1001, 1ch Buck-Boost DC/DC Converter IC for Automotive applications S6BP203A8F Evaluation Kit
- S6SBP401AM2SA1001, 6ch PMIC for Automotive ADAS S6BP401AM2 Evaluation Kit
- S6SBP501A00VA1001/S6SBP502A00VA1001, Automotive PMIC Evaluation Kit Operation Guide

Revision history

Document version	Date of release	Description of changes
**	2017-12-07	New application note.
*A	2021-06-14	Updated to Infineon template.

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