AN218254

Design Considerations for EMI Reduction in Automotive Power Management Systems

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Associated Part Family: S6BP20xA, S6BP401A, S6BP50xA

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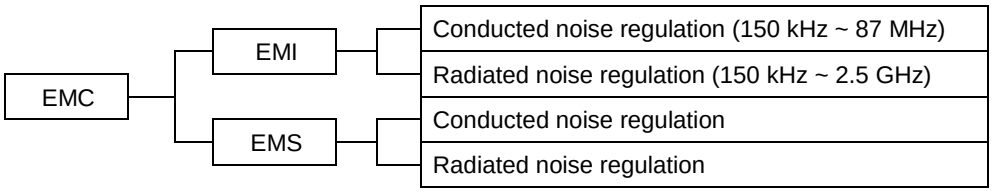
AN218254 explains the important points and some examples for EMI noise reduction of a power management system with Cypress's Power management IC (PMICs).

Contents

1 Introduction

Automotive systems have several receivers, including many receivers installed around the car. International Electro-technical Commission (IEC) has formulated international standards with the aim of protecting these in-vehicle (or peripheral installed) receivers. The international standard for this electromagnetic noise is formulated as CISPR 25, and the power supply contained in the in-vehicle module is required to meet this standard. Electromagnetic noise can be classified as shown in the figure below. EMI is a part of it.

Figure 1. Electromagnetic Noise



Where
EMC: Electromagnetic Compatibility
EMI: Electromagnetic Interference
EMS: Electromagnetic Susceptibility
Frequency in the figure is within the regulated frequency range of CISPR 25

The following table shows the representative Cypress PMICs for automotive.

Table 1. Cypress PIMICs Lineup for Automotive

Part Number	Application	PMIC Type	Power Composition	Switching Freq.	Output Voltage/Current
S6BP201A	Cluster BCM ADAS	Primary	1-ch Buck-boost	200 kHz~2.1 MHz	5.0 V / 1.0 A
S6BP202A					5.0 V / 2.4 A
S6BP203A					3.3 V / 2.4 A
S6BP401A	ADAS	Secondary	4-ch Buck + 2-ch LDO	2.1 MHz	1.0 V~3.4 V / 0.2 A~3 A
S6BP501A	Cluster	Primary + Secondary	2-ch Buck + 1-ch Boost	420 kHz, 2.1 MHz	1.0 V~5.2 V / 1.3 A~1.4 A
S6BP502A					1.0 V~5.2 V / 1.3 A~2.0 A

Where,

ADAS：Advanced Driver Assistance System

BCM： Body Control Module

Refer to the S6BP201A , S6BP202A ,S6BP203A ,、S6BP401A , S6BP501A , S6BP502A datasheet for more information on these PMICs.

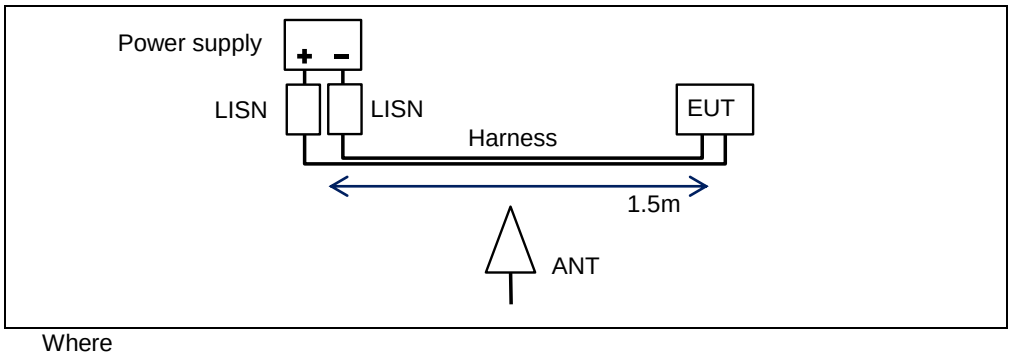
The power supply using Cypress PMICs in automotive systems is a DC/DC converter with switching operation. The electromagnetic noise over 100 MHz, which is far higher than the switching frequency (roughly from 100 kHz to 2 MHz) may occur because of the switching operation and operating environment. Therefore, countermeasures to reduce this electromagnetic noise are required.

This application note explains the EMI countermeasure in designing power supply systems using Cypress PMICs.

2 Relationship Between EMI Noise and Primary Power Supply

CISPR 25 defines the test configuration as shown below for measuring the emitted radiation noise from the equipment.

Figure 2. EMI Radiated Noise Test Configuration Example (Top View)



Where

LISN: Line Impedance Stabilization Network

EUT: Equipment under test

ANT: Antenna

In the case of radiated noise measurement of 1 GHz or less, the antenna is put on the center of the harness. The current (or voltage) of the harness (or LISN) is measured for conducted noise. The length of the harness is different from the test condition for radiation noise. Therefore, it is important to lower the level of the noise source and to prevent noise propagation to the harness to reduce the EMI noise. This harness means that a power supply line for a power supply module including PMICs, and it is particularly important to reduce EMI noise in the primary power supply.

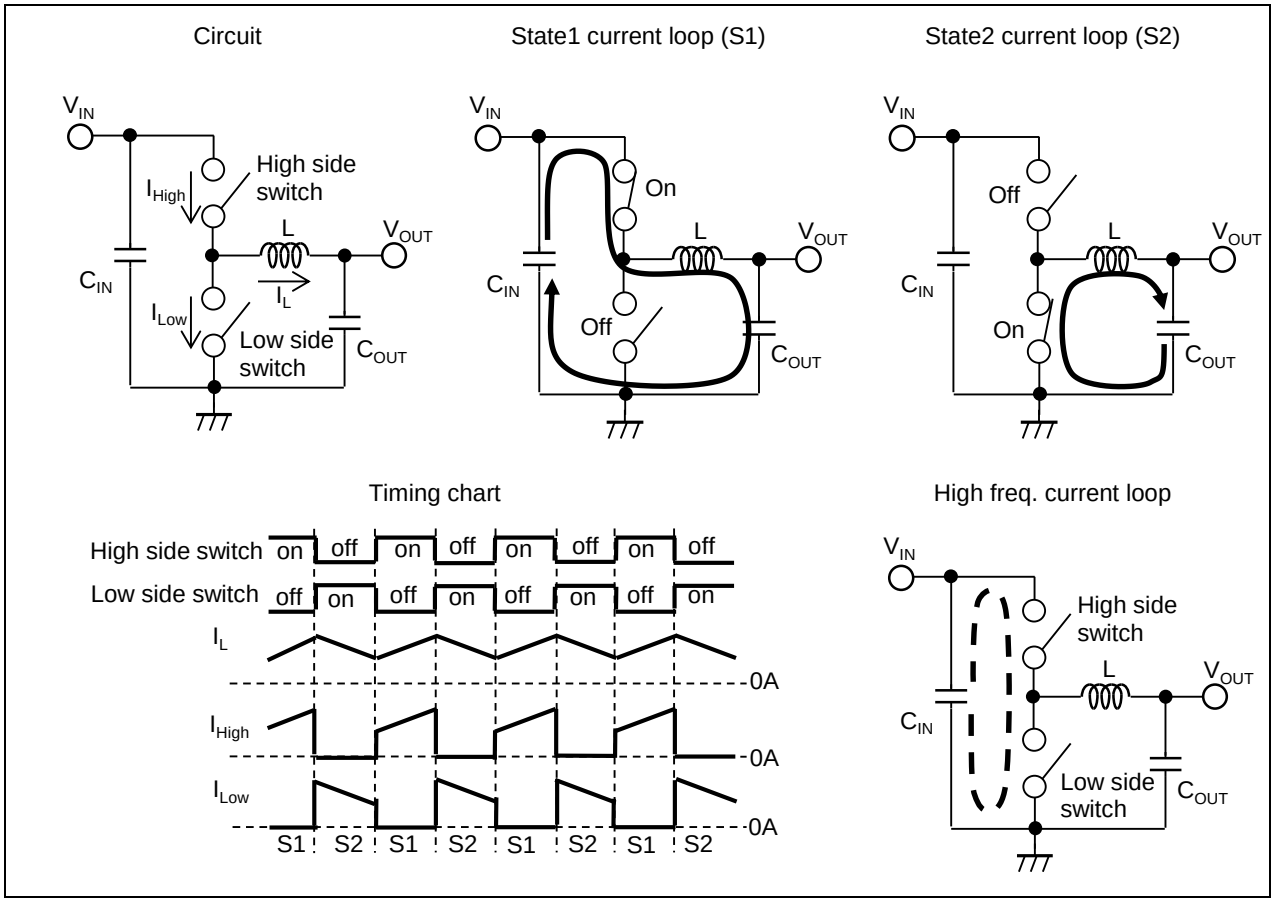
3 High-Frequency Noise Generated by Switching Operation

Cypress PMICs for automotive systems have the 2-MHz switching frequency except for some devices. Therefore, there is almost no issue in the AM radio range (530 kHz to 1.8 MHz) as under 2 MHz, but countermeasures may be required with the over 2-MHz range frequency. This application note describes noise before explaining the countermeasure method. In particular, high-frequency noise above 30 MHz is the most important because the high-frequency current by the switching operation of the DC/DC converter and its path generates the high-frequency noise. This section explains the principle of high-frequency noise in each topology.

3.1 Step-Down Buck Topology DC/DC Converter

Buck Topology DC/DC converter circuit, current loop routing, and timing chart are shown in the following figure.

Figure 3. Buck Topology DC/DC Converter



The Buck topology DC/DC converter constitutes a circuit with the input capacitor (C_{IN}), inductor (L), output capacitor (C_{OUT}), and two switches (High side and Low side switch). The High side switch and Low side switch alternately turns ON or OFF as shown in the timing chart and alternates between State 1 and State 2. The input voltage (V_{IN}) is divided to get the output voltage (V_{OUT}) by smoothing the current flowing through each switch by an LPF (low-pass filter), which consists of L and C_{OUT}. A large current slew rate is generated on the high-frequency current loop of the dashed line indicated at the moment of switching ON and OFF. The parasitic inductance on the loop and the high-frequency current generate the high-frequency voltage, resulting in high-frequency noise. To reduce this high-frequency noise, it is necessary to reduce the parasitic inductance and the current slew rate at the switching moment.

The DC/DC converter channel of each PMIC corresponding to this topology is shown in the table below.

Table 2. Corresponding DC/DC Converter Channel for Buck Topology

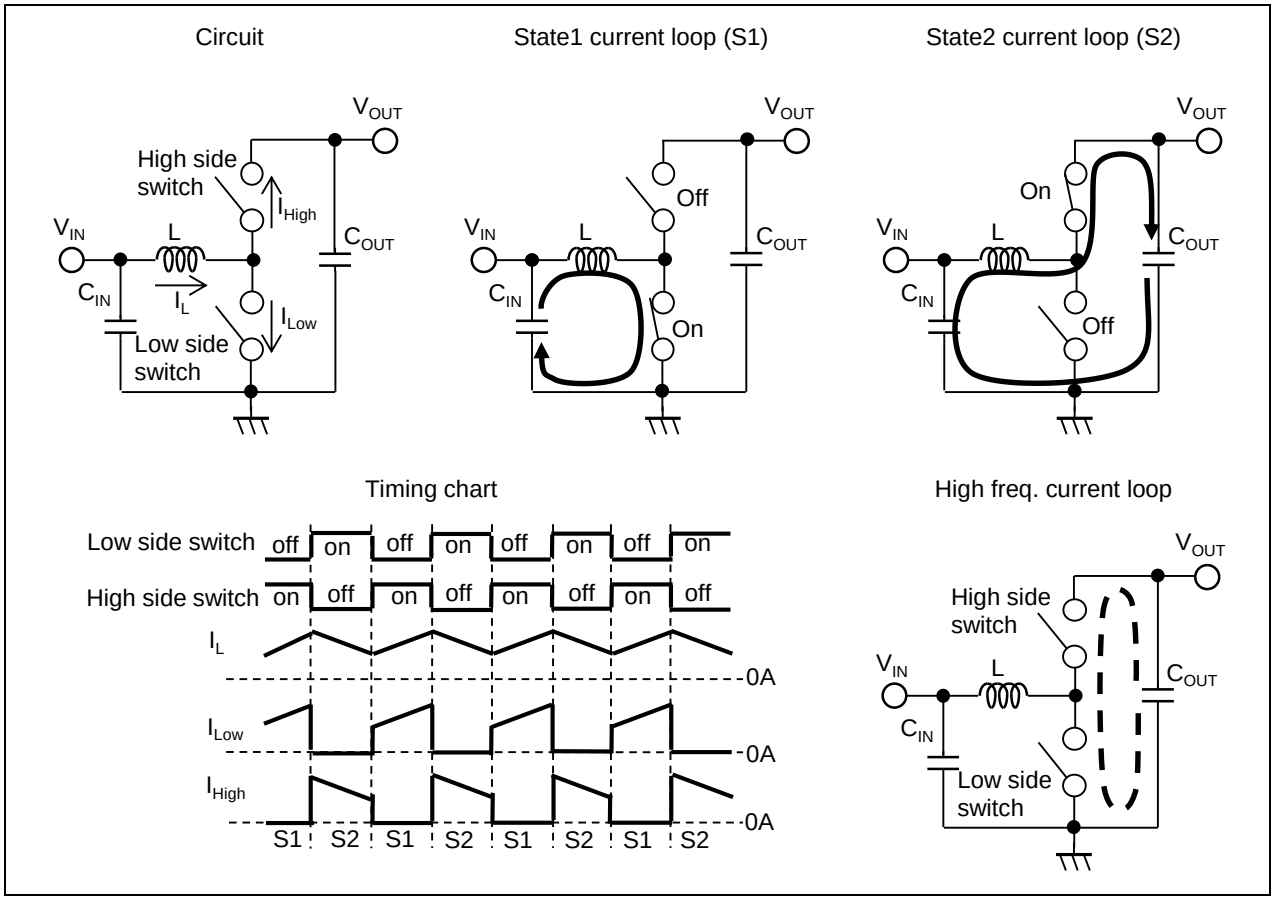
Part Number	DC/DC Converter Channel
S6BP201A,S6BP202A,S6BP203A	None
S6BP401A	DD1, DD2, DD3, DD4
S6BP501A,S6BP502A	DD1V, DD3V

Refer to the S6BP201A, S6BP202A, S6BP203A, S6BP401A, S6BP501A, and S6BP502A datasheets for more detail the DC/DC converter channel.

3.2 Step-Up Boost Topology DC/DC Converter

Boost Topology DC/DC converter circuit, current loop routing, and timing chart are shown in the following figure.

Figure 4. Boost Topology DC/DC Converter



The Boost topology DC/DC converter constitutes a circuit with the input capacitor (C_{IN}), inductor (L), output capacitor (C_{OUT}), and two switches (High side switch, Low side switch). The High side switch and Low side switch alternately turns ON or OFF as shown in the timing chart and alternates between State 1 and State 2. Since the inductor maintains the current in State 2, the step-up voltage is generated and the electric power is supplied to C_{OUT}. The output voltage (V_{OUT}) is generated by smoothing this current with C_{OUT}. A large current slew rate is generated on the high-frequency current loop of the dashed line at the moment of switching ON and OFF. The parasitic inductance on the loop and the high-frequency current generate the high-frequency voltage, resulting in high-frequency noise. To reduce this high-frequency noise, you should reduce the parasitic inductance and the current slew rate at the switching moment.

The DC/DC converter channel of each PMIC corresponding to this topology is shown in the table below.

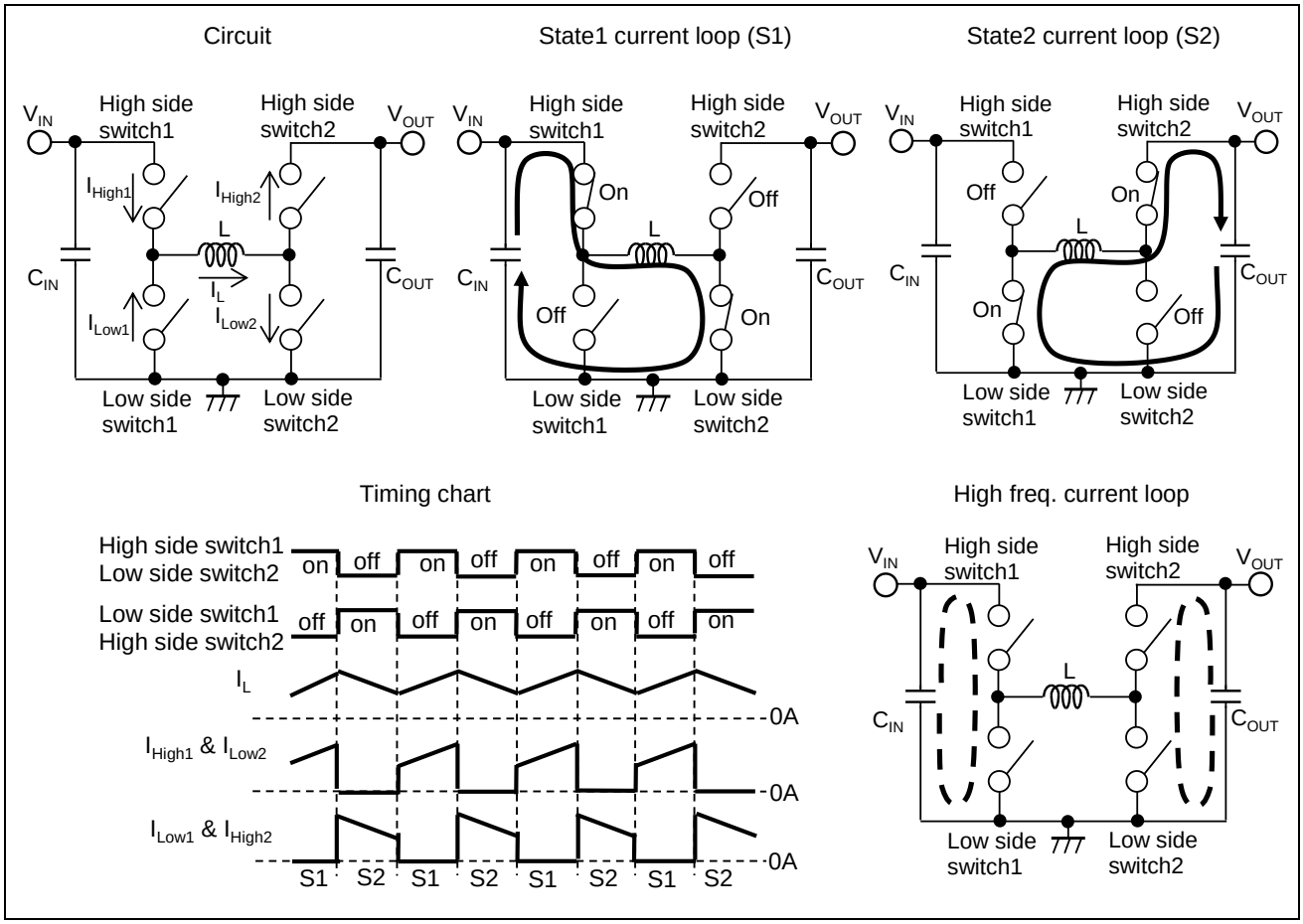
Table 3. Corresponding DC/DC Converter Channel for Boost Topology

Part Number	DC/DC Converter Channel
S6BP201A,S6BP202A,S6BP203A	None
S6BP401A	None
S6BP501A,S6BP502A	DD5V

3.3 Buck-Boost Topology DC/DC Converter

Buck-boost Topology DC/DC converter circuit, current loop routing, and timing chart are shown in the following figure.

Figure 5. Buck-boost Topology DC/DC Converter



The Buck-boost topology DC/DC converter constitutes a circuit with the input capacitor (C_{IN}), inductor (L), output capacitor (C_{OUT}), and four switches (High side switch 1, Low side switch 1, High side switch 2, Low side switch 2). The four switches alternately turn ON or OFF as shown in the timing chart and alternates between State 1 and State 2. The output current (V_{OUT}) is generated by smoothing the current flowing through each of these switches with C_{OUT}. The current flowing through the four switches, C_{IN}, and C_{OUT} has a large current slew rate at the moment of switching ON and OFF. At this time, the high-slew-rate current and the parasitic inductance on the loop of the dashed line indicated generates the high-frequency voltage. High-frequency noise is generated in this way. There are two high-frequency current loops in the Buck-boost circuit. To reduce this high-frequency noise, you should reduce the parasitic inductance and the current slew rate at the switching moment.

The DC/DC converter channel of each PMIC corresponding to this topology is shown in the table below.

Table 4. Corresponding DC/DC Converter Channel for Boost Topology

Part Number	DC/DC Converter Channel
S6BP201A,S6BP202A,S6BP203A	Applicable
S6BP401A	None
S6BP501A,S6BP502A	None

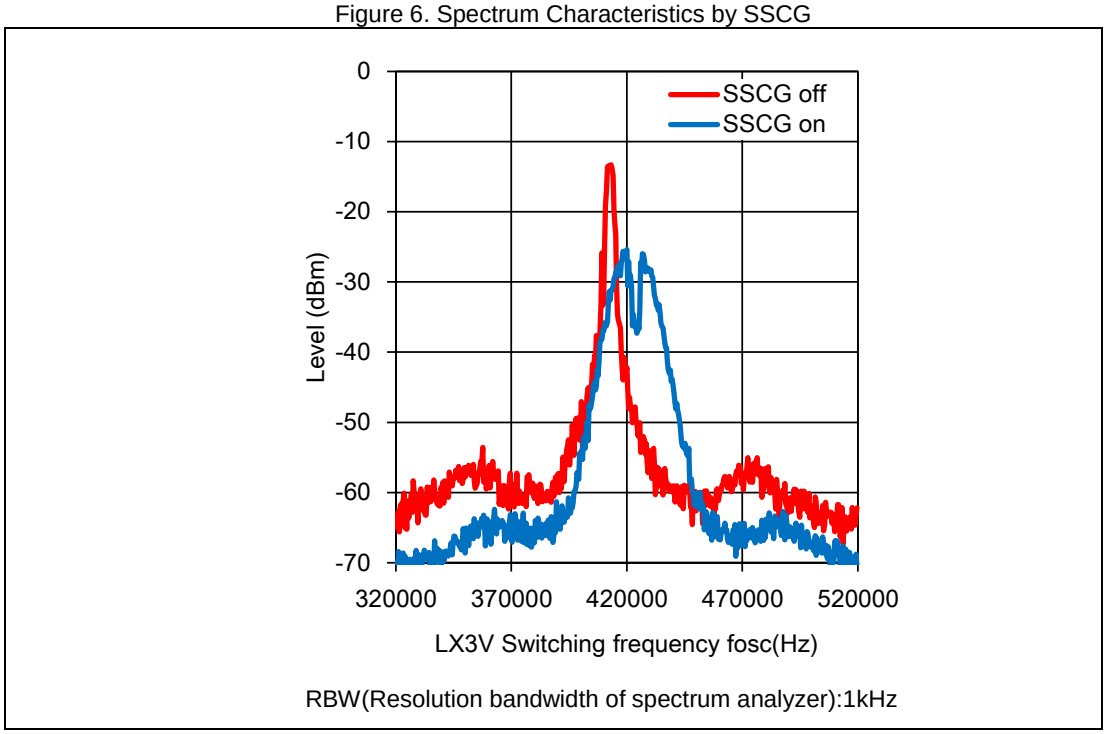
4 Countermeasures of EMI Noise

There are several ways to implement countermeasures for EMI noise reduction. We will explain the setting of PMICs, the components selection, and the PCB layout as the method that does not impact BOM. Additional countermeasures by adding circuits and components will be explained in later sections.

4.1 Spread Spectrum Clock Generator (SSCG) Function

SSCG reduces the EMI noise level by spreading the switching frequency of the DC/DC converter. S6BP501A and S6BP502A have this function that spreads the switching frequency of all DC/DC converter channels by 6%. To enable SSCG, connect the ENSS terminal to the VB terminal (Refer the datasheet about the ENSS terminal and the VB terminal). The diffusion characteristics of the switching node LX3V by the SSCG function is shown below as an example.

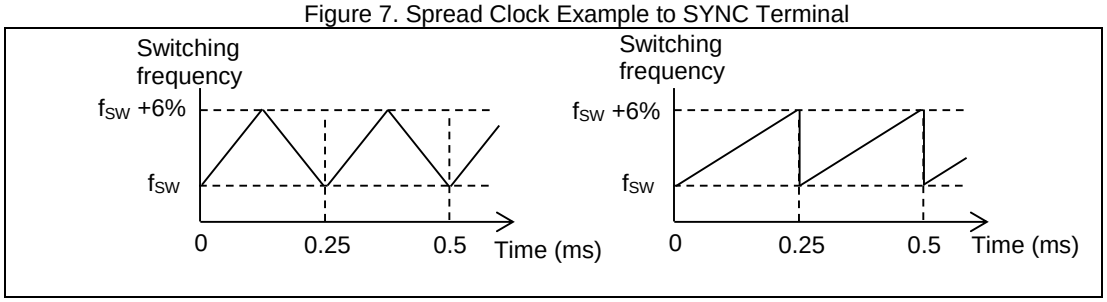
Figure 6. Spectrum Characteristics by SSCG



LX3V is the terminal name of S6BP501A and S6BP502A, which is the switching node signal of the DC/DC converter.

S6BP201A, S6BP202A, S6BP203A, and S6BP401A can work in the same way as the SSCG of S6BP501A and S6BP502A by providing a spread clock signal to the SYNC terminal. The spread clock signal to the SYNC terminal for the SSCG operation is shown below as an example.

Figure 7. Spread Clock Example to SYNC Terminal



4.2 Components Selection of DC/DC Converter

Select components with a small Equivalent Series Inductor (ESL) as a parasitic element which has a high-frequency current loop passing through. If the switching transition time is 2 ns at the load of 2 A in the operation of the DC/DC converter, 1 V is generated only with 1 nH as ESL. Therefore, reduction of ESL is very important for reducing the EMI noise. This section describes components selection.

4.2.1 Input Capacitor, Output Capacitor

It is recommended to select a ceramic capacitor that can effectively absorb the switching frequency ripple current. Ceramic capacitors that satisfy the required capacitance as the input capacitor and the output capacitor are often 3216 size or bigger. For example, a 3216-size ceramic capacitor generally has 1 nH or more inductance as ESL. For ESL reduction, it is recommended to place smaller size ceramic capacitor. For example, the ESL of a 1005-size ceramic capacitor (e.g. 0.1 µF or 0.01 µF) is as small as 0.5 nH. It is also effective to select flip-type ceramic capacitor or three-terminals ceramic capacitor for ESL reduction.

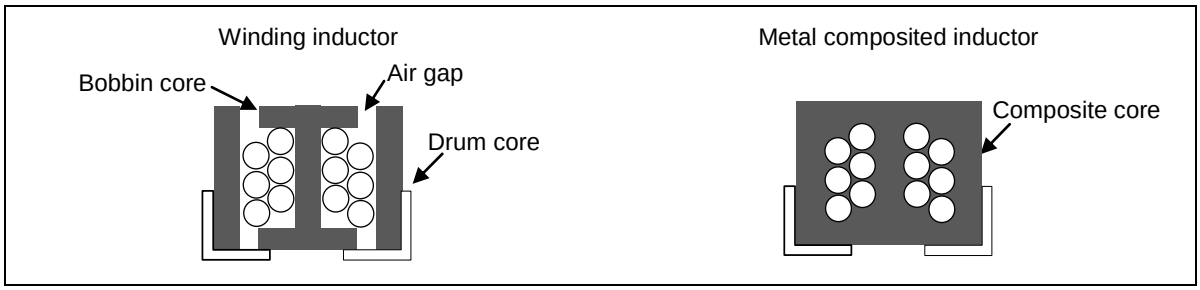
4.2.2 External Switching FET

In the case of the DD3V channel of S6BP501A and S6BP502A, this DC/DC converter channel needs external switching FET. The switching FET should be selected with a small ESL package and lead. For example, a smaller DFN (Dual Flat pack No-leaded) is more advantageous than a conventional lead shape such as SOP (Small Outline Package).

4.2.3 Inductor

In the rare case, unexpected EMI-radiated noise may be generated in the AM radio band (500 kHz to 2 MHz) by the electric field noise from the air gap of the coil. In this case, we can reduce the EMI noise by the changing inductor from the winding inductor with the core air gap to the metal composited inductor. The following figure shows the sectional structure example of each inductor.

Figure 8. The Sectional Structure Example of Each Inductor



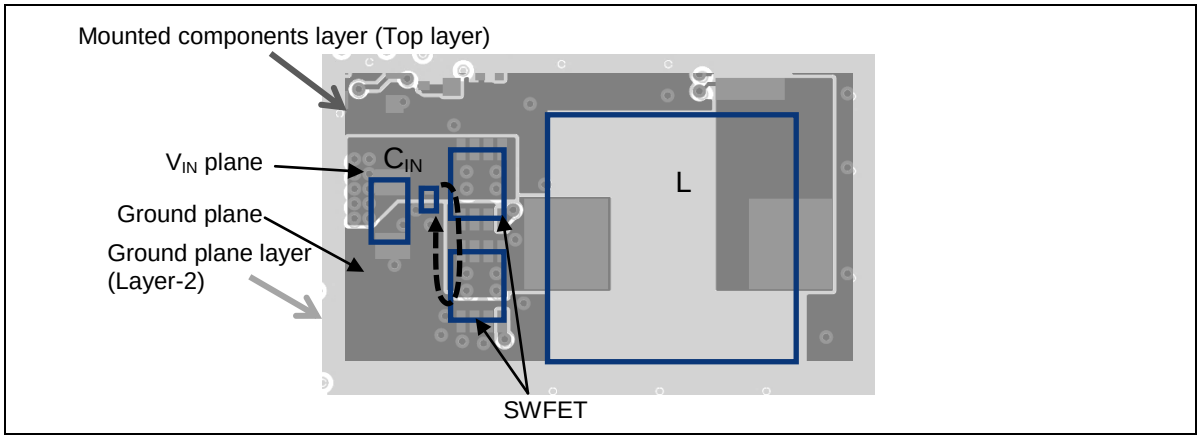
4.3 PCB Layout

The basic policy of EMI noise countermeasures by layout is "to design the PCB layout to have a smaller high-frequency current loop". It is also described in the layout guidelines of the PMIC application note. This section explains specifically about countermeasures for the high-frequency current loop.

4.3.1 Step-down Buck DC/DC Converter

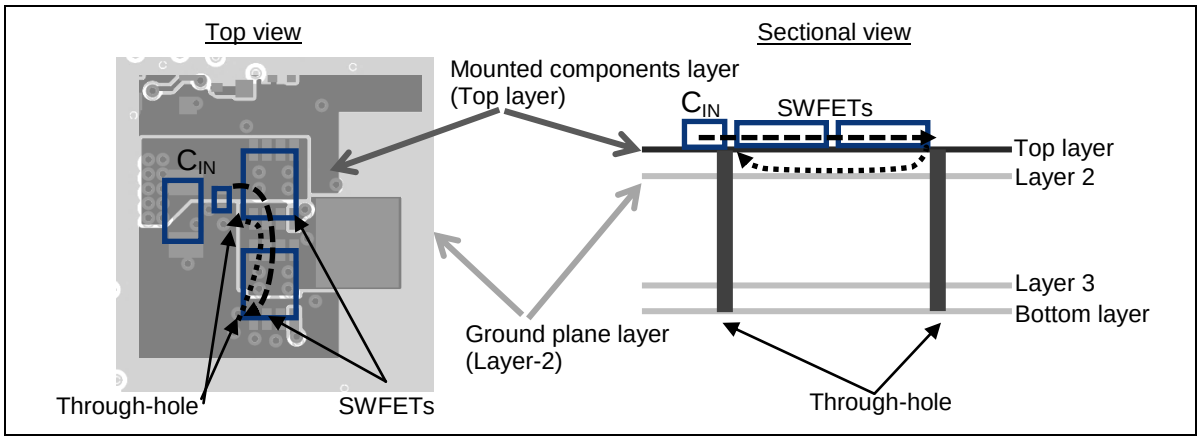
The following figure shows a layout example of the DD3V channel of S6BP502A. This example is the layout design for four-layer PCB; Layer 1 as the Top layer and Layer 2 as the inner layer are excerpted.

Figure 9. Layout Example of DD3V Channel of S6BP502A



The DD3V channel of S6BP502A is a Buck topology DC/DC converter. Therefore, the input capacitor (C_{IN}) and the two switching FETs (SWFET) constitute a high-frequency current loop. In this case, the high-frequency current loop is very small as shown by the dashed line. This is a loop composed on the Top layer, and there is also a loop with Layer 2 as the inner layer ground plane shown in the following figure. This current loop also is indicated by a dashed line, and the right-side figure is a diagram of the PCB cross section.

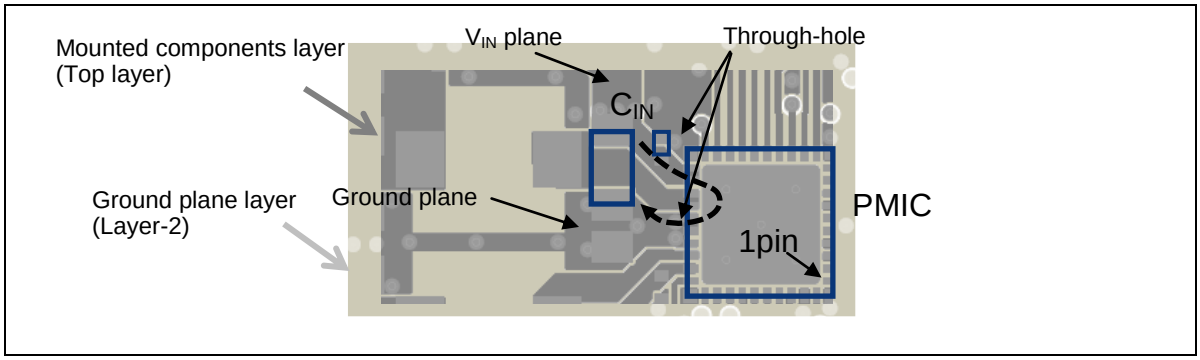
Figure 10. High-Frequency Current Loop with Layer 2



In the case of a four-layer PCB, the gap between the Top layer and Layer 2 is generally 100 µm ~ 200 µm and the loop area is also very small. The ground plane directly under the component mounting surface can ensure this short high-frequency current return path. High-frequency current flows through the loop with the top layer and loop with Layer 2, the smaller the loop inductance. In the case of a four-layer PCB, narrowing the interlayer gap is the countermeasure for reducing the high-frequency EMI noise. In the case of a two-layer PCB, since the PCB thickness is the same as the layer gap, the parasitic inductance of the loop becomes 8 ~ 16 times that of the four-layer PCB; this means that two-layer PCB is disadvantageous.

The following figure shows an example layout of the DD2 channel of the S6BP401A in the case of the integrated switching FETs in PMIC. This layout example also is with a four-layer PCB, and Layer 1 (Top layer) and Layer 2 of the inner layer are extracted.

Figure 11. Layout Example of DD2 Channel of S6BP401A

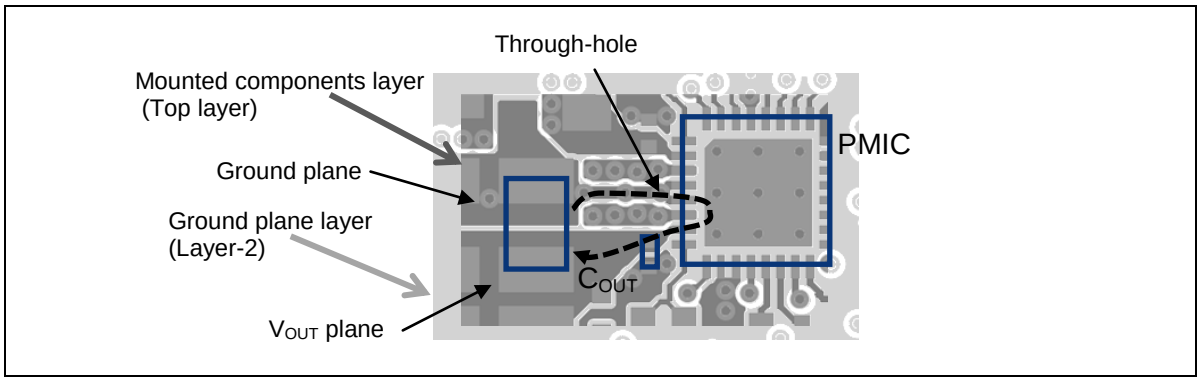


DD6 of S6BP401A is a Buck topology DC/DC converter. Since two switching FETs are built in the PMIC, a high-frequency current loop is composed of the input capacitor (C_{IN}) and the PMIC itself. In this layout example, the high-frequency current loop is shown by the dashed line. This is a loop composed by the top layer, and there is also a loop with Layer 2 of the inner layer ground plane as a route as in the case of the DD3V channel described above. In the case of this layout example also, both high-frequency current loops are the shortest.

4.3.2 Step-up Boost DC/DC Converter

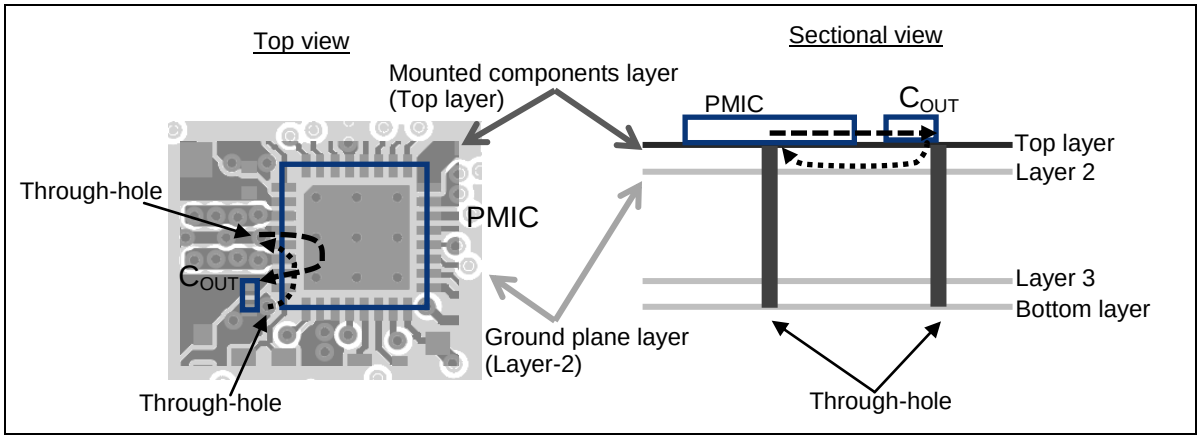
The following figure shows a layout example of the DD5V channel of S6BP502A. This example is the layout design for a four-layer PCB; Layer 1 as the Top layer and Layer 2 as the inner layer are excerpted.

Figure 12. Layout Example of DD5V Channel of S6BP502A



The DD5V channel of S6BP502A has Boost topology. Since the two switching FETs are built in the PMIC, a high-frequency current loop is formed by the output capacitor (C_{OUT}) and PMIC. In the case of this layout example, the high-frequency current loop is shown by the dashed line. This loop is composed on the Top layer, and there is also a loop with Layer 2 of the inner layer ground plane shown in the following figure. The current loop is shown by the dashed line, and the right-hand side section shows the PCB cross section.

Figure 13. High-Frequency Current Loop with Layer 2

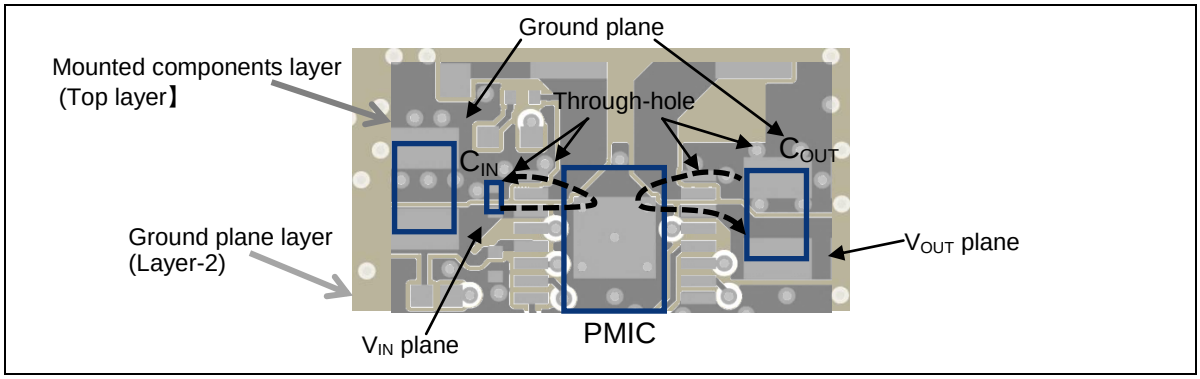


The high-frequency current loop with Layer 2 is also the shortest in this layout example.

4.3.3 Buck-boost DC/DC Converter

The layout example of S6BP202A is shown in the figure below. This example is for a four-layer PCB; Layer 1 (Top layer) and Layer 2 of the inner layer are extracted.

Figure 14. Layout Example of S6BP202A



S6BP202A is a Buck-boost topology DC/DC converter. Since the four switching FETs are built in the PMIC, the two high-frequency current loops are constituted by an input capacitor (C_{IN}) and two switching FETs (SWFETs) inside the PMIC and by an output capacitor (C_{OUT}) and two switching FETs (SWFET) inside the PMIC. In the case of this layout example, high-frequency current loop is shown by the dashed line. This is a loop composed on the Top layer, and there is also a loop with Layer 2 of the inner layer ground plane as well as other topologies; this current loop is also the shortest in this layout.

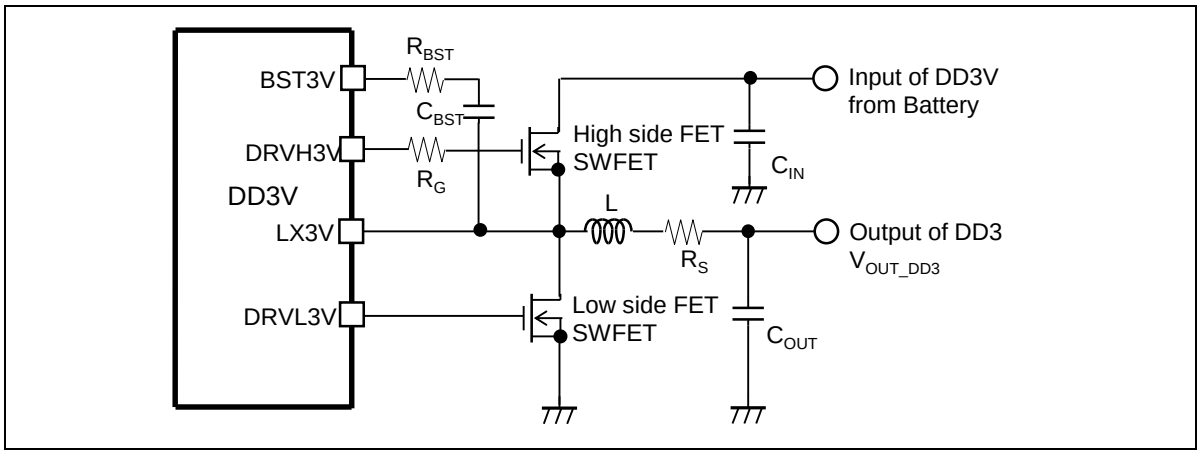
4.4 Adding Circuits and Components

For the countermeasures by adding circuits and parts for EMI noise reduction, there are the following methods:

4.4.1 Bootstrap Resistor (R_{BST}), Switching FET Gate Resistor (R_G)

The following figure shows the circuit example of the buck Converter.

Figure 15. DD3V Layout Example of S6BP502A



BST3V, DRVH3V, LX3V, and DRVL3V are PMIC terminal names. Refer to the S6BP501A,S6BP502A datasheet for more details.

The reduction in the switching current slew rate is also effective to reduce high-frequency noise above 30 MHz. This means lowering the switching speed of the switching FET. In the case of the buck converter, the SWFET switching speed of the high-side FET is important for EMI noise reduction.

The bootstrap resistor (R_{BST}) can lower the rising edge slew rate of the switching node waveform connected to LX3V. This countermeasure is applicable to the DC/DC converter channel, which has a bootstrap capacitor.

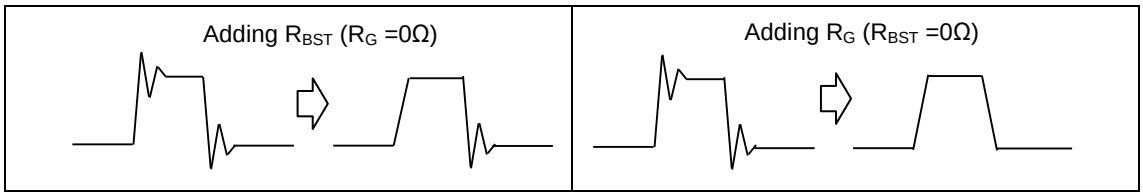
It should be confirmed that increasing of R_{BST} may affect the conversion efficiency of the DC/DC Converter and the limitation of the charge current to the bootstrap capacitor (C_{BST}). R_{BST} should be determined by confirming the EMI noise level, the switching waveform, and the conversion efficiency of the DC/DC converter. When R_{BST} increases, the EMI noise level improves. However, when the R_{BST} value is too high, the switching waveform collapses from square wave and conversion efficiency becomes low. Considering these factors, the value of R_{BST} is typically 10 Ω

In another approach, the gate resistance (R_G) of the High side FET can lower the rising and falling edge slew rate of the switching node waveform connected to LX3V. This countermeasure is applicable to the DC/DC converter channel, which has the switching FETs outside the PMIC.

It should be confirmed that increasing of R_G may affect the OFF timing of the High side FET to be delayed. In this timing, if the Low side FET turns ON, a large through current may flow. R_G also should be determined by confirming the EMI noise level, the switching waveform, and the conversion efficiency of the DC/DC converter. Considering these factors, a value of 10 Ω is recommended for R_G.

The following figure shows the effectiveness of the reducing waveform slew rate by adding each resistor.

Figure 16. Effectiveness of Reducing Waveform Slew Rate by R_{BST}, R_G



The PMICs channels to which this solution can be applied are shown in the following table.

Table 5. Corresponding DC/DC Converter Channel for Adding R_{BST}, R_G

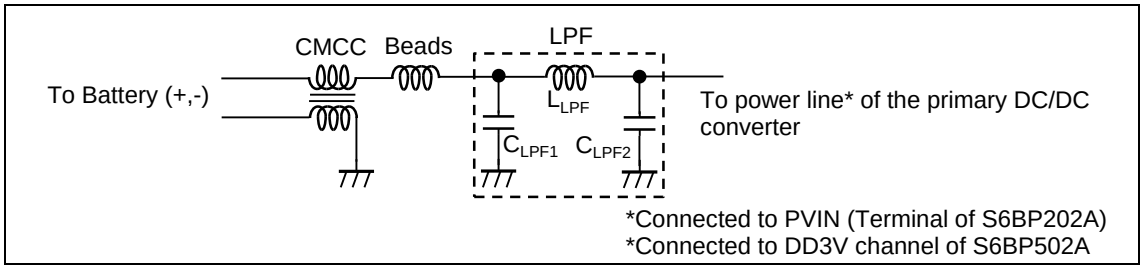
Part Number	Adding R_{BST}	Adding R_G
S6BP201A,S6BP202A,S6BP203A	Applicable	Not applicable
S6BP401A	Not applicable	Not applicable
S6BP501A,S6BP502A	Applicable to DD3V only	Applicable to DD3V only

If both R_G and R_{BST} are applicable, R_{BST} should be tried as the countermeasure first; if the improvement by R_{BST} is not enough, then RG should be tried after changing R_{BST} to 0 Ω.

4.4.1 Low-Pass Filter (LPF), Chip Beads (Beads), Common Mode Choke Coil (CMCC)

If the switching ripple current of the primary power supply is conducted on the power supply line, the EMI noise level may increase in the AM radio (500 kHz to 2 MHz) or higher ranges. In this case, adding an LPF between the primary power supply and the power supply harness from the battery improves EMI reduction. Beads or CMCC is effective in reducing the EMI noise of the high-frequency range exceeding 30 MHz. Beads can effectively reduce the differential EMI noise on the positive side and negative side harness from the battery. CMCC can effectively reduce the common EMI noise. Beads and CMCC selected for the power supply line must satisfy the current rating and have the effective noise reduction characteristics with EMI noise frequency range. An example of an additional circuit is shown in the following figure.

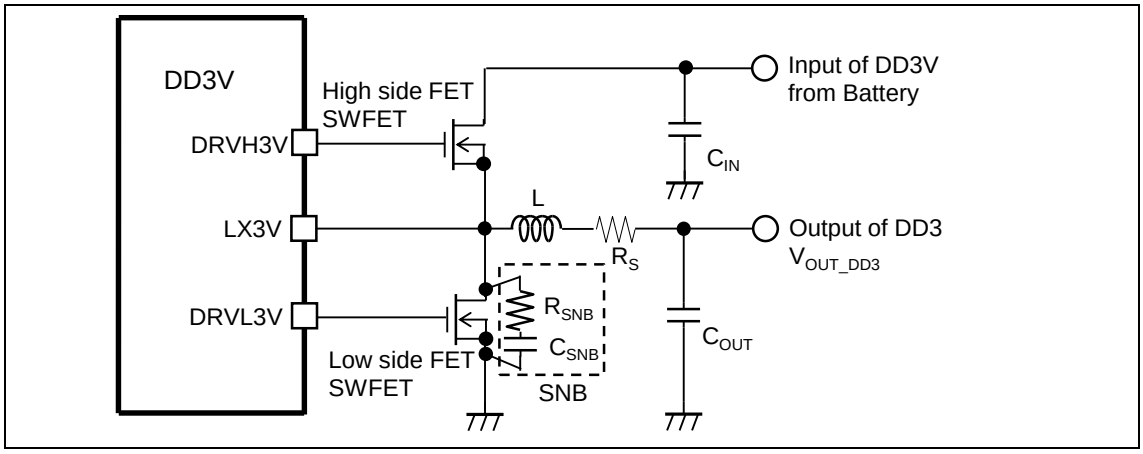
Figure 17. Circuit Example with LPF, Beads and CMCC



4.4.2 Snubber (SNB) of Switching Node

The following figure shows the DD3V channel circuit of S6BP502A as an example of the buck DC / DC converter.

Figure 18. Circuit Example with SNB



When there is high-frequency (over 30 MHz) ringing waveform on the switching node connected to LX3V, SNB can reduce the ringing waveform. In general, R_{BST} and R_G referred in section 4.4.1 are more effective for EMI, but SNB can help to reduce the EMI noise if RBST and RG are not effective enough or R_{BST} and R_G are not applicable. The SNB is connected to a resistor (RSNB) and a capacitor (CSNB) inline as shown in Figure 18. Small-size chip resistors or ceramic capacitors should be used as SNB components because small-size chip components have small ESL. (e.g., ESL of 1005 size chip capacitor is 0.5 nH)

General SNB connection points of each topology are shown in the table below.

Table 6. SNB's Connection Points

Topology	Connecting Point
Buck	Drain-Source of Low side FET
Boost	Drain-Source of High side FET
Buck-boost	LX1-PGND1

LX1, PGND1 are the terminal names of S6BP201A, S6BP202A, S6BP203A.

Refer to the S6BP201A , S6BP202A , S6BP203A datasheet for more detail.

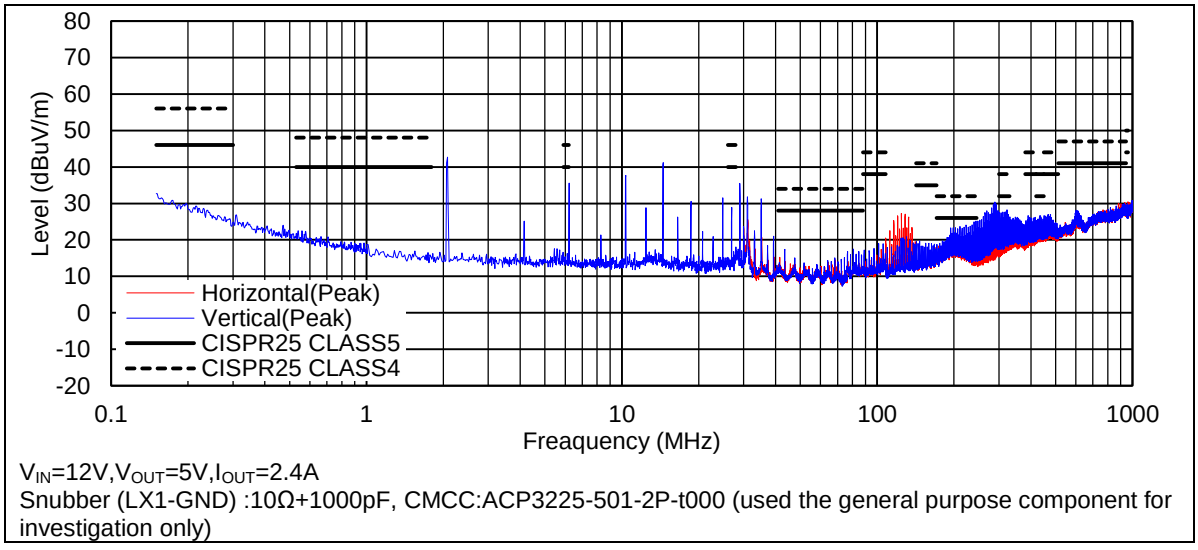
4.5 Shield

The shield of the DC/DC converter should have a height as low as possible and its size should be compact. Generally, the shield is made by a ferromagnetic material such as iron, but shielding by copper also is effective for electromagnetic field noise reduction at high-frequency (30 MHz or more) and for electric field noise reduction at low-frequency (30 MHz or less).

5 EMI Radiated Noise Level Examples

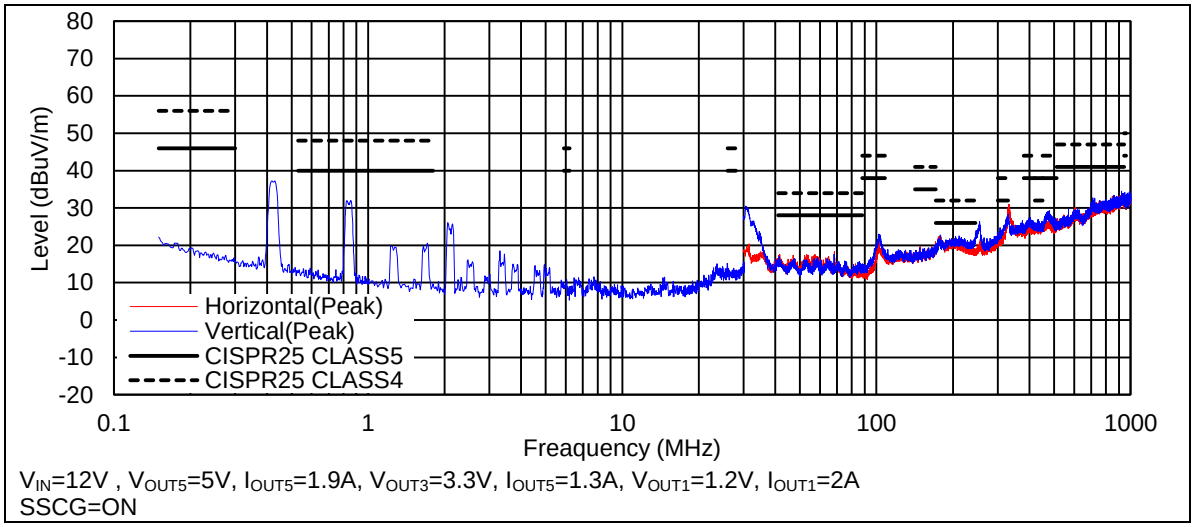
The EMI radiated noise level (peak value) examples of the primary DC/DC converter are below.

Figure 19. S6BP202A (EUT: S6SBP202A1FVA1001)



V_{IN}=12V,V_{OUT}=5V,I_{OUT}=2.4A
Snubber (LX1-GND) :10Ω+1000pF, CMCC:ACP3225-501-2P-t000 (used the general purpose component for investigation only)

Figure 20. S6BP502A (EUT: S6SBP502A00VA1001)



6 Related Documents

6.1 Application Notes

- AN99497 - Designing a Power Management System with S6BP201A, S6BP202A, and S6BP203A
- AN98649 - How to Design a Power Management System with S6BP401A
- AN99435 - Designing a Power Management System with S6BP501A and S6BP502A

6.2 Datasheets

- S6BP201A - S6BP201A, ASSP 42V, 1A, Synchronous Buck-boost DC/DC Converter IC
- S6BP202A - S6BP202A, ASSP 42V, 2.4A, Synchronous Buck-boost DC/DC Converter IC
- S6BP203A - S6BP203A, ASSP 42V, 2.4A, Synchronous Buck-boost DC/DC Converter IC
- S6BP401A - S6BP401A Power Management IC for Automotive ADAS Platform
- S6BP501A, S6BP502A datasheet -S6BP501A, S6BP502A 3ch DC/DC Converter IC for Automotive Cluster

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**	5660986	YMAE	05/26/2017	New application note

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