PSoC 6 MCU Hardware Design Considerations

Associated part family

PSoC 6 MCU

About this document

Scope and purpose

AN218241 shows you how to design a hardware system around a PSoC® 6 MCU device, starting with considerations for package selection, power, clocking, reset, I/O usage, programming and debugging interfaces, and analog module design.

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1 Introduction

PSoC 6 MCU is Cypress' ultra-low-power PSoC device with a dual-CPU architecture tailored for smart homes, IoT gateways, and so on. The PSoC 6 MCU device is a programmable embedded system-on-chip that integrates the following features on a single chip:

- Single-CPU microcontroller: Arm® Cortex®-M4 (CM4) or Dual-CPU microcontroller: Arm Cortex-M4 (CM4) and Cortex-M0+ (CM0+).
- Programmable analog and digital peripherals.
- Up to 2 MB of flash and 1 MB of SRAM.
- Fourth-generation CapSense® technology.

This application note discusses considerations for hardware design including package, power, clocking, reset, I/O usage, programming/debugging, CapSense, and BLE antenna design.

The PSoC 6 MCU device must be configured to work in its hardware environment, which you can do with integrated design environment (IDE) like PSoC Creator™ or ModusToolbox™ IDE. The application note explains various configurations available in PSoC Creator and ModusToolbox IDE required to set up the device for a given hardware environment.

To get started with PSoC 6 MCU, see **AN228571 – Getting Started with PSoC 6 MCU on ModusToolbox** or **AN221774 – Getting Started with PSoC 6 MCU on PSoC Creator**.

2 Package Selection

One of the first decisions that you must make for your PCB is the choice of package. Several considerations drive this decision, including the number of PSoC device pins required, PCB and product size, PCB design rules, and thermal and mechanical stability. PSoC 6 MCU devices are available in BGA, WLCSP, MCSP, QFN, and TQFP packages – see **Table 1**. See the respective device **datasheet** for more details on packaging.

Table 1 Package Dimensions

PSoC 6 MCU Device	Package
CY8C61x6/7	124-BGA
	80-WLCSP
CY8C62x6/7	124-BGA
	80-WLCSP
CY8C63x6/7	116-BGA
	104-MCSP
	124-BGA
	68-QFN
CY8C61xA/8 CY8C62xA/8	124-BGA
	128-TQFP
	100-WLCSP
CY8C61x5 CY8C62x5	100-TQFP
	68-QFN
	49-WLCSP
CY8C62x4	80-TQFP
	64-TQFP
	68-QFN

As a design reference, see **PSoC 6 MCU CAD Libraries**, which contain PSoC 6 MCU schematics and PCB libraries. Note that you may need to modify the libraries slightly when you use them in your hardware design. Infineon takes no responsibility for issues related to the use of the libraries.

3 Power

PSoC 6 MCU can be powered by a single supply with a wide voltage range, from 1.7 V to 3.6 V. As listed in **Table 2**, it has separate power domains for analog and digital modules. Details of connections to these pins are discussed in the **Power Pin Connections** section.

3.1 Buck Regulator Inductor/Capacitor Selection

PSoC 6 MCU has an on-chip buck regulator. In some PSoC 6 MCU devices, the buck regulator generates two outputs (VBUCK1 and VRF). The VBUCK1 output can power the PSoC 6 MCU core. The VRF output can power the BLE radio in CY8C63x6/7 devices. In other PSoC 6 MCU devices, the on-chip buck regulator generates one output that can power the MCU core. See **Table 2** to know the type of buck regulator supported by the PSoC 6 MCU device selected for your design.

When selecting the inductor and capacitor for the buck regulator, it is recommended to use the following components:

Inductor: Use an inductor with an inductance value of 2.2 µH. It is recommended to keep the DC resistance below 0.2 Ω.

Capacitor: The capacitor connected to the output of the buck regulator should meet the required capacitance at the operating voltage (1.1 V or 0.9 V) that is, 4.7 µF load capacitor for VCCD pin. For BLE operation in CY8C63x6/7 devices, a load capacitor of 10 µF at VRF pin or VDCDC pin is required. See **Figure 1** and **Figure 2**. It is recommended to use a load capacitor with dielectric constant of X5R or above.

See the "Power Supply and Monitoring" chapter of **PSoC 6 MCU: Architecture TRM** for details on the buck regulator and how to use it.

Table 2 PSoC 6 MCU Power Domains

Power Domain	Supply Pin[1]	Ground Pin	Supported Voltage Range	Description	Supported Devices
SIMO Buck Regulator	VDD_NS[2]	VSS	1.7 V to 3.6 V	Input to the SIMO Buck Regulator	CY8C61x6/7, CY8C62x6/7, CY8C63x6/7 devices
	VBUCK1[2]	VSS	ULP or LP	Output 1 of on-chip SIMO regulator. Requires bypass capacitor connection for proper operation. This output can power VCCD when internal regulators are powered down. See the device **datasheet** for supported voltage range (ULP or LP).	
	VRF[2]	VSS	1.05 V to 1.50 V	Output 2 of on-chip SIMO regulator. Requires bypass capacitor connection for proper operation. This output can power the VDCDC input.	
	VIND1[2], VIND2[2]	–	–	Pins for inductor required by the SIMO buck regulator	

[1] Availability of supply pins in various power domains depends on the device. See the respective device **datasheets** for more details.

[2] Optional supply pins. When these supply rails (input or output) are not used, it is recommended to leave the pin floating. For example, when USB is not used, you can leave VDDUSB supply pin floating.

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Power Domain	Supply Pin[1]	Ground Pin	Supported Voltage Range	Description	Supported Devices
SISO Buck Regulator	VDD_NS[2]	VSS	1.7 V to 3.6 V	Input to the SISO buck regulator	CY8C61xA/8, CY8C62xA/8, CY8C61x5, CY8C62x5, CY8C62x4 devices
	VIND[2]	–	–	Inductor connection for the internal buck regulator	
Analog	VDDA	VSS	1.7 V to 3.6 V	Analog power supply input	All PSoC 6 MCU devices
Digital	VDDD	VSS	1.7 V to 3.6 V	Digital power supply input and core regulators' supply input	All PSoC 6 MCU devices
	VCCD	VSS	ULP or LP	Internal core regulators' (LDO) output. Requires bypass capacitor connection for proper operation. Used as core supply input when internal regulators are OFF. Refer to device **datasheet** for supported voltage range (ULP or LP).	
	VDDUSB[2]	VSS	2.85 V to 3.6 V	Power supply pin for USB block. When USB is not used, the pin can support voltage ranging from 1.7 V to 3.6 V	PSoC 6 MCU devices with USB support
I/O	VDDIOx where x = 0,1,2	VSS	1.7 V to 3.6 V	I/O power supply input	All PSoC 6 MCU devices
RF	VDDR[2]	VSSR	1.05 V to 1.50 V	BLE radio analog supply input; connected to VDCDC externally	CY8C63x6, CY8C63x7 devices
	VDDR_HV[L]	VSS	1.75 V to 1.95 V	PSoC 6 MCU to BLE radio interface supply output; requires bypass capacitor connection for proper operation	
	VDCD[C]	VSS	1.05 V to 1.50 V	BLE radio digital supply input; typically connected to VRF externally	
	DVDD[2]	VSS	~ 1 V	BLE subsystem regulators' (LDO) output; requires bypass capacitor connection for proper operation	
Backup	VBACKUP	VSS	1.4 V to 3.6 V	Backup domain supply	All PSoC 6 MCU devices

3.2 Power Pin Connections

PSoC 6 MCU offers power supply options that support a wide range of application voltages and requirements. The VDDD input supports a voltage range of 1.7 V to 3.6 V. If the application voltage is in this range, then PSoC 6 MCU can be connected directly to the application voltage. In applications that have the voltage beyond this range, a suitable power management IC (PMIC) should be used to bring the voltage to this range.

Figure 1 and **Figure 2** show various power pads in PSoC 6 MCU and the recommended connections for a typical design. The VBACKUP power pin can operate from 1.4 V to 3.6 V and can exist independent of other rails. Therefore, the VBACKUP rail can be connected to a separate rail such as a coin cell battery or a super capacitor

or tied to VDDD directly if the design does not support a separate VBACKUP supply. Other supply rails and pins such as VDDA and VDDIO also exist independent of VDDD and VCCD. In addition, the power rails provide supply voltage to I/O ports. **Table 3** shows the I/O ports and their respective power supply rails. I/O levels on a port should not exceed its supply voltage; otherwise it will be clamped to the supply level.

Table 3 Power Supply for I/O Ports

I/O Ports Powered	Power Supply Rail	Alternate Supply Rail
Port 0	VBACKUP	VDDD
Port 1	VDDD	-
Port 2, 3, 4	VDDIO2	-
Port 5, 6, 7, 8	VDDIO1	-
Port 9, 10	VDDIOA	VDDA
Port 11, 12, 13	VDDIO0	-
Port 14	VDDUSB	-

*Note: Availability of ports depends on the device. See the respective device **datasheets** for details on available port pins.*

As a rule of thumb, connect one 0.1-µF and one 1-µF (10 µF in some cases; see **Figure 1** and **Figure 2**) ceramic decoupling capacitor to each power supply pin. Note that certain packages have more than one VDDD, VDDA, VDDR, and VDDIOx (x = 0, 1, 2) pins. In such cases, where the same power supply pin is brought out to multiple pins, the pins can be shorted externally and can share the decoupling capacitors. For example, in 100 TQFP package of CY8C62x5 device, pin VDDIO0 is brought out to pin 91 and pin 92 of the device. These pins (pin 91 and pin 92) can be shorted together and share the same decoupling capacitors. For package specific power supply consideration, refer to the respective device **datasheets**. A ferrite bead is recommended between the input supply and the VDD_NS pin for isolating the VDD_NS domain from the supply. This is because of the noise injected on the VDD_NS rail from the SIMO buck operation. See **Figure 1** and **Figure 2** for recommended values of various components used. The PCB trace between the pin and the capacitors should be as short as possible. For more information, see **Appendix A -** PCB Layout Tips.

Note: It is a good practice to check a capacitor's datasheet before you use it, specifically for working voltage and DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the DC bias is a significant lower percentage of the rated working voltage. Ensure that the capacitance variation is lower for the operating voltage range it serves.

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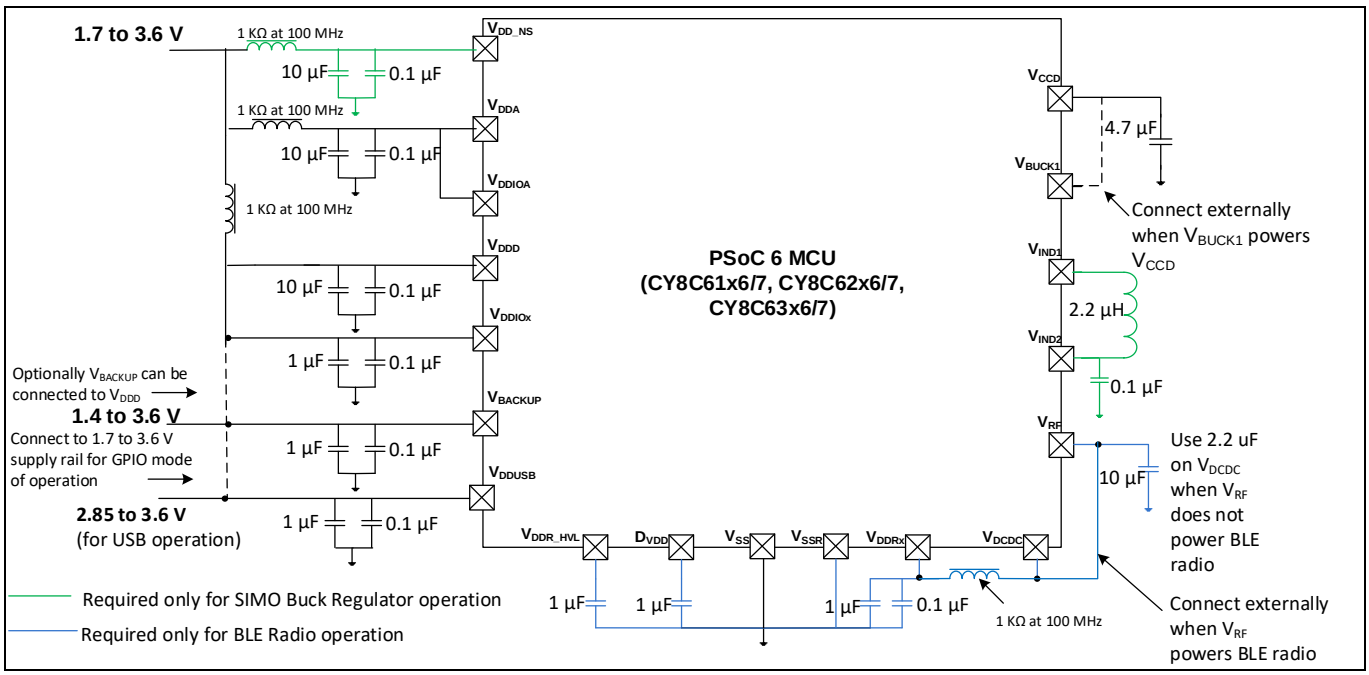

Figure 1 Power System Connections

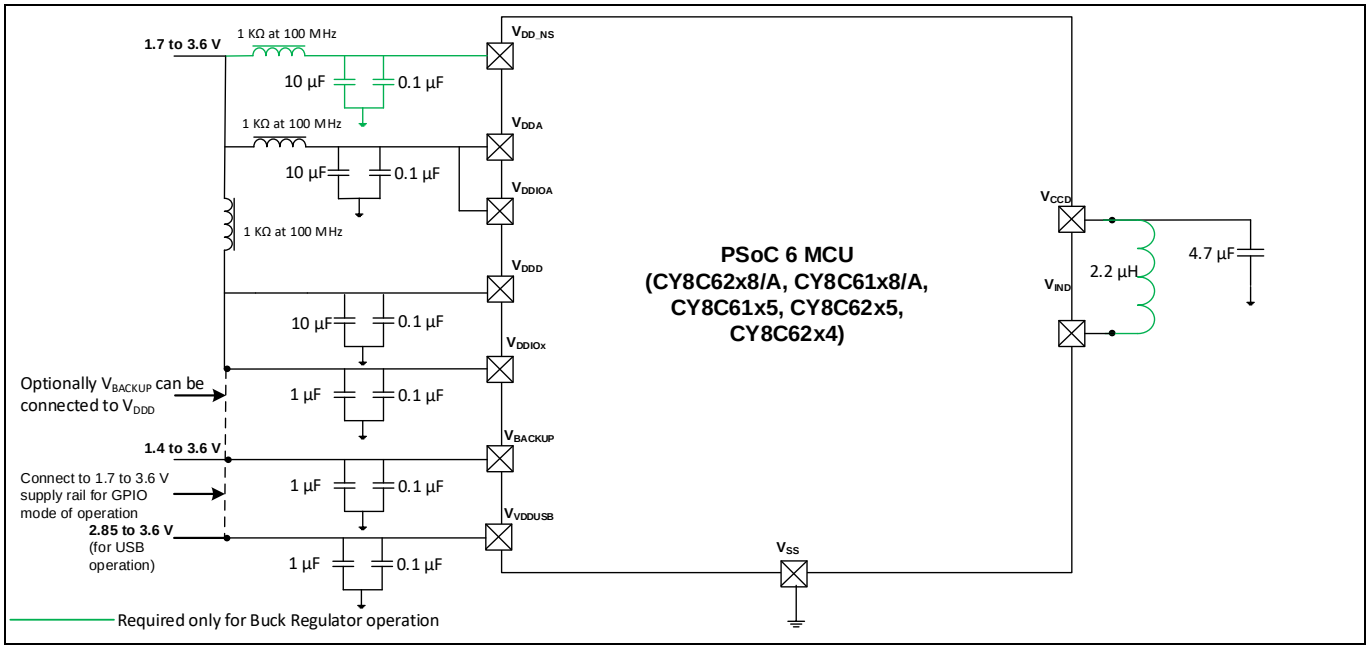

Figure 2 Power System Connections

You can use a single power supply rail for digital power and analog power, which helps to simplify the power design in your board. However, to get a better analog performance in a mixed-signal circuit design, use separate power supply rails for the digital power and the analog power. It is recommended to isolate the rails using ferrite beads. For more mixed-signal circuit design techniques, see **AN57821 – PSoC Mixed-Signal Circuit Board Layout Considerations**.

Proper use and layout of capacitors and ferrite beads help to improve the EMC performance. For more information, see **AN80994 – Design Considerations for Electrical Fast Transient (EFT) Immunity**.

The Cypress PSoC 6 MCU kits (like **CY8CKIT-062-BLE, CY8CKIT-062-WIFI-BT, CY8CPROTO-062-4343W, CY8CPROTO-062S3-4343W** and so on) provide schematics and bills of material (BOMs) that give good

examples of how to incorporate PSoC 6 MCU into board schematics. Also, see the respective device **datasheets** for package specific power supply considerations. For more information, see **Related Documents**.

3.3 PMIC Controller

PSoC 6 MCU supports a PMIC controller in the backup domain. The PMIC controller can be used to enable/disable the power supplies to PSoC with the backup domain (VBACKUP) running from another supply, typically from a coin cell or super capacitor. PSoC 6 MCU provides configurable wakeup sources either by an RTC alarm or by a GPIO input pin. To use the PMIC controller, ensure that the following are present in hardware:

The selected PMIC supports an active HIGH PMIC enable signal that supports the input levels in the VBACKUP voltage range.

An independent supply (other than the PMIC output) such as a coin cell or super capacitor powers VBACKUP.

The Wakeup_OUT (P0[5]) pin is connected to the PMIC enable signal with an optional pull-up resistor to VBACKUP.

If the RTC alarm is used as a wakeup source, ensure that an external 32.768-kHz crystal or signal clocks the RTC.

If an external pin (P0[4]) is used as a wakeup source, the signal should be driven externally i.e., a necessary pull-down resistor should be connected externally because the wakeup logic is active HIGH. The Wakeup_IN pin is a High-Z digital input to PSoC.

Figure 3 illustrates using a PMIC controller with a PSoC 6 MCU design.

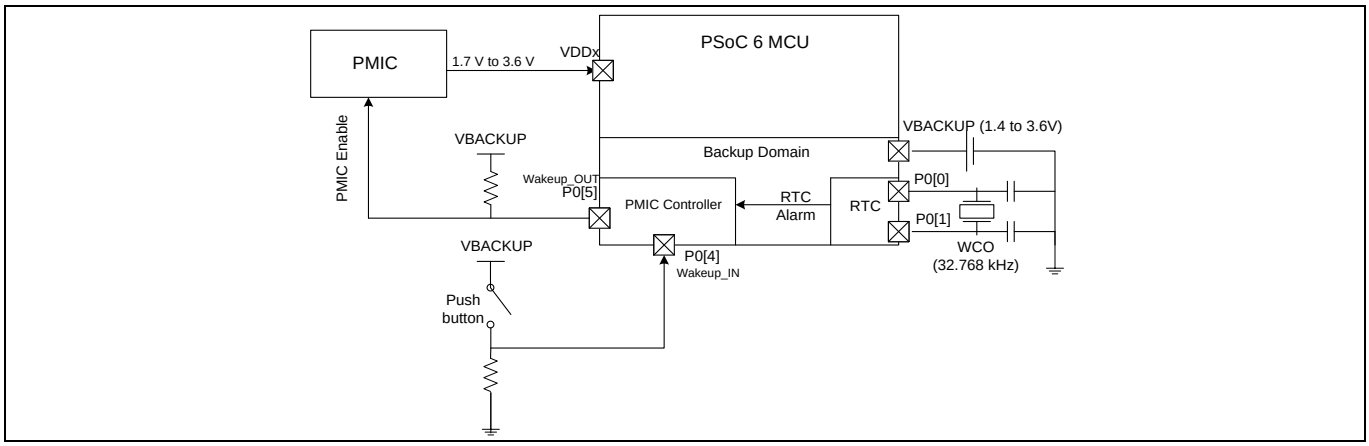

Figure 3 Using PMIC Controller

3.4 Power Ramp-Up and Sequencing Considerations

VDDD, VBACKUP, VDDIO, and VDDA do not have any sequencing limitation and can establish in any order. However, VDDIO should be greater than or equal to VDDA when using CapSense in the design. CapSense signals can switch between VSSA and VDDA, thus requiring VDDIO to support the swing to VDDA. In addition, the presence of VDDA without VDD or VDDD can cause some leakage from VDDA. However, it will not drive any analog or digital output. All the VDDA pins in packages that offer multiple VDDA supply pins must be shorted externally on the PCB. The maximum allowed voltage ramp rate for any power pin is 100 mV/µs in Active power mode and the allowed ramp is 20 mV/µs in Deep Sleep power mode.

3.5 Device Power Settings

You can use Cypress' development environments, either PSoC Creator or ModusToolbox IDE, to manage device power settings. PSoC Creator automatically configures Components for optimal performance for the voltages

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applied to the power pins. To do so, it needs to know the value of these voltages. The **System** tab in the PSoC Creator project's Design-Wide Resources (DWR) window is used for this purpose. To open the DWR window, double-click the *.cydwr* file in the project navigator, as **Figure 4** shows.

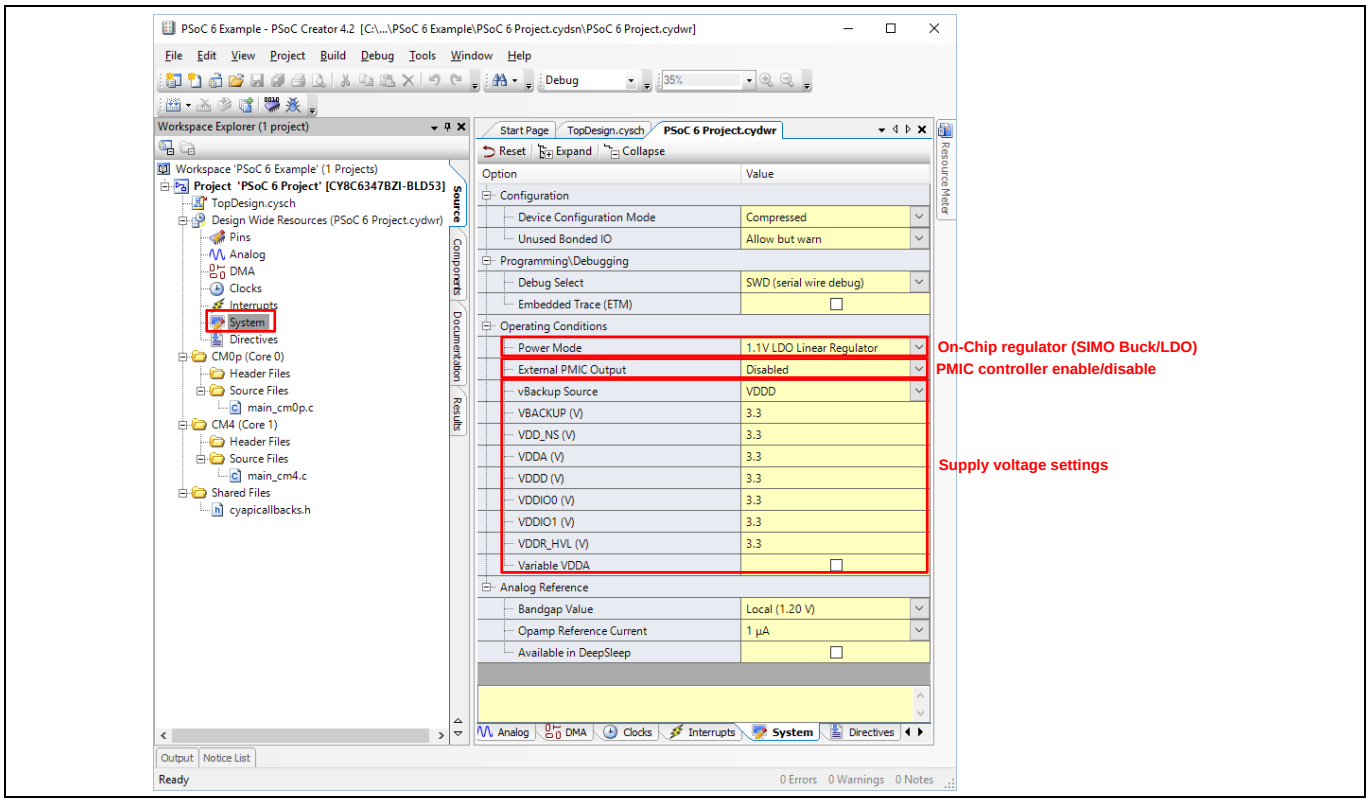

Figure 4 Device Power Settings in PSoC Creator

Figure 5 shows how to manage device power settings using the Device Configurator from ModusToolbox IDE.

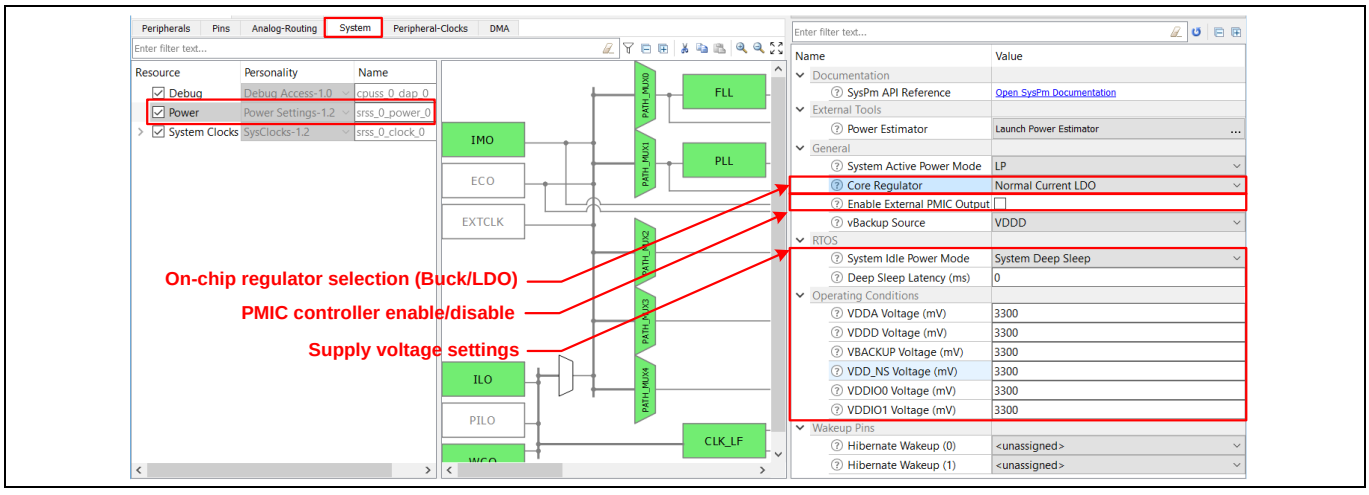

Figure 5 Device Power Settings in ModusToolbox

3.6 Thermal Considerations

Thermal considerations are important in the hardware design processes, such as package selection and PCB layout. PSoC 6 MCU targets low-power applications, as it consumes no more than 0.2 W. The maximum power consumption is so low that thermal considerations are not necessary.

3.7 eFuse Programming

PSoC 6 MCU supports a 1024-bit One-Time-Programmable (OTP) eFuse. Each bit of the eFuse can be blown independently. See the "Nonvolatile Memory Programming" chapter of **PSoC 6 MCU: Architecture TRM** for details. While specific system calls are used to blow the eFuse bits, the VDDIO0 (or VDDIO if only one VDDIO is present in the package) supply of the device should be set to 2.5-V (±5%) for successfully programming/blowing the eFuse bits. The programming voltage of eFuse block is connected to V_{DDIO0} internally. Typically, eFuse programming is done only once before deployment. You can either blow the eFuse bits in the device before putting it on the hardware or make a provision to connect 2.5-V to VDDIO0 in the hardware for eFuse programming. eFuse programming is supported in PSoC Programmer 3.27 or later.

4 Clocking

The PSoC 6 MCU clocking system includes three internal clock sources: 8-MHz internal main oscillator (IMO), 32-kHz internal low-speed oscillator (ILO), and precision 32-kHz internal low-speed oscillator (PILO). Note that that PILO is not available in CY8C61x8/A, CY8C62x8/A, CY8C61x5, CY8C62x5, and CY8C62x4 devices. IMO has an accuracy of ±2 percent across voltage and temperature. ILO has an accuracy of ±10 percent. PILO has an accuracy of ±2 percent, which can be calibrated to ±500 ppm with a high-accuracy clock source.

Besides the internal clock sources, PSoC 6 MCU has three external clock sources: External clock (EXTCLK) generated using a signal from an I/O pin, external 16-35 MHz crystal oscillator (ECO), and external 32.768-kHz watch crystal oscillator (WCO).

The BLE radio in PSoC 6 MCU includes an additional crystal oscillator (32 MHz). An external 32 MHz crystal is mandatory for proper BLE operation. The clock generated by this oscillator block is available for other blocks inside PSoC 6 MCU. This clock is routed as the AltHF clock in the clocks settings discussed in **Clock Settings**. Note that this clock is available only when the BLE radio is powered. See **AN95089 - PSoC® 4 BLE Crystal Oscillator Selection and Tuning Techniques** for details on selecting and tuning WCO/ECO crystals for BLE applications.

For more details, see the Clocking chapter of the **PSoC 6 MCU: Architecture TRM**.

4.1 Clock Settings

You can use either of the development environment to manage clocks.

Using PSoC Creator, you can configure sources and paths for High Frequency Clock (HFCLK) and Low Frequency Clock (LFCLK). The **Source Clocks** tab allows you to configure various clock sources and the **FLL/PLL** tab allows you to configure the (frequency-locked loop) FLL and phase-locked loop (PLL) inside PSoC 6 MCU. Switch to the **Clocks** tab in the DWR window, and double-click any row in the table of clocks or click the **Edit Clock** button to open the **Configure System Clocks** dialog, as **Figure 6** shows.

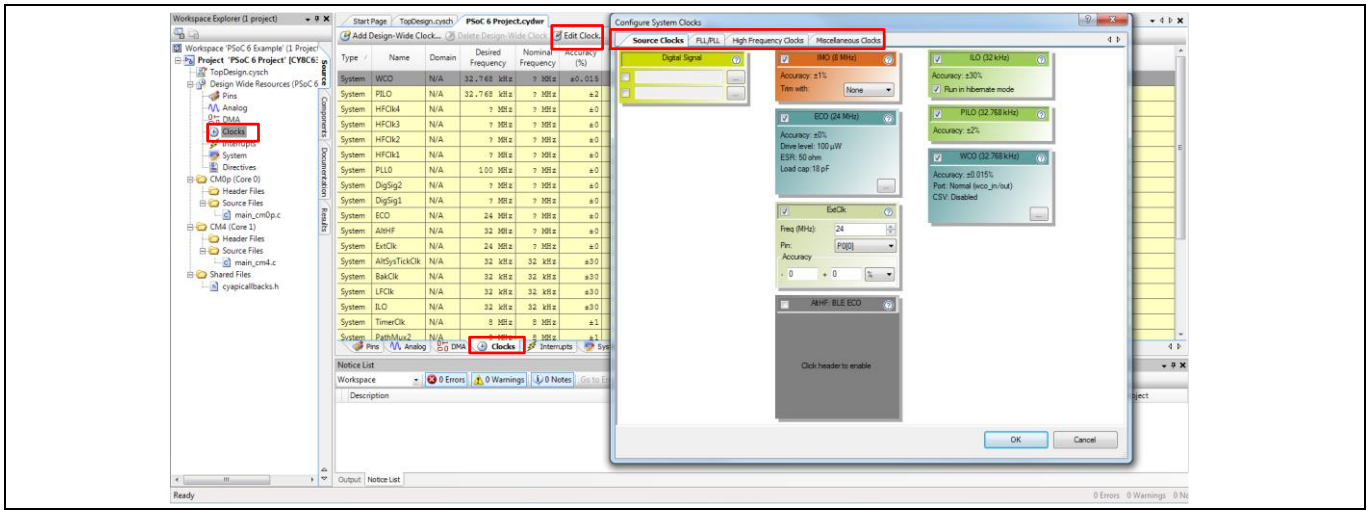

Figure 6 Clock Settings in PSoC Creator

Clocking

In ModusToolbox IDE, the **System** tab in the **Device Configurator** (*design.modus*) provides the options for configuring the clocks. **Figure 7** shows how to configure system clocks using ModusToolbox.

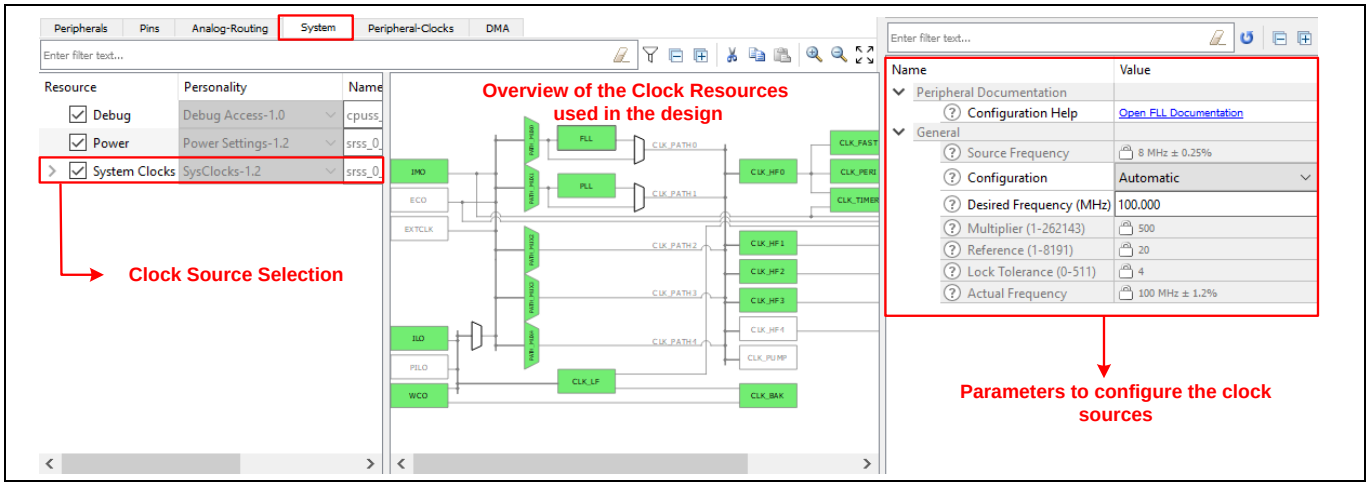

Figure 7 Clock Settings in ModusToolbox

4.1.1 Crystal Oscillators

4.1.1.1 ECO

The ECO block requires an external crystal (16 MHz to 35 MHz) connection to appropriate pins as shown in **Figure 8**.

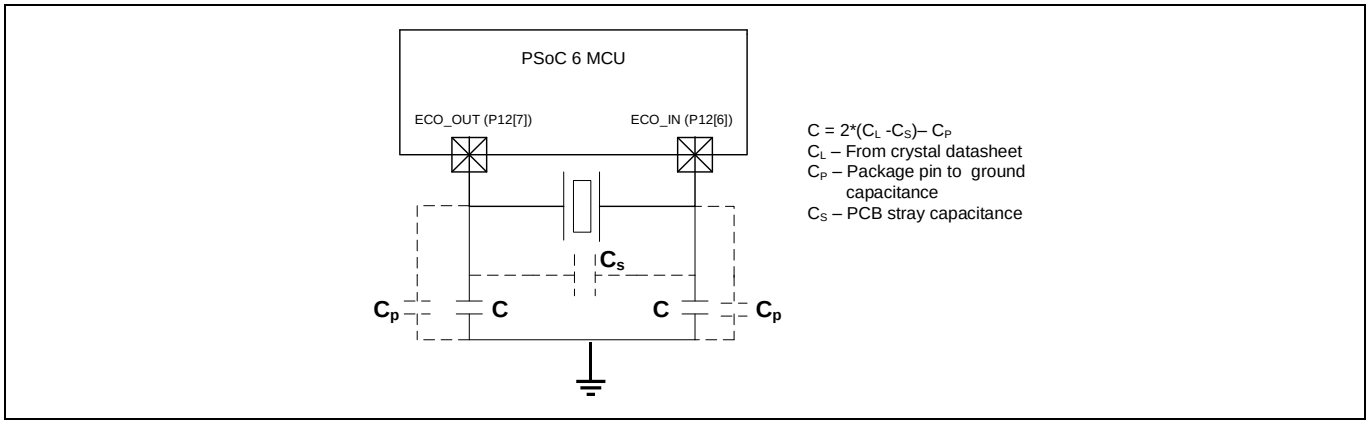

Figure 8 ECO Connections

In PSoC 6 MCU, the external crystal connects to Port 12[6] and 12[7]. When the ECO is enabled, the corresponding I/O pins are configured appropriately by both PSoC Creator and ModusToolbox IDE to interface the external crystal.

Crystal manufacturers typically provide numerical values for parameters, namely the maximum drive level (DL), the equivalent series resistance (ESR), and the parallel load capacitance (C_L). These data should be entered in the Configure ECO settings to configure the ECO appropriately. The external load capacitors for the ECO are calculated as:

$$C = 2 * (C_L - C_S) - C_P$$

where C_L – Crystal load capacitor as per the crystal datasheet

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C_S – PCB stray capacitance. A well-designed PCB to minimize the stray capacitance includes a grounded copper wire between the crystal input and output wires.

C_P – Package pin to ground parasitic capacitance (typical value of 3 pF. See the device **datasheet** for more details on pin parasitic capacitance).

It should be noted that the ECO available as part of the BLE radio has its own pins (XI and XO). You can add the load capacitor, crystal accuracy, and startup time details in the AltHF clock configure window as shown in **Figure 9**. External load capacitors for the BLE ECO are not required.

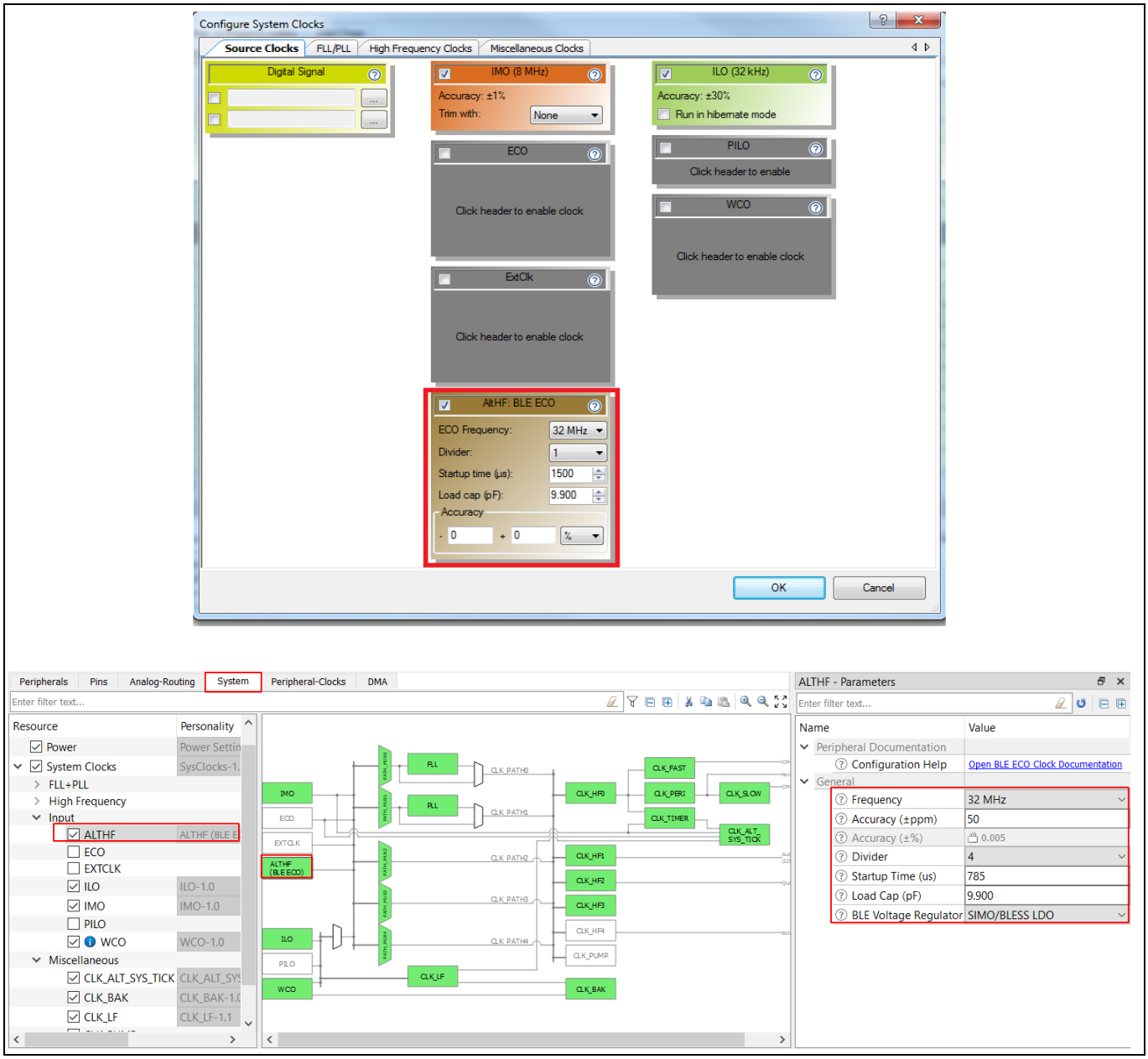

Figure 9 Configuring BLE ECO in PSoC Creator and ModusToolbox

4.1.1.2 WCO

The WCO block requires an external 32.768-kHz crystal along with input and output load capacitors for proper operation. This is shown in **Figure 10**.

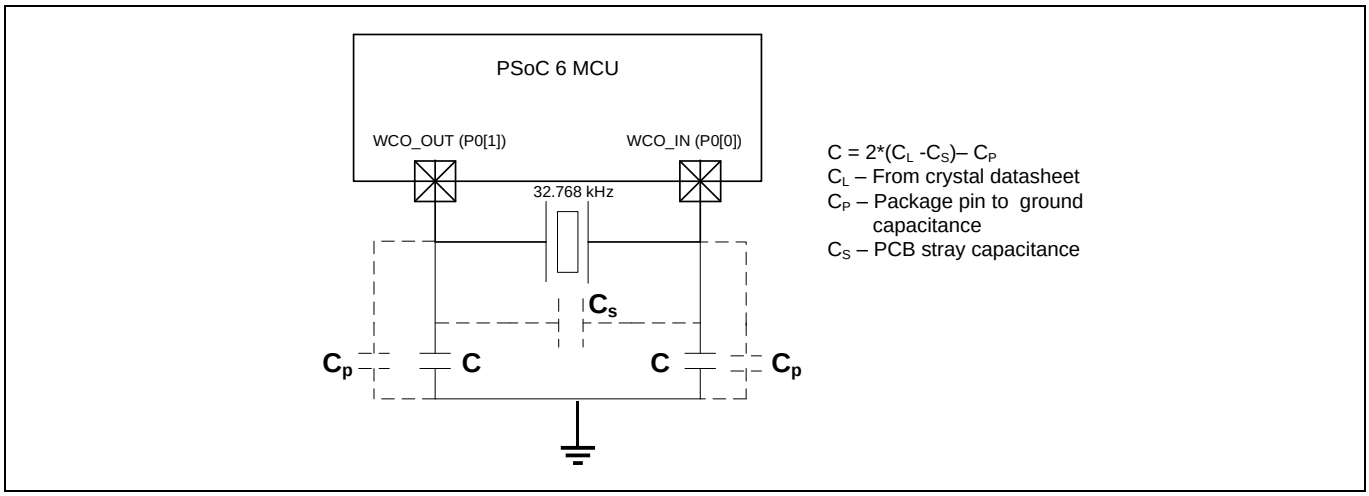

Figure 10 WCO Connections

In addition, the WCO block can be bypassed altogether and a 32.768-kHz external sine wave can be directly fed to the WCO_OUT pin. In this configuration, the WCO_IN pin should be left floating. To bypass the WCO using PSoC Creator, enable WCO in **Configure System clocks** window and set the **Clock port** radio button in the **Configure WCO** dialog box to **Bypass (External sine wave)** as shown in **Figure 11**. In ModusToolbox, enable WCO in the **Device Configurator** (*design.modus*) and set the Clock Port to **Bypass (External sine wave)** as shown in **Figure 12**. This will configure the WCO block to route a 32.768-kHz clock (sine wave signal) on WCO_OUT pin to RTC and LFCLK. Make sure that the WCO_IN pin is not used and left floating in the design.

The external load capacitors for the WCO are calculated as:

$$C = 2 * (C_L - C_S) - C_P$$

where C_L – Crystal load capacitor as per the crystal datasheet

C_S – PCB stray capacitance. A well-designed PCB to minimize the stray capacitance includes a grounded copper wire between the crystal input and output wires.

C_P – Package pin to ground parasitic capacitance (typical value of 3 pF. See the device **datasheet** for more details on pin parasitic capacitance).

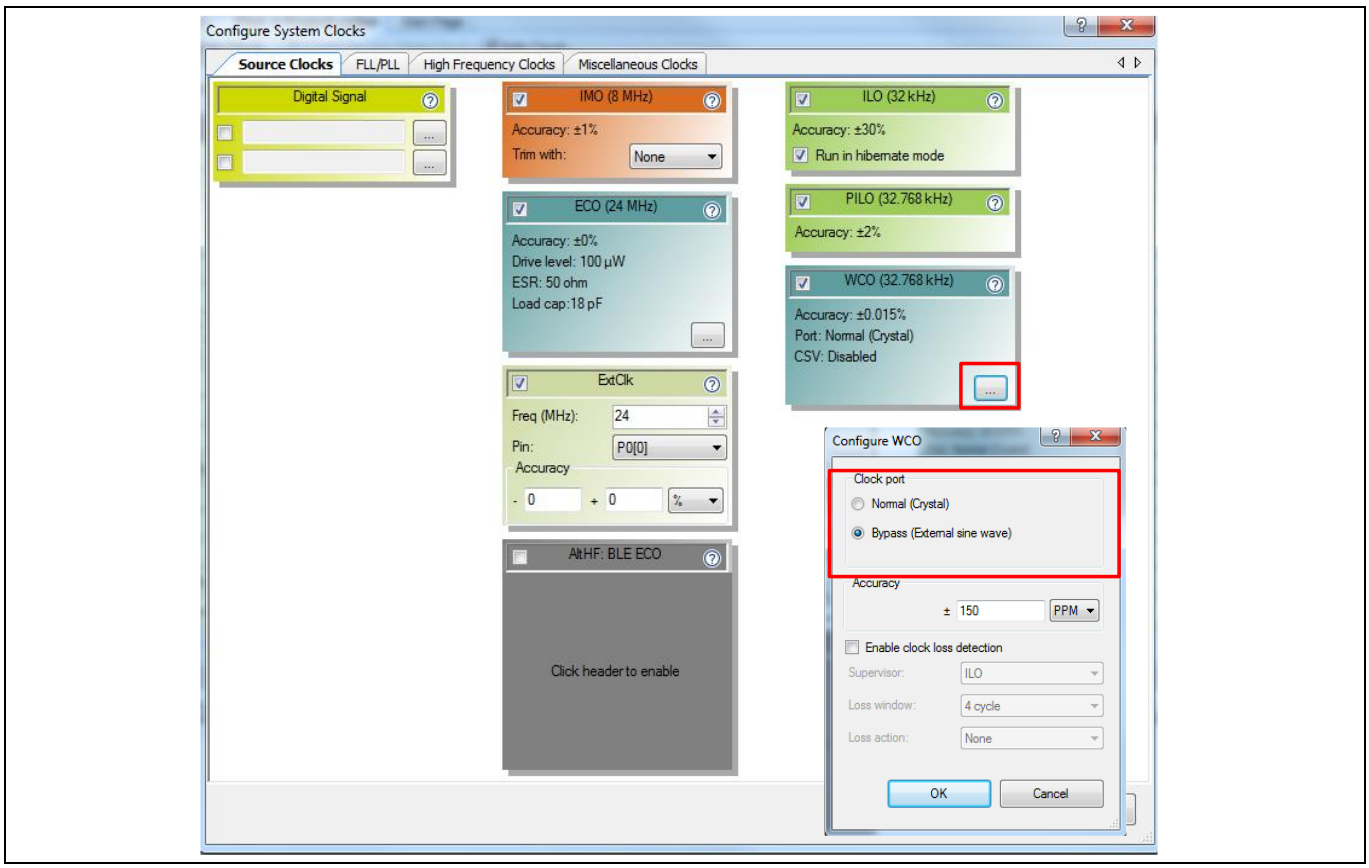

Figure 11 Configure WCO Option in PSoC Creator

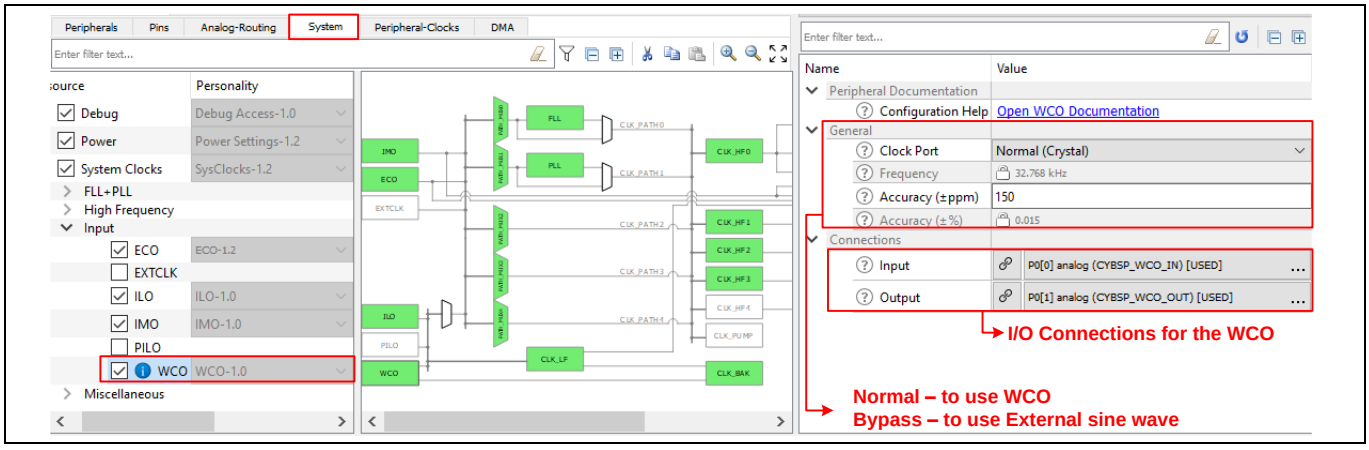

Figure 12 Configure WCO in ModusToolbox

4.1.2 External Clock

In PSoC 6 MCU, a 0–100 MHz-range clock can be connected to an EXT_CLK pin (P0[0] or P0[5]) and routed to various blocks inside PSoC. This is shown in **Figure 13** and **Figure 14**. When a pin is selected for receiving the external clock, it is automatically configured and reserved for EXTCLK by both PSoC Creator and ModusToolbox. PSoC expects a 0-100 MHz-range digital signal with a 45-55% duty cycle on the EXTCLK input.

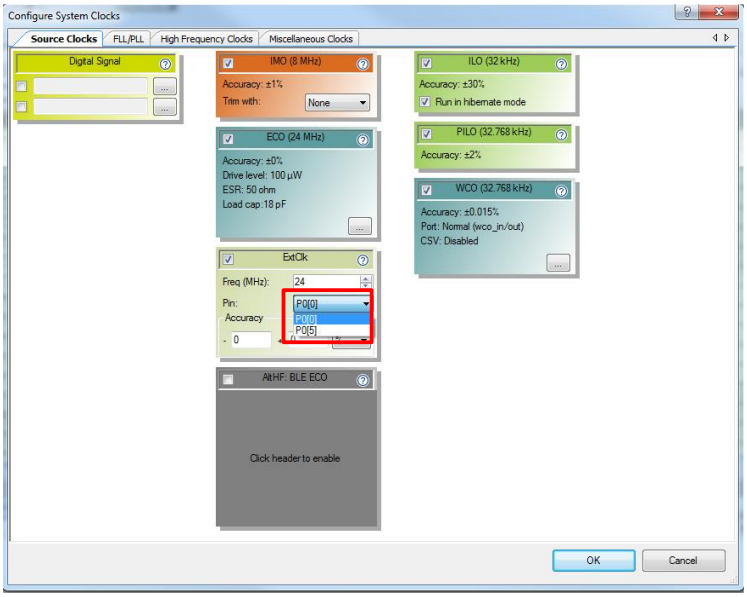

Figure 13 Routing External Clock in PSoC Creator

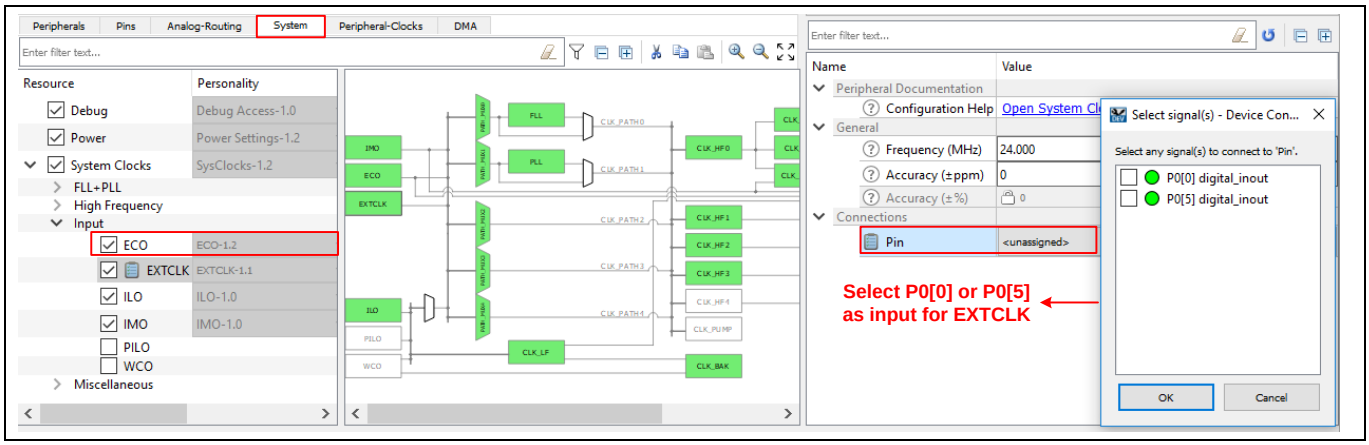

Figure 14 Routing External Clock in ModusToolbox

In addition, the output of CLK_HF4 can be routed out through P0[0] or P0[5]. Note that both the EXTCLK input and CLK_HF4 output use the same signal path. Hence only one of them can be active at a time. To use P0[0] or P0[5] as EXTCLK input, the HSIOM setting should be set to SRSS_EXT_CLK and drive mode should be configured as high impedance digital with input buffer enabled. To use the pin as CLK_HF4 output, the HSIOM setting should be set to SRSS_EXT_CLK and drive mode should be configured as strong drive with input buffer disabled.

Clocking

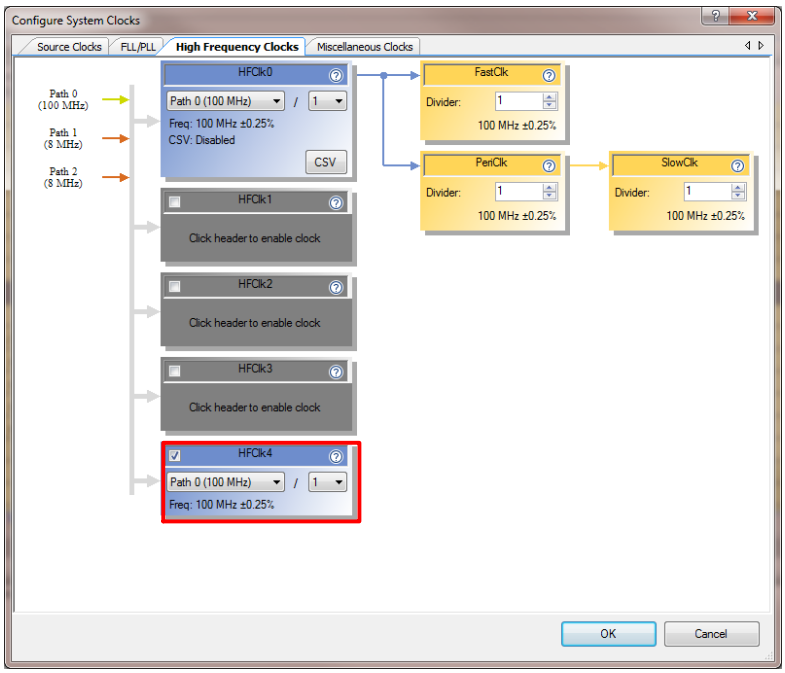

Figure 15 CLK_HF4 Option in PSoC Creator

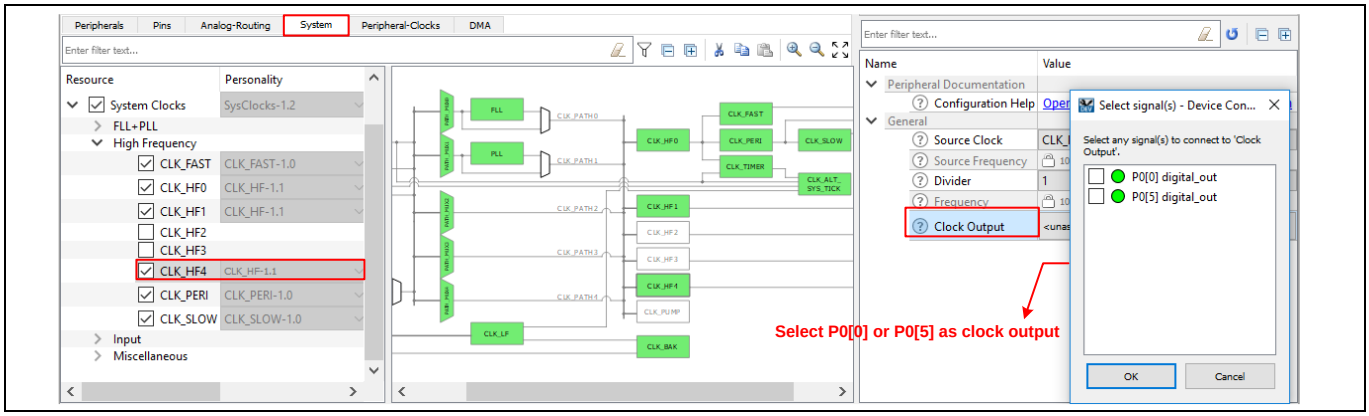

Figure 16 CLK_HF4 Option in ModusToolbox

5 Reset

PSoC 6 MCU has a reset pin, XRES, which is active LOW. You have to externally pull up the XRES pin to VDDD via a 4.7-kΩ resistor. This will make sure that the XRES pin is not left floating in the design and the device can function properly. You can also connect a capacitor (typically 0.1 µF) to the XRES pin, as **Figure 17** shows, to filter out glitches and give the reset signal better noise immunity. Optionally, if PSoC is controlled by an external host, the XRES pin can be directly driven by the host.

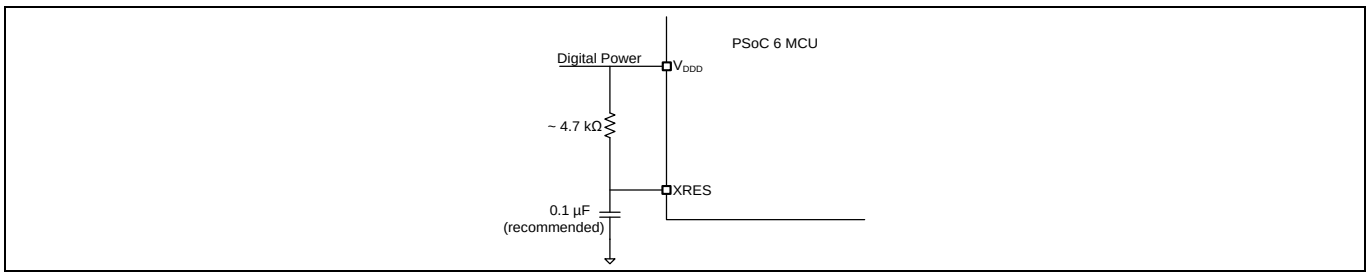

Figure 17 XRES Pin Connection

6 Programming and Debugging

The PSoC 6 MCU Program and Debug interface provides a communication gateway for an external device to perform programming or debugging. The external device can be a Cypress-supplied programmer and debugger or a third-party device that supports programming and debugging. The serial wire debug (SWD) or the JTAG interface can be used as the program/debug protocol between the external device and PSoC 6 MCU. In addition, PSoC 6 MCU supports Arm Embedded Trace Macrocell (ETM) on the Cortex-M4 CPU.

6.1 SWD

For SWD programming or debugging, you can use the onboard programmer/debugger of PSoC 6 MCU Kits (KitProg), or connect PSoC BLE 6 to an external debugger such as **CY8CKIT-002 MiniProg3** via any connector supported by the debugger. MiniProg3 supports a 10-pin and a 5-pin connector for SWD programming and debugging (see **Figure 18**). In addition to SWD, PSoC 6 MCU supports single-wire viewer (SWV) interface defined by Arm. The SWV interface is used for program and data monitoring, where the firmware may output data in a method similar to “printf” debugging on PCs, using a single pin. The SWV support in MiniProg3 is available only on the 10-pin header (see **Figure 19**).

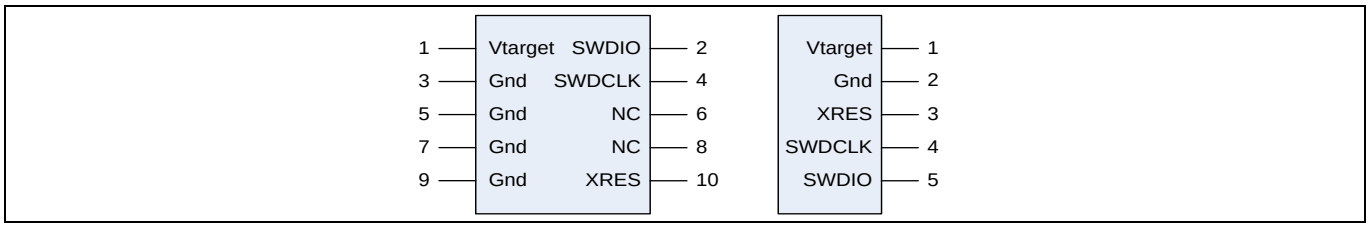

Figure 18 SWD Connector Pin Maps for MiniProg3

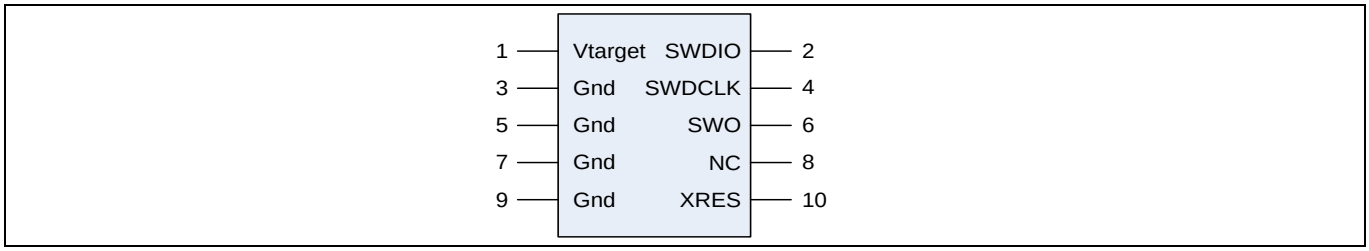

Figure 19 SWD+SWV Connector Pin Maps for MiniProg3

Figure 20 shows the SWD and SWV connections in PSoC 6 MCU.

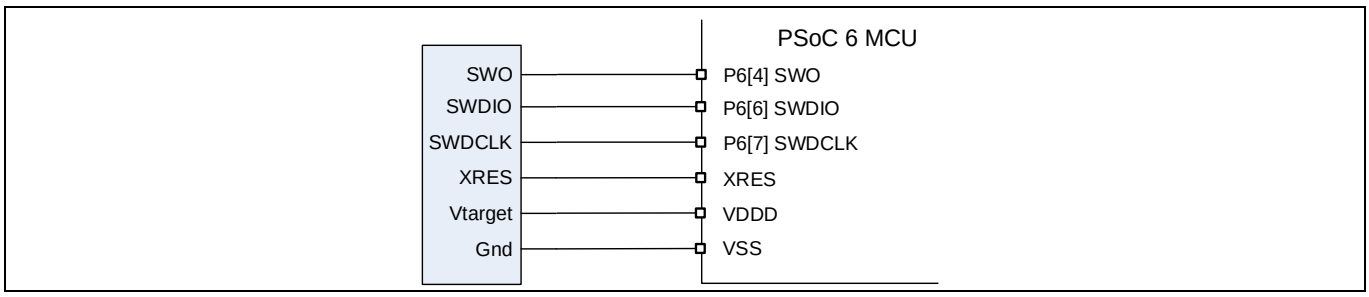

Figure 20 SWD/SWV Connections to PSoC 6 MCU

6.2 JTAG

For JTAG programming and debugging, external debuggers like MiniProg3 or ULINK can be used. Both 4-wire and 5-wire JTAG programming is supported in PSoC 6 MCU. **Figure 21** shows the JTAG connections to PSoC 6 MCU. MiniProg3 supports 4-wire JTAG programming (see **Figure 22**) on the 10-pin connector.

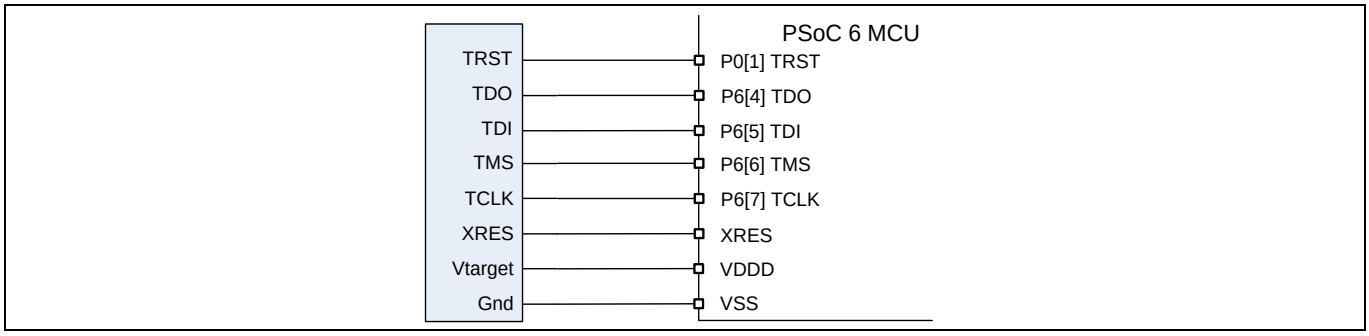

Figure 21 JTAG Connections to PSoC 6 MCU

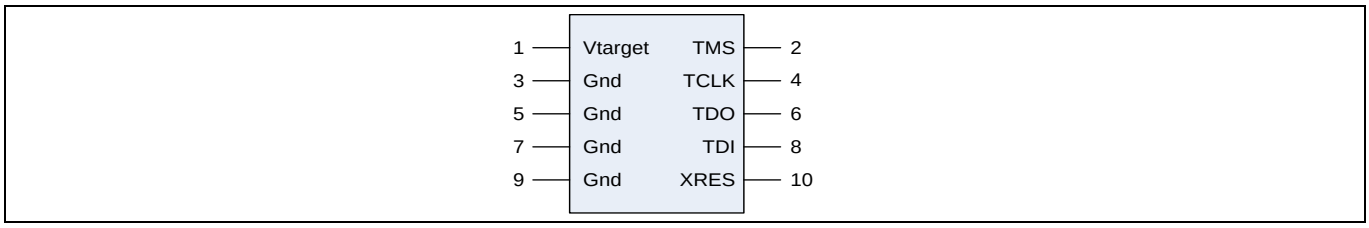

Figure 22 JTAG Connections in MiniProg3 10-pin Header

6.3 ETM

The Cortex-M4 CPU in PSoC 6 MCU supports ETM. Any ETM trace viewers can be used with PSoC 6 MCU. ETM trace connections to PSoC 6 MCU are shown in **Figure 23**.

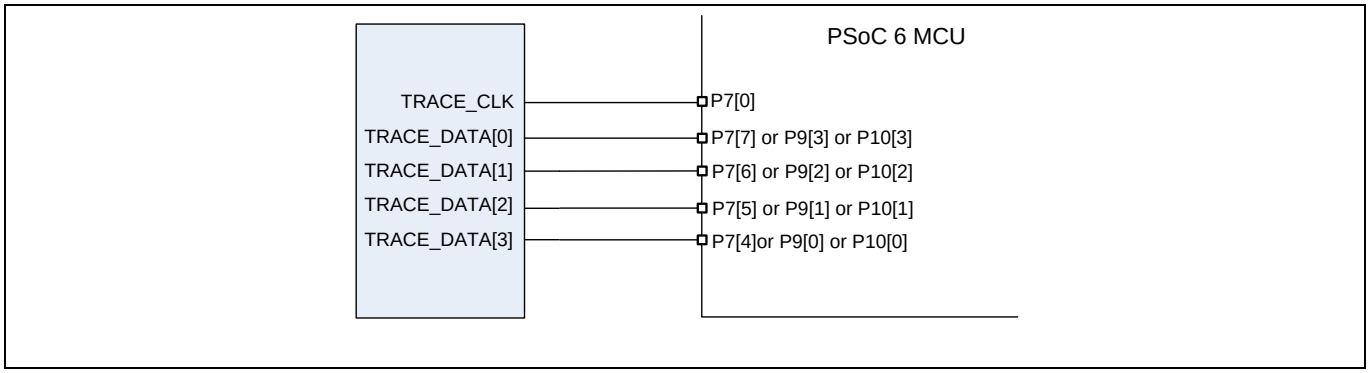

Figure 23 ETM Connections to PSoC 6 MCU

6.4 Debug Select

The SWD and JTAG pins could be used for other functionality when the devices are not being programmed; see the device **datasheet** for the possible functionality details. However, if you need to use SWD/JTAG pins for run-time debugging, select **SWD/4-wire JTAG/5-wire JTAG**, instead of **GPIO**, from the **Debug Select** pull-down list in the **System** tab of the DWR window, as **Figure 24** shows. **Figure 25** shows the corresponding debug settings in ModusToolbox IDE. In this case, the pins cannot be used for other functionality any longer. Similarly, if SWV

Programming and Debugging

and/or ETM trace is required, the appropriate option can be selected in the Debug Select dropdown (**SWD+SWV**) and checking the **Embedded Trace (ETM)** checkbox.

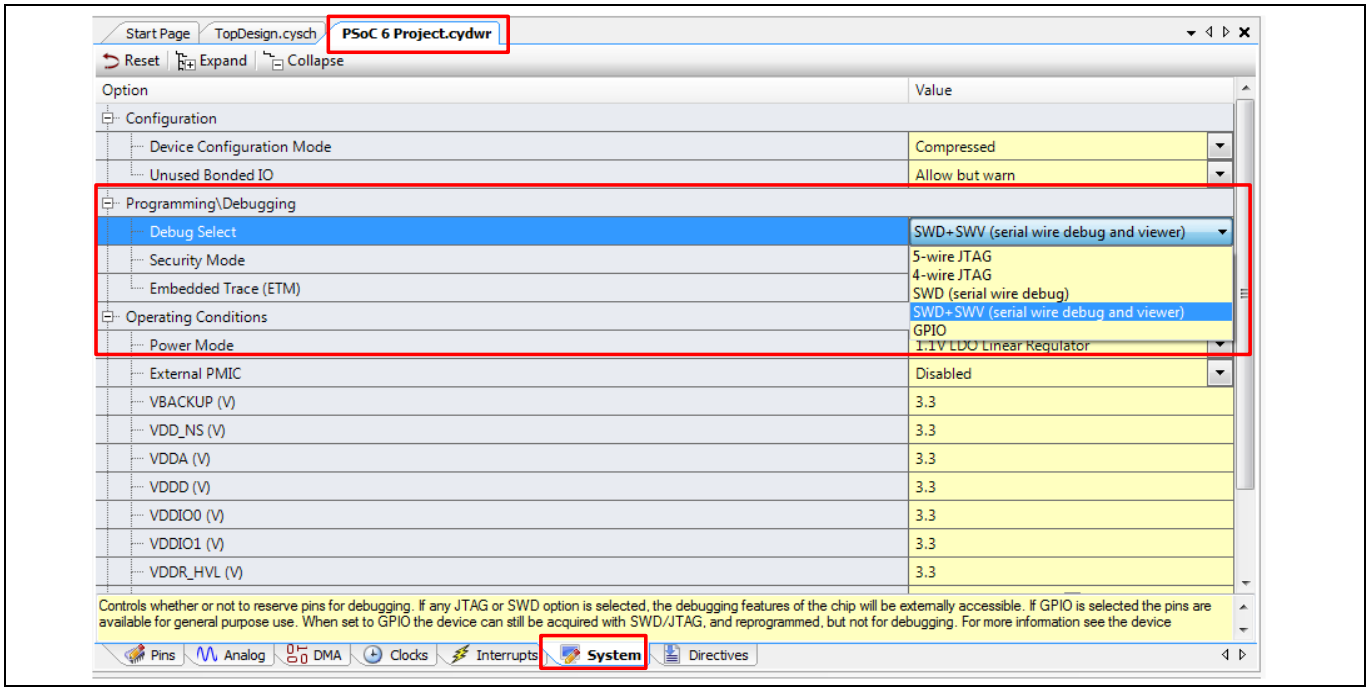

Figure 24 PSoC Creator Debug Settings

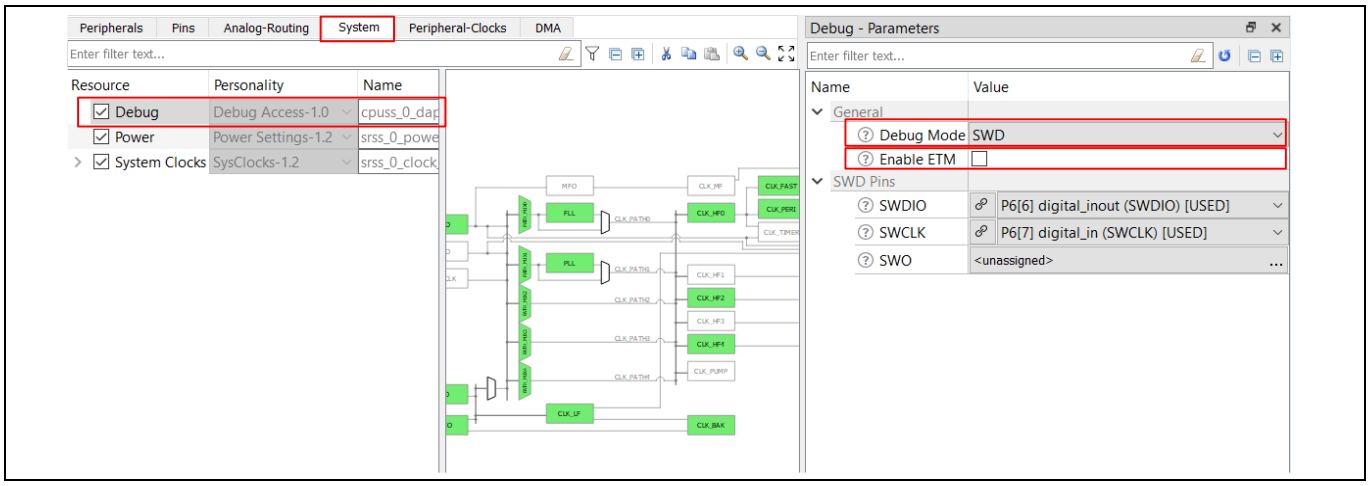

Figure 25 ModusToolbox Debug Settings

7 GPIO Pins

PSoC 6 MCU provides flexible GPIO pins. All GPIO pins can be controlled by firmware. Most of them also have alternative connections to PSoC 6 MCU peripherals. Different peripherals have different dedicated or fixed pins for their terminals. You get the best performance when a peripheral is connected to its own dedicated pin or pins. However, for flexibility, you can connect the peripheral to other pins at the cost of using some internal routing resources. The flexibility of PSoC devices and the capability of its I/O to route most signals to most pins greatly simplify circuit design and board layout. If a peripheral has fixed pins, then you can connect it only to those pins.

7.1 I/O Pin Selection

When you design a hardware system, based on PSoC 6 MCU, you should assign the GPIO pins in the following sequence as shown in **Table 4**. See the device **datasheet** to determine whether the peripheral block listed in **Table 4** is supported by your PSoC 6 MCU device.

Table 4 I/O Pin Selection Guide

Block	Pin Name	Port#[Pin#]	Fixed/ Dedicated	Remarks
System Function Pins				
Run-time Debug			Fixed	If you need run-time debugging, trace, or SWV support, select the appropriate setting in the System settings explained in **Debug Select** . The selection will automatically lock the required IOs for the purpose.
External Crystal Oscillator (ECO)	ECO_IN	P12[6]	Fixed	External crystal frequency range: (16 MHz – 35 MHz); Use this ECO when BLE ECO is not used or the required crystal frequency is not 16/32 MHz.
	ECO_OUT	P12[7]	Fixed	
Watch Crystal Oscillator (WCO)	WCO_IN	P0[0]	Fixed	If you need a highly accurate and low-frequency clock for RTC or Deep Sleep wakeup purpose, use the WCO block with an external 32.768-kHz crystal or clock. Note that the WCO block is present in the device's backup domain and is available, even when the VDDD of the device is removed (VBACKUP supply should be present).
	WCO_OUT	P0[1]	Fixed	
Wakeup (Hibernate and PMIC controller)	HIB_WAKEUP	P0[4] or P1[4]	Fixed	The hibernate wakeup pin is used to wake PSoC 6 MCU from the hibernate mode. To wake up PMICs that supply V_{DDD}, use the WAKEUP_OUT pin. The PMIC wakeup signal can be generated from internal RTC alarms or an input on P0[4] (WAKEUP_IN).
	WAKEUP_OUT	P0[5]	Fixed	
	WAKEUP_IN	P0[4]	Fixed	
External Clock	EXT_CLK	P0[0] or P0[5]	Fixed	Configure the pin as input (high impedance digital) for receiving the external clock.

GPIO Pins

Block	Pin Name	Port#[Pin#]	Fixed/ Dedicated	Remarks
				Configure the pin as output (strong drive with input buffer disabled) for routing internal clock (CLK_HF4) out.
Analog Pins				
Low-Power Comparator	LPCOMP.IN_P	P5[6], P6[2]	Dedicated	PSoC 6 MCU has two low-power comparators that can work in all system power modes.
	LPCOMP.IN_N	P5[7], P6[3]	Dedicated	
Opamp	Vplus Input	P9[0], P9[6], P9[5], P9[7]	Dedicated	PSoC 6 MCU has up to two opamps. These opamps are operational in Deep Sleep power mode and can be used for buffering, pre-amplifier, voltage follower and sample and hold operations by peripherals like SAR ADC and CTDAC. Note that this feature is not available in CY8C61x8/A, CY8C62x8/A, CY8C61x5, and CY8C62x5 devices. Note that the availability of pins depends on the selected PSoC 6 MCU device. See the respective device **datasheet** for the pin availability. For more details, see the Continuous Time Block mini (CTBm) chapter in **PSoC 6 MCU Architecture TRM**.
	Vminus Input	P9[1], P9[4]	Dedicated	
	Output	P9[2], P9[3]	Dedicated	
CapSense	CMOD	P7[1] or P7[2] or P7[7]	Fixed	For the self-capacitance method, connect a modulator capacitor to the CMOD pin and reservoir capacitor to the CSH_TANK pin. For the mutual-capacitance method, connect two integrating capacitors CINT1 and CINT2 pins. See the CapSense sections for details.
	C_{SH_TANK}	P7[1] or P7[2] or P7[7]	Fixed	
	CINT1	P7[1]	Fixed	
	CINT2	P7[2]	Fixed	
SAR ADC	SAR ADC pins	P10[0]-P10[7]	Dedicated	Port 10 has the dedicated connection to SAR ADC. You can route the ADC connection to other ports using AMUX A and AMUX B. Port 9 is the preferred port after port 10 because connection to other ports involve additional switch resistance in their paths.
Digital Pins				
Timer/Counter Pulse-Width Modulator (TCPWM)	TCPWM pins	See the device **datasheet**	Dedicated	PSoC 6 MCU has up to 32 TCPWM blocks with each block having two complimentary PWM signals. All these signals are routed to dedicated GPIO pins.

GPIO Pins

Block		Pin Name	Port#[Pin#]	Fixed/ Dedicated	Remarks
Serial Communication Block (SCB)		SCB pins	See the device **datasheet**	Fixed	CY8C61x6/7, CY8C62x6/7, and CY8C63x6/7 devices have up to 9 SCBs out of which 8 SCBs can be configured as SPI, I^2C, or UART. One SCB supports only I^2C or SPI mode and is available in Deep Sleep power mode. CY8C62x8/A devices have up to 13 SCBs out of which 8 SCBs can be configured as SPI, I^2C, or UART, four SCBs can be either UART or I^2C, and one SCB is operational in Deep Sleep supporting I^2C or SPI mode. CY8C62x4, CY8C61x5, and CY8C62x5 devices have 7 SCBs out of which 6 SCBs can be configured as SPI, I^2C, or UART and one SCB is operational in Deep Sleep supporting I2C or SPI mode.
Serial Memory Interface (SMIF)		SMIF pins	P11[0]-P11[7] P12[0]-P12[4]	Fixed	The SMIF block uses fixed pins. See the **SMIF** section and device **datasheet** for details on these pins.
Secure Data Host Controller (SDHC)		SDHC pins	See the device **datasheet**	Fixed	The SDHC block uses fixed pins. See the **SDHC** section and device **datasheet** for details on these pins.
Controller Area Network (CAN FD)		CAN pins	P5[0], P5[1]	Fixed	CAN with Flexible Data rate (CAN FD). CAN FD block is available in CY8C61x5, CY8C62x5, and CY8C62x4 devices only. See the device **datasheet**.
Segment LCD		Com and Seg pins	Routing is available to almost all the GPIO pins	-	Segment LCD drive block is available in CY8C61x5, CY8C62x5, and CY8C62x4 devices only. This block can operate in Deep Sleep power mode. See the device **datasheet**.
Audio Block	PDM	PDM_DATA PDM_CLK	See the device **datasheet**	Fixed	The Audio subsystem consists of an I2S block and two PDM channels. CY8C62xA devices have two I2S blocks and two PDM channels See the **Audio Subsystem** section and device datasheet for details on these pins
	I2S	I2S_TX_SCK I2S_TX_WS I2S_TX_SDO I2S_RX_SCK I2S_RX_WS I2S_RX_SDO I2S_MCLK	See the device **datasheet**	Fixed	

*Note: For some devices in the PSoC 6 MCU family, simultaneous GPIO switching with unrestricted drive strengths and frequency can induce noise in on-chip subsystems affecting CapSense and ADC results. For more details. see the Errata section of the corresponding device **datasheet**.*

8 Analog Module Design Tips

8.1 CapSense

In the self-capacitance mode, you can connect any PSoC 6 MCU pin to a CapSense sensor except **CMOD** (or **C_MOD**) pin, which is reserved for the modulating capacitor (C_{MOD}) function. In PSoC 6 MCU, CMOD should be connected to P7[1] or P7[2] or P7[7]. When you need to use a shield electrode for waterproofing or proximity features, you may also need to reserve the **CTANK** (or **C_SH_TANK**) pin for the tank capacitor, C_{SH_TANK}. In PSoC 6 MCU, C_{SH_TANK} can be connected to P7[1] or P7[2] or P7[7]. If the parasitic capacitance of the shield is less than 200 pF, it is optional to use C_{SH_TANK}; otherwise, it is recommended to use the tank capacitor for improved water tolerance. The value for C_{MOD} is usually 2.2 nF. The value of C_{SH_TANK} is usually 10 nF.

In mutual capacitance, you can connect any PSoC 6 MCU pin to a CapSense Rx/Tx sensor. Two integrating capacitors (C_{INT1} and C_{INT2}) are required for proper operation. A 470-pF capacitor is recommended on C_{INT1} and C_{INT2}. In PSoC 6 MCU, C_{INT1} and C_{INT2} should be connected to P7[1] and P7[2].

CapSense detects a finger touch by a tiny variation in the sensor's capacitance (less than 1 pF). It is very sensitive to both signal and noise. Note the PCB layout tips for CapSense. See **PSoC 4 and PSoC 6 MCU CapSense Design Guide** for more details.

Pins with a large sink current that are close to CapSense pins can introduce an offset to the CapSense module's "GND." **Figure 26** illustrates a switch circuit for CapSense in the IDAC source mode. R1 and R2 represent the resistances of PSoC 6 MCU internal traces, and R3 represents the resistance of a PCB trace. A shared return path of sink current and CapSense current is composed of R2 and R3. The closer a pin is to the CapSense pin, the higher is the offset generated with increase in sink current that flows through the return path.

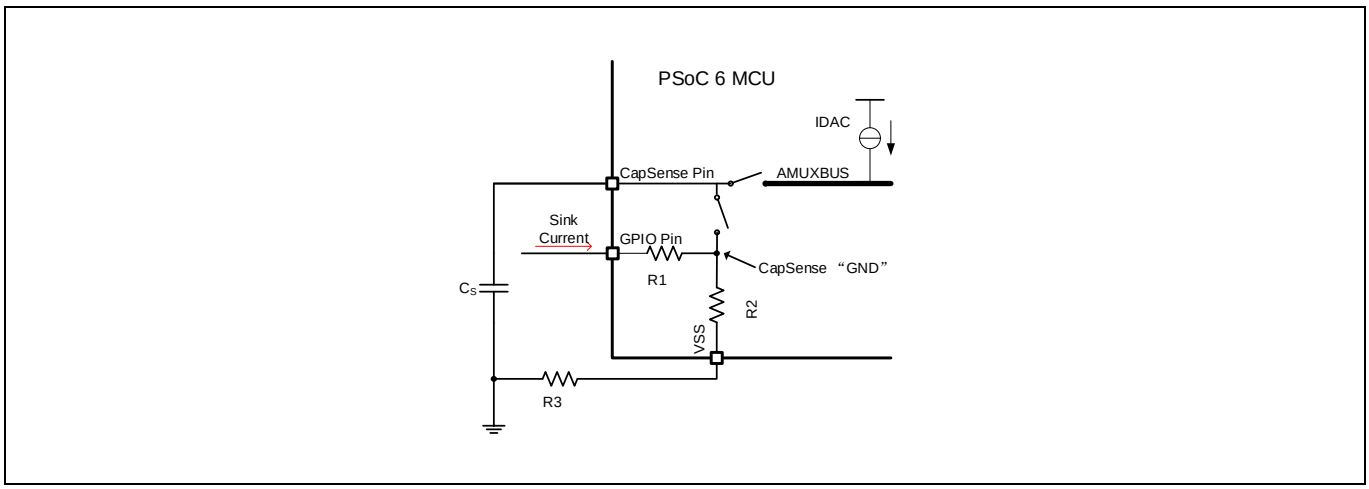

Figure 26 Sharing Return Path

This offset is undesirable and may cause fluctuations in the CapSense reading and possible false triggers. Offset compensation can be done in firmware, but it is strongly recommended that you remove the offset in the hardware design instead. Keep pins with a large sink current as far as possible from the CapSense pins (best practice is by more than three pins). In addition, pay attention to the return path in your PCB. See **AN57821 – PSoC 3, PSoC 4, and PSoC 5LP Mixed-Signal Circuit Board Layout Considerations** for more details on mixed-signal circuit design.

The CapSense block can be time shared for implementing both mutual and self-capacitance mode of sensing. For this, one has to connect the CMOD capacitor to P7[7] for CSD mode of sensing and CINT1 and CINT2 capacitors to P7[1]/P7[2] for CSX mode of sensing. This method, however, does not allow the use of a tank capacitor for CSD operation.

Analog Module Design Tips

In PSoC 6 MCU, follow the pin preference shown in **Table 5** for routing the CapSense sensor, shield, and Rx and Tx signals in your design. This preference is based on the pin's proximity to the CapSense block inside PSoC 6 MCU. Choosing a lower preference port might result in slight performance degradation. If the board design/routing suits a lower-preference I/O port, it can be selected. Use this preference only if routing is not a constraint.

Table 5 CapSense Port Preference for Routing

Preference	CapSense Sensor	CapSense Shield	CapSense Rx	CapSense Tx
First Preference	Port 5, Port 6, Port 7, Port 8			Any Port
Second Preference	Port 9 and Port 10			
Third Preference	Port 0, Port 1, Port 11, Port 12, and Port 13			

*Note: Simultaneous GPIO switching with unrestricted drive strengths and frequency can affect CapSense performance. For selecting GPIO pins for CapSense sensors, follow the recommendations given in **AN85951 - PSoC 4 and PSoC 6 MCU CapSense Design Guide**.*

A quick CapSense layout rule checklist is provided in **Table 6**.

Table 6 CapSense Layout Quick Guide

Category			Min	Max	Remarks/Recommendations
Sensor Construction	Sensor Material		N/A	N/A	Copper, Indium Tin Oxide (ITO), printed ink on substrates such as glass, flex PCB
	Overlay Material		N/A	N/A	Needs to be non-conductive material with high permittivity: Glass, ABS Plastic, Formica Avoid using conductive paints on the overlay.
	Widget				
	Button	Shape			Circle or rectangular with curved edges
		Size	5 mm	15 mm	10 mm
		Clearance to ground hatch	0.5 mm	2 mm	Should be equal to overlay thickness
		Overlay thickness	N/A	5 mm	
	Slider	Width of segment	1.5 mm	8 mm	8 mm
		Clearance between segments	0.5 mm	2 mm	0.5 mm
		Height of segment	7 mm	15 mm	12 mm
		Overlay thickness	N/A	5 mm	
	Overlay Adhesive		N/A	N/A	Use a nonconductive adhesive film for bonding the overlay and the PCB. 3M™ makes a high-performance acrylic adhesive called 200MP that is widely used in CapSense applications.
PCB Layout	Sensor Traces	Width	N/A	7 mil	Use the minimum width possible with the PCB technology that you use.

Analog Module Design Tips

Category			Min	Max	Remarks/Recommendations
		Length	N/A	300 mm for a standard (FR4) PCB 50 mm for flex PCB	Keep as low as possible
		Clearance to ground and other traces	0.25 mm	N/A	Use maximum clearance while keeping the trace length as low as possible.
		Routing	N/A	N/A	Route on the opposite side of the sensor layer. Isolate from other traces. If any non-CapSense trace crosses the CapSense trace, ensure that intersection is orthogonal. Do not use sharp turns.
	Via	Number of vias	1	2	At least one via is required to route the traces on the opposite side of the sensor layer.
		Hole size	N/A	N/A	10 mil
	Ground	Hatch fill percentage	N/A	N/A	Use hatch ground to reduce parasitic capacitance. Typical hatching: 25% on the top layer (7-mil line, 45-mil spacing) 17% on the bottom layer(7-mil line, 70- mil spacing)
Liquid Tolerance	Shield electrode	Spread	N/A	1 cm	If you have PCB space, use 1-cm spread.
	Guard sensor	Shape	N/A	N/A	Rectangle with curved edges Recommended thickness of guard trace is 2 mm and distance of guard trace to shield electrode is 1 mm.
EMC	Series resistor	Placement	N/A	N/A	Place the resistor within 10 mm of the PSoC pin.

8.2 SAR ADC

PSoC 6 MCU has a 12-bit differential SAR ADC (CY8C62x4 has two 12-bit SAR ADCs), with a sampling rate up to 2 Msps. Note that the maximum sampling rate of the SAR ADC depends on the selected PSoC 6 device. See the respective device **datasheet** to know the maximum SAR ADC sampling rate of the device. As mentioned in **I/O Pin Selection**, SAR ADC uses dedicated GPIO pins for multichannel inputs**.** They provide the lowest parasitic path resistance and capacitance. You can also route the signals from other pins to the SAR ADC using the internal analog bus, but doing so will introduce high switch resistance (R_{SW} in **Figure 27**) and additional parasitic capacitance.

Analog Module Design Tips

SAR ADC in PSoC 6 MCU has the following options for voltage reference:

- Internal V_{REF} (1.2 V or 0.8 V reference from AREF)
- V_{DDA}
- $V_{DDA}/2$
- External V_{REF}

PSoC 6 MCU also has an internal precision reference of 1.2 V (±1 percent). You can use other internal references, including V_{DDA} and V_{DDA} / 2, to extend the SAR ADC's input range. However, note that the accuracy of V_{DDA} and V_{DDA} / 2 as references depends on your power system design, and it probably cannot be better than the 1.2-V precision reference. When you use the internal reference or V_{DDA} / 2 as your reference, a bypass capacitor on the VREF pin can help you run the SAR ADC at a faster clock. See **Table 7** for details.

Table 7 References for SAR ADC

References	VDDA	Maximum SAR ADC Clock Frequency	Maximum Sample Rate	Supported Devices
External reference	1.7 V – 3.6 V	18 MHz	1 Msps	All PSoC 6 devices
	2.7 V – 3.6 V	36 MHz	2 Msps	CY8C62x4, CY8C61x5, CY8C62x5 CY8C62x8/A, and CY8C61x8/A devices.
Internal reference without bypass capacitor	1.7 V – 3.6 V	1.8 MHz	200 ksps	CY8C62x4, CY8C61x5, CY8C62x5 CY8C62x8/A, and CY8C61x8/A devices.
			100 ksps	CY8C61x6/7, CY8C62x6/7 and CY8C63x6/7 devices
Internal reference with bypass capacitor	1.7 V – 3.6 V	18 MHz	1 Msps	All PSoC 6 devices
V_{DDA} as reference	1.7 V – 2.7 V	18 MHz	1 Msps	All PSoC 6 devices
	2.7 V – 3.6 V	36 MHz	2 Msps	CY8C62x4, CY8C61x5, CY8C62x5 CY8C62x8/A, and CY8C61x8/A devices.

If you need a reference with a higher accuracy or a specific voltage value, you can connect a custom external reference and a bypass capacitor to the VREF pin.

The SAR ADC is differential physically. When you select single-ended input mode, you must select the connection for the negative input. There are three options: VSS, VREF, and an external pin. The SAR ADC's input range is affected by the selection as well as by the value of the reference voltage. See the chapter "SAR ADC" in **PSoC 6 MCU: Architecture TRM** devices for more information.

*Note: Simultaneous GPIO switching with unrestricted drive strengths and frequency can affect ADC performance. For more details, see the Errata section of the corresponding device **datasheet**.*

8.2.1 SAR ADC Acquisition Time

Another parameter of concern is the SAR ADC acquisition time, which depends on your hardware design, as **Figure 27** shows.

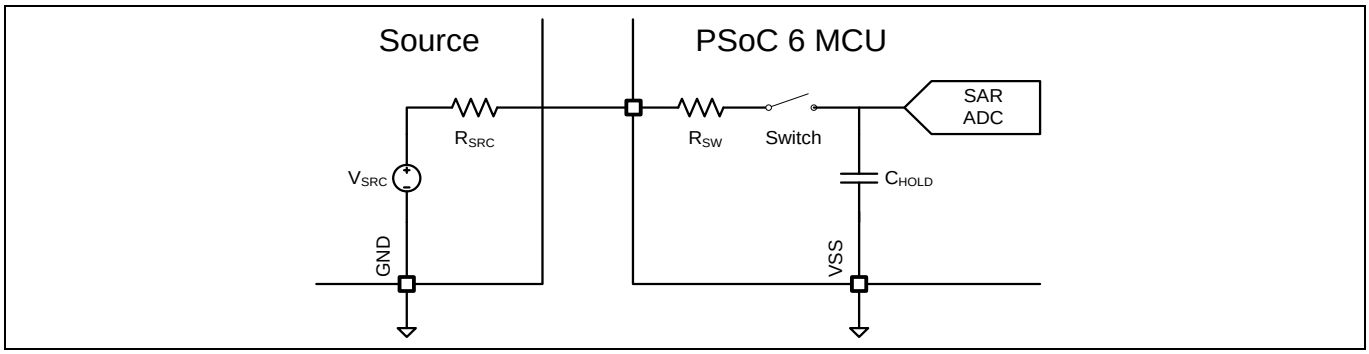

Figure 27 Equivalent Sample and Hold Circuit of PSoC 6 MCU SAR ADC

V_{SRC} is the sampled signal source, and R_{SRC} is its output resistance. R_{SW} is the resistance of the path from a dedicated pin to the SAR ADC input. C_{HOLD} is the sample and hold capacitance. See the respective PSoC 6 MCU device **datasheet** for the values of R_{SW} and C_{HOLD}.

Figure 28 shows how C_{HOLD} is charged during the acquisition time. During the acquisition time, the switch in **Figure 27** is on. Assuming that C_{HOLD} is charged from 0, the acquisition time is the time required to charge C_{HOLD} to a voltage level (V_{HOLD}) such that the error ($V_{SRC} – V_{HOLD}$) is less than the ADC's resolution.

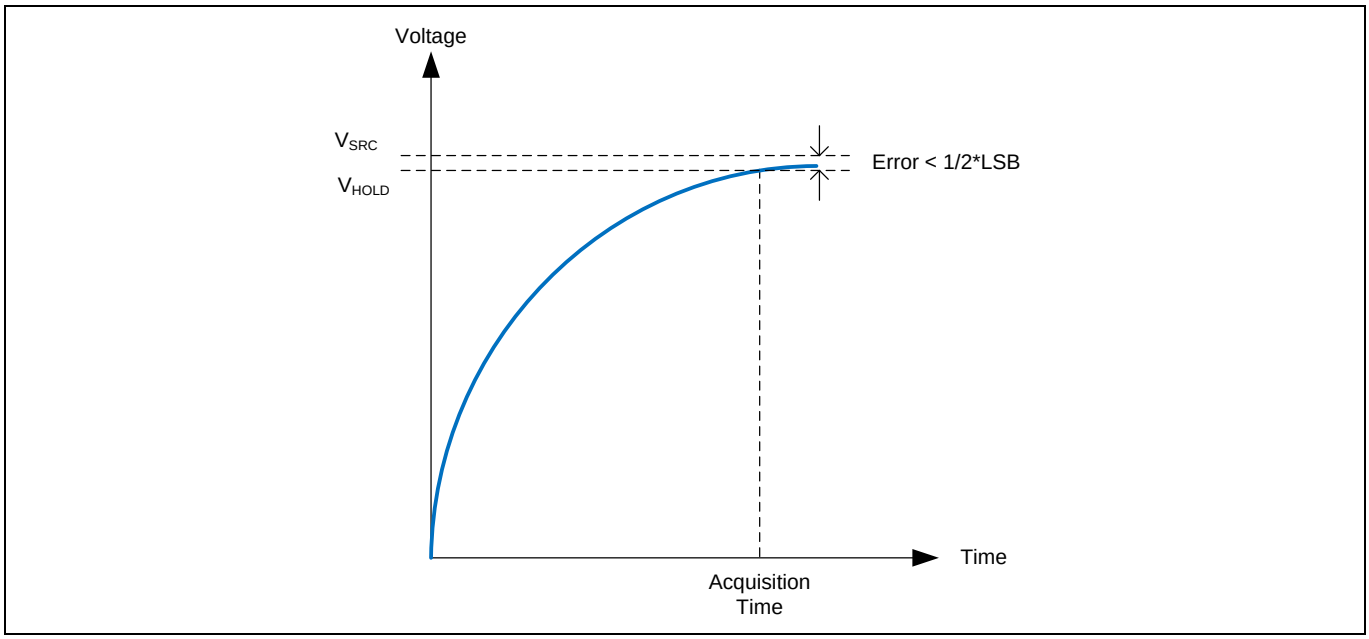

Figure 28 C_{HOLD} Charging Process

If the error is smaller than half the ADC's resolution (1/2 * LSB), it should be okay. The error can be related to the acquisition time in the following equation:

$$Error = V_{SRC} \cdot e^{-\frac{t_{ACQ}}{\tau}} = V_{SRC} \cdot e^{-\frac{t_{ACQ}}{(R_{SRC}+R_{SW}) \times C_{HOLD}}}$$

Analog Module Design Tips

Here, t_{ACQ} is the acquisition time, while $_{\tau}$ is the charging time constant.

PSoC 6 MCU provides a 12-bit differential ADC. If V_{REF} is the reference voltage, the resolution can be expressed in the following equation:

$$\mathrm{LSB} = \frac{2V_{\mathrm{REF}}}{2^{12}}$$

This example assumes that the negative input is connected to V_{REF}, so that V_{SRC} has an input range from 0 to 2 V_{REF}. If the acquisition time is 9 * (R_{SRC} + R_{SW}) * C_{HOLD}, the error can be expressed as follows:

$$Error = V_{\mathrm{SRC}} \cdot e^{-9} \approx \frac{V_{\mathrm{SRC}}}{8013} < \frac{2V_{\mathrm{REF}}}{8013} \approx \frac{1}{2} \cdot \frac{2V_{\mathrm{REF}}}{2^{12}} = \frac{1}{2} \cdot \mathrm{LSB}$$

This equation shows that you should choose an acquisition time that is longer than 9 * (R_{SRC} + R_{SW}) * C_{HOLD} to make the error less than 1/2 * LSB of the 12-bit ADC.

In conclusion, pay attention to the output resistance of the sampled signal source, R_{SRC}, and the resistance introduced by PCB traces in your ADC hardware design. These determine the acquisition time and therefore the sampling rate. For example, in the CY8C62x4 device, the input resistance (R_{SW}) and input capacitance (C_{HOLD}) of the SAR ADC are 1 kΩ and 5 pF, respectively. If the output resistance of the sampled signal source is negligible, then the acquisition time of the SAR ADC can be calculated as 9 * (RSW) * $C_{HOLD,}$ which is approximately 45 ns.

8.3 CTDAC

The PSoC 6 MCU analog subsystem supports a 12-bit continuous time digital-to-analog converter (CTDAC). The 12-bit DAC provides a continuous time output without the need for an external sample-and-hold (S/H) circuit. The CTDAC block can be used in applications that require voltage references, bias, or analog waveform output.

CTDAC can have one of the following sources as the input voltage reference:

- V_{DDA}
- Internal V_{REF}
- External voltage reference

The opamp OA1 in the CTBm block is configured as a voltage follower and used to route the external signal as the reference voltage to the CTDAC. The external signal is routed to the DAC using AMUX and therefore any GPIO can be used to connect the external signal. Note that any signal on the OA1 output terminal can be used as an external signal source if OA1 is disabled. In that case, the signal will be loaded by the DAC's resistive ladder directly. Therefore, the impact of such loading should be considered.

Note: CY8C61x8/A, CY8C62x8/A, CY8C61x5, and CY8C62x5 devices do not contain the CTDAC block.

The CTDAC output can be routed in three different paths. **Table 8** shows the CTDAC output ports.

Table 8 CTDAC Output Paths

CTDAC Output Mode	Port#[Pin#]
Direct output path	P9[6]
Buffered output path via Opamp0	P9[2]
Sample and hold path using Opamp0 and C_{HOLD} capacitor	P9[2]

9 Using External Memory in the Design

PSoC 6 MCU has a provision for interfacing with an external memory if your design requires it. The serial memory interface (SMIF) IP block is used for this purpose. The SMIF block primarily implements a single-SPI, dual-SPI, quad-SPI, or octal-SPI communication to interface with external memory chips. The SMIF block's primary use case is to set up the external memory and have it mapped to the PSoC memory space using the hardware. The SMIF block connects to dedicated pins. Therefore, if your design requires the use of an external memory, then the corresponding pins should be used. See the device **datasheet** for more details on the pins.

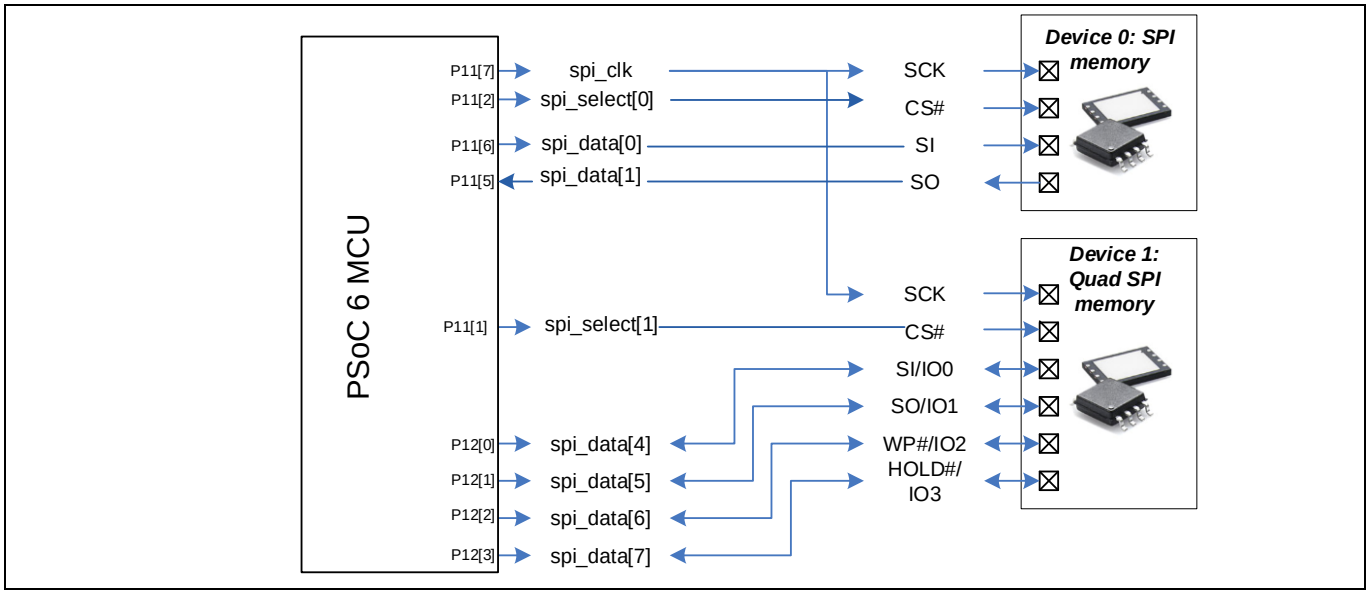

Figure 29 Serial Memory Interfacing with PSoC 6 MCU

10 USB Connection

The USB block is available as a fixed-function digital block in the PSoC device. It supports full-speed communication (12 Mbps) and is designed to be compliant with USB 2.0. The USB block includes the transmitter and receiver, which correspond to the USB physical layer (USB PHY). The USB PHY in PSoC also includes the pull-up resistor on the D+ line to identity the device as Full-Speed type to the host. The PHY integrates the 22-Ω series termination resistors on the USB lines.

10.1 PSoC 6 MCU USB Pin Description

Signal	PSoC 6 MCU Pin	Functionality
USBDP (D+)	P14[0]	Data line
USBDM (D-)	P14[1]	Inverted data line
VBUS	VDDUSB	USB power supply
GND		Ground

10.2 PSOC 6 MCU as USB Device

When designing hardware for a USB Device, consider the following:

- Use ferrite beads for VBUS, GND, and receptacle shield.
- Use an ESD protection device placed near the USB receptacle.

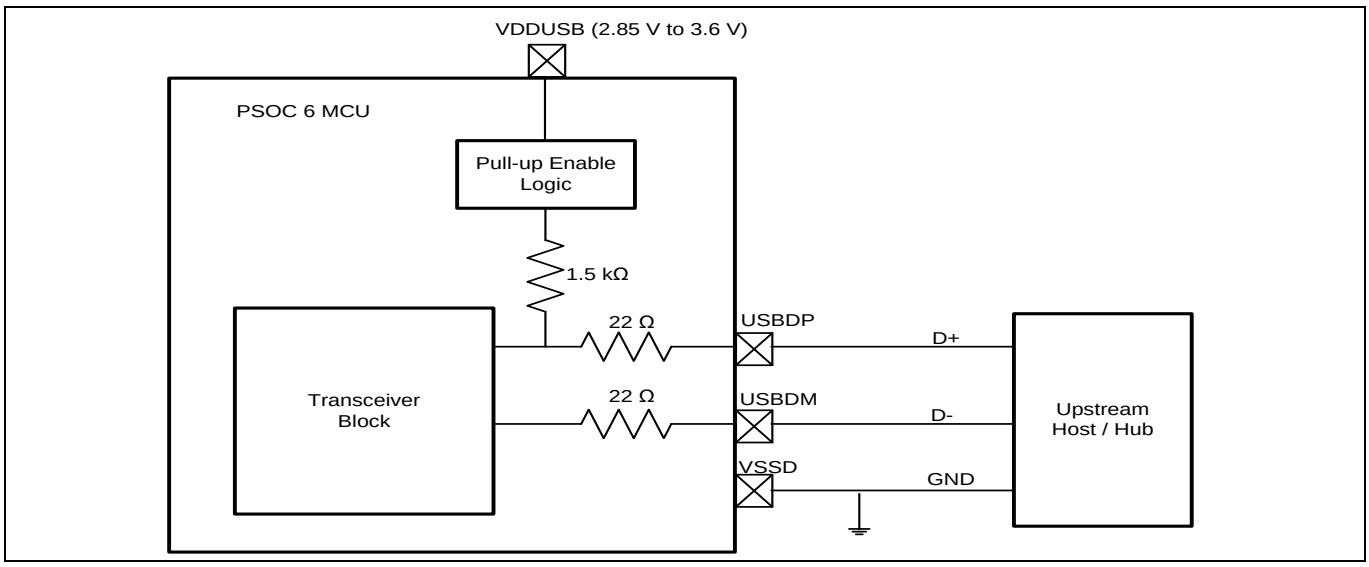

Figure 30 PSoC as USB Device

VDDUSB powers the USBDM and USBDP pins. For proper operation of the USB block, the VDDUSB supply voltage must in the range of 2.85 V to 3.6 V. When the USB block is not used in the design, the USB D+ and D- pins (USBDM and USBDP pins) can be used as GPIOs. When used as GPIOs, VDDUSB supports an operating voltage of 1.7 V to 3.6 V.

11 Antenna Design

PSoC 63 family of devices includes an on-chip BLE radio. Therefore, antenna design and RF layout become critical for a wireless system that transmits and receives electromagnetic radiation in free space. The wireless range that an end-customer gets out of the system with a current-limited power source such as a coin-cell battery depends greatly on the antenna design, the enclosure, and a good PCB layout. **Table 9** provides quick guidelines on antenna and RF layout.

Table 9 Antenna and RF Layout Quick Guide

PCB Stack up	**Four-Layer PCB** Cypress strongly recommends 4-layer PCB for all RF designs. Top Layer: RF IC and components, RF Trace, antenna, decoupling capacitors Layer 2: Ground plane Layer 3: Power plane Bottom Layer: Non-RF components and signals	**Two-Layer PCB** Typically used for simpler and cost-effective applications Top Layer: RF IC and components, RF Trace, antenna, decoupling capacitors Bottom Layer: Solid ground plane
Antenna Placement	Always place the antenna in a corner of the PCB with sufficient clearance as mentioned in the antenna datasheet from the rest of the circuit. Always follow the antenna designer's/manufacturer's recommended ground pattern for the antenna. Never place any component, planes, mounting screws, or traces in the antenna keep-out area across all layers. Ensure that the battery cable or mic cable does not cross the antenna trace on the PCB on the either side of the antenna. Do not place the antenna close to plastic in the industrial design. Proximity of plastic reduces the resonant frequency. Ensure that there is no trace or metallic plane in the antenna keep out area in any of the layers. Antenna must not be covered by a metallic enclosure Ensure that the orientation of the antenna is in line with the final product orientation so that the radiation is maximized in the desired direction. Plan to have a provision for an antenna-matching network because a lot of parameters in the antenna's proximity can vary its impedance, and therefore, the antenna may need retuning. Verify the antenna matching with the final enclosure.	
RF Trace Layout	Choose the right kind of transmission line (micro strip or Coplanar waveguide (CPWG)) when calculating the trace width needed for a 50-ohm characteristic impedance. Ensure that the RF trace has a 50-Ω characteristic impedance and maintain constant width for the RF trace. Ensure a clean, uninterrupted ground beneath the RF trace without any other traces crossing the RF trace. Maintain the shortest possible length for the RF trace. Avoid bends in the RF trace. If bends are unavoidable, make a curved bend to maintain a uniform width. Avoid stubs or branching and test points on the RF trace. Do not place any other traces close to and parallel to the RF trace.	

Antenna Design

PCB Stack up	**Four-Layer PCB** Cypress strongly recommends 4-layer PCB for all RF designs. Top Layer: RF IC and components, RF Trace, antenna, decoupling capacitors Layer 2: Ground plane Layer 3: Power plane Bottom Layer: Non-RF components and signals	**Two-Layer PCB** Typically used for simpler and cost-effective applications Top Layer: RF IC and components, RF Trace, antenna, decoupling capacitors Bottom Layer: Solid ground plane
Ground Plane	Allow a wide ground plane beneath the RF trace. It is better to keep a layer completely dedicated for ground. Keep the bottom ground plane together with the top ground plane and add vias between the two ground planes to improve the EMI and EMC performance. Cover the corners of the power plane with via holes connecting ground planes on either side of the power plane to arrest the unwanted EMI.	
Power Supply Decoupling	Place the capacitors close to the supply pin on the same layer as the IC with the smallest value capacitor closest. Use separate vias to the ground for each decoupling capacitor.	
Vias	Use plenty of vias spaced not more than one-twentieth of the wavelength of the RF signals between ground fillings at the top layer and inner ground layer. Place ground vias immediately next to pins/pads in the top layer and never share via with multiple pins/pads. Avoid using vias to route the RF trace to a different layer. Whenever possible, use vias to form a ground fencing around the RF section to isolate it from the rest of the circuit.	
Capacitors and Inductors	Use only C0G/NP0 capacitors for matching network and crystal load. X5R or X7R capacitors can be used for decoupling capacitors. Use only high-Q capacitors for RF circuits. For matching networks, use high-Q inductors with a self-resonant frequency (SRF) well above the operating frequency. For power supply filtering, use inductors with an SRF close to the noise frequency. Do not place inductors parallel and close to each other.	
Coexistence with Wi-Fi	Keep the BLE antenna and Wi-Fi antenna as far apart as possible. For antennas with linear polarization, orient the antennas such that they are electrically orthogonal to each other. If possible, orient the antennas such that the direction of the nulls of the antennas is collinear. Place via fencing between the BLE and Wi-Fi sections of the board to minimize leakage through the PCB.	

11.1 Support for External Power Amplifier/Low-Noise Amplifier/RF Front-End

Some applications may need a range higher than what is typically supported by the chipset. In such cases, either an external power amplifier (PA) and/or a low-noise amplifier (LNA) can be used to boost the link budget. For the 2.4-GHz radio, there are plenty of front-end ICs that include the power amplifier, low-noise amplifier, switches and controls needed to control them. These controls need to be precisely timed based on the actual transmit and receive timing. If the product has to remain BLE-compliant, ensure that the transmit power level does not exceed 20 dBm.

PSoC 6 MCU has three control signals to control the RF front-end ICs. **Figure 31** shows the interfacing of these control signals between PSoC 6 MCU and external RF front-end IC.

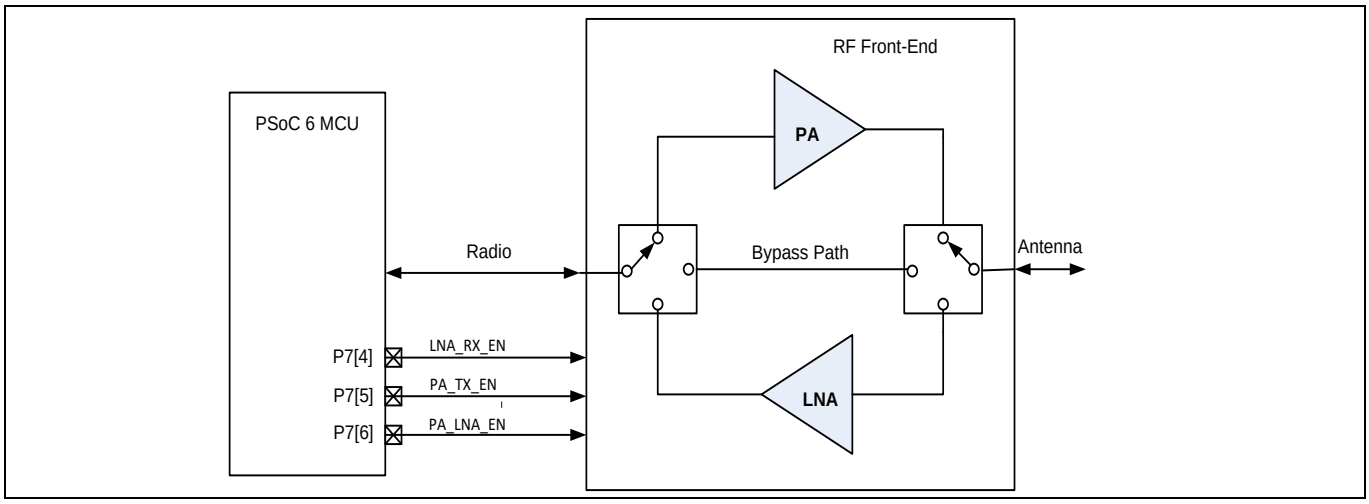

Figure 31 Interfacing RF Front-End with PSoC 6 MCU

Table 10 lists the control signals, their functions, and the corresponding pin mapping.

Table 10 PSoC 6 MCU Control Signals for Interfacing RF Front-End IC

Control Signal	Port#[Pin#]	Function
LNA_RX_EN	P7[4]	This signal is asserted when the receiver is enabled and de-asserted when receiver is off.
PA_TX_EN	P7[5]	This signal is asserted when the transmitter is enabled and de-asserted when transmitter is off.
PA_LNA_EN	P7[6]	This signal is asserted when either transmitter or receiver is active and de-asserted when neither of them is active. Can be used as chip select for front end modules

Antenna Design

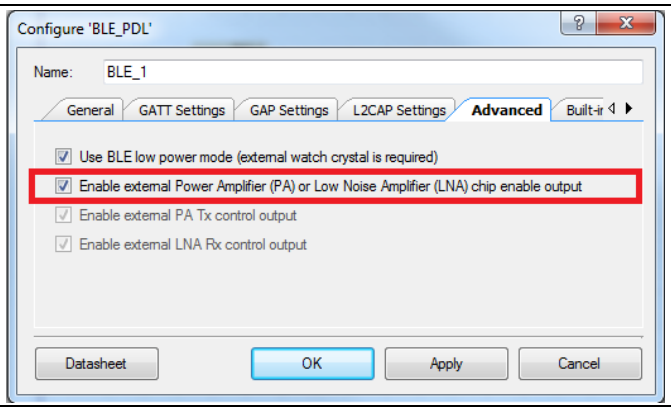

Figure 32 Configuring BLE to Interface with External RF Front-End IC in PSoC Creator

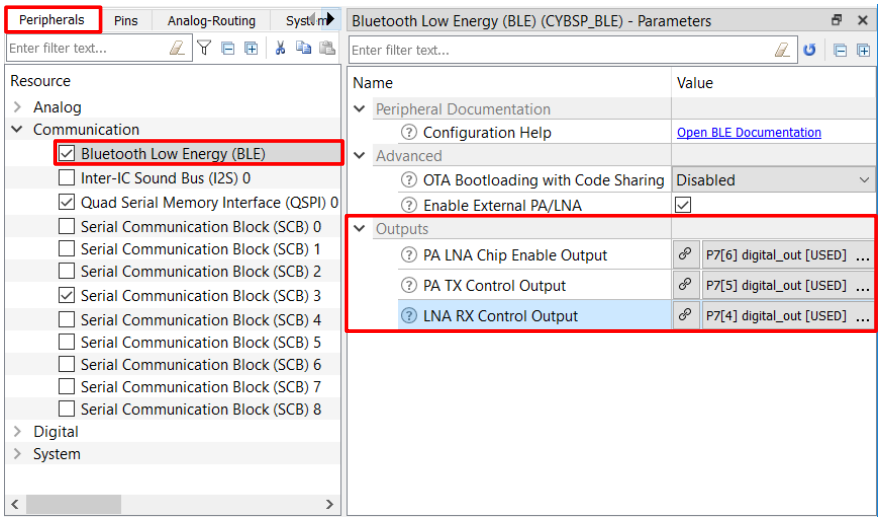

Figure 33 Configuring BLE to Interface with External RF Front-End IC in ModusToolbox

You can configure the BLE Component to interface with external RF front-end as shown in **Figure 32** and **Figure 33** using PSoC Creator and ModusToolbox IDE respectively. For more details on antenna design, see **AN91445 – Antenna Design and RF Layout guidelines**.

12 Audio Subsystem

The audio subsystem in PSoC 6 MCU consists of up to two I2S block and two PDM channels. The PDM channels interface to a PDM microphone's bit-stream output and produce word lengths of 16 to 24 bits at audio sample rate of up to 48 ksps. The I2S interface supports Master mode with Word Clock rates of up to 192 ksps (8-bit to 32-bit words).

Figure 34 and **Figure 35** show the interfacing of PDM audio device and I2S audio device with PSoC 6 MCU, respectively.

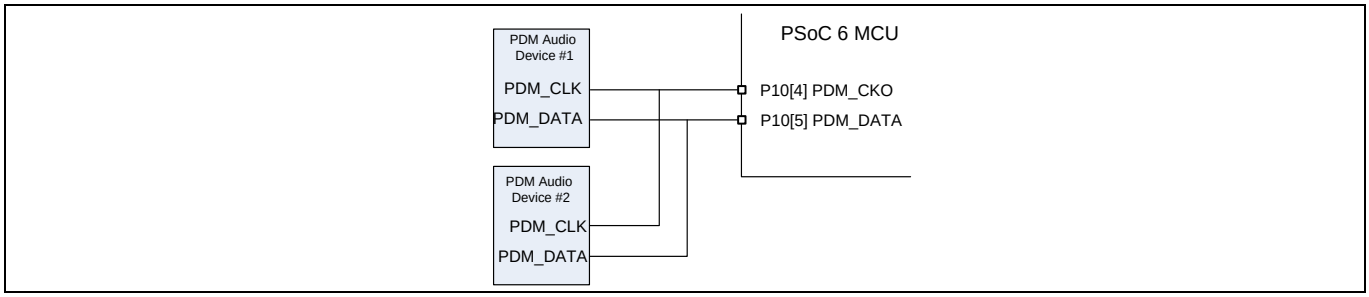

Figure 34 Interfacing PDM Audio Device with PSoC 6 MCU

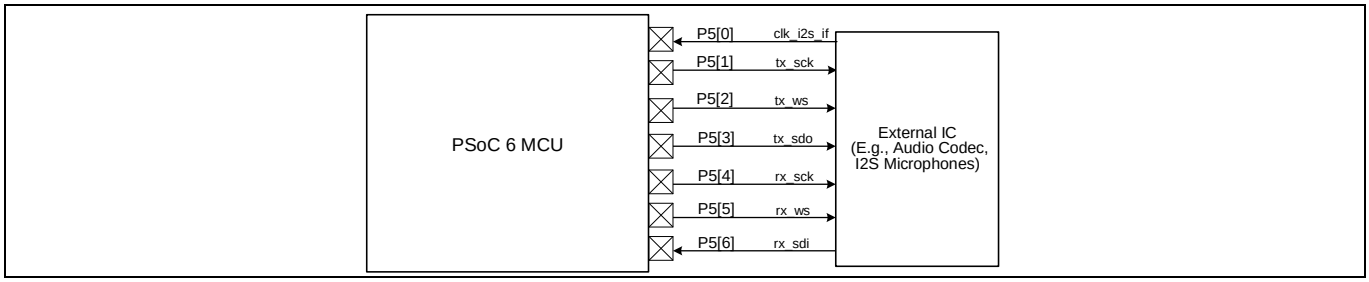

Figure 35 Interfacing I2S Audio Device with PSoC 6 MCU

I2S can be operated from an external master clock provided through an external IC such as audio codec. Pin P5[0] (clk_i2s_if) is used to drive an external clock to the I2S block.

12.1 Clock Generation for PDM-PCM Converter

In PSoC 6 MCU PDM-PCM converter has three stages of clock dividers to generate the clock (PDM_CKO), which is the input to the external PDM microphone clock input. The three stages are as follows:

- The first stage clock divider is used to generate the actual clock signal (PDM_CLK) which goes to the PDM-PCM converter. HFClk1 is the input clock for this stage. 1st Clock Divisor value can take integer values from 1 to 4.

  PDM_CLK=HFClk1/1st Clock Divisor
- The second stage is used to generate an internal master clock (MCLK) from the PDM_CLK. 2nd Clock Divisor value can take integer values from 1 to 4.

  MCLK=PDM_CLK/2nd Clock Divisor
- The third stage clock divider is used to generate the clock that goes to the PDM microphone. The third stage divider can take value between 2 and 16.

  PDM_CKO=MCLK/3rd Clock Divisor

The sample rate (F_s) for the PDM audio devices is given by the following relation:

Audio Subsystem

F_s=PDM_CKO / (2 x Sinc Decimation Rate)

12.2 Clock Generation for I2S Audio Devices

Audio applications require high accuracy clocks and therefore, a highly accurate ECO is required in such applications. Typically, a 17.2032-MHz crystal oscillator is used to generate 22.579 MHz for the 44.1-kHz audio sample rate and 24.576 MHz for the 48-kHz audio sample rate. **Table 11** shows the settings of the PLL to generate the required clock frequencies. You can set the divider and multiplier settings of the PLL either manually or automatically. **Table 12** shows the clock divider settings for typical audio sample rate and word lengths.

Table 11 PLL Multiplier and Divider Settings

ECO (MHz)	PLL Multiplier (P)	PLL Divider (Q)	PLL Output Frequency (MHz)
17.2032	21	16	22.579
17.2032	10	7	24.576

Table 12 Clock Divider Settings for Typical Audio Sample Rates and Word Lengths

Audio Sample Rate (kHz)	PLL Output Frequency (MHz)	Word Length					
		8-bit		16-bit		32-bit	
		Codec Clock (kHz)	Clock Divider	Codec Clock (kHz)	Clock Divider	Codec Clock (kHz)	Clock Divider
44.1	22.579	705.6	32	1411.2	16	2882.4	8
48	24.576	768	32	1536	16	3072	8
96	24.576	1536	16	3072	8	6144	4
192	24.576	3072	8	6144	4	12288	2

For more details, see the "PDM-PCM" and "I2S Sound Bus" chapters of **PSoC 6 MCU: Architecture TRM**.

13 Secure Digital Host Controller

CY8C62xA/8/5 devices of the PSoC 6 MCU family have up to two secure digital host controllers (SDHC). The SDHC allows interfacing with embedded multimedia card (eMMC)-based memory devices, secure digital (SD) cards and secure digital input output (SDIO) cards. The SDHC block can be used to connect devices providing the SDIO interface, such as Cypress' Wi-Fi products. **Figure 36** and **Figure 37** shows interfacing of a Wi-Fi device and SD storage with PSoC 6 MCU. It is recommended to have pull-up resistors (R_pull_up) in the range of 10 kΩ – 100 kΩ on the SDIO lines. Also, it is recommended to use series termination resistor of 33 Ω on the SDIOs lines.

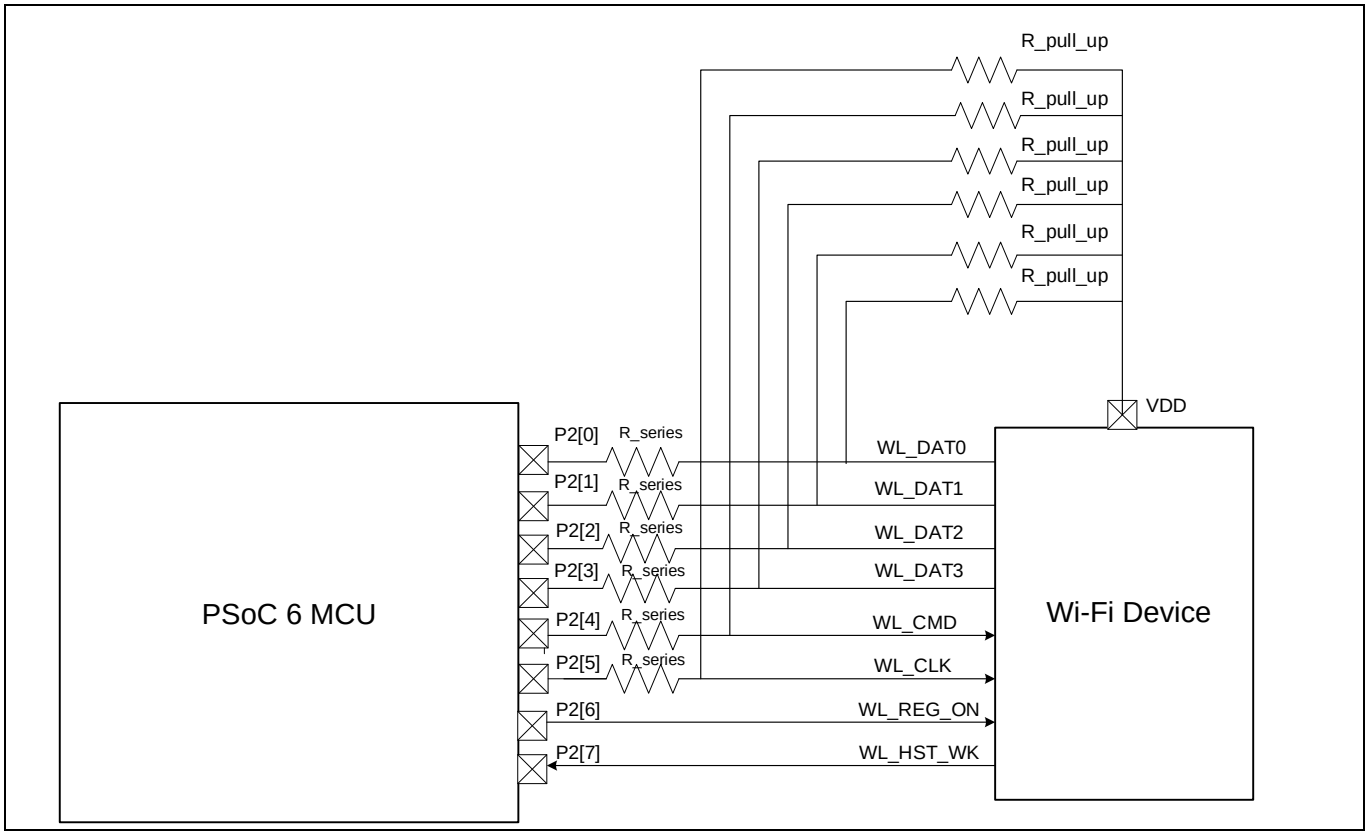

Figure 36 Interfacing Wi-fi Device Using SDHC in PSoC 6 MCU

Secure Digital Host Controller

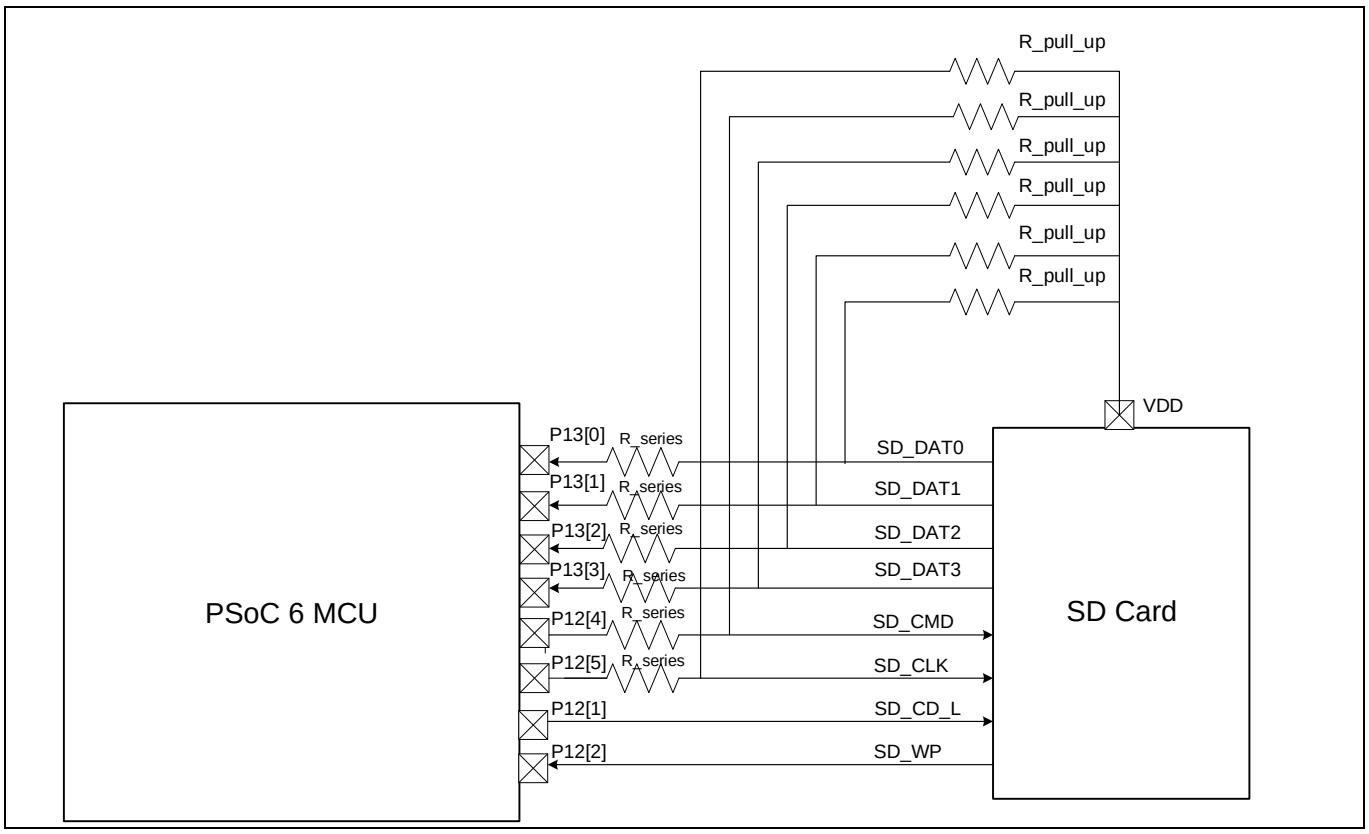

Figure 37 Interfacing SD Storage Using SDHC in PSoC 6 MCU

14 Summary

PSoC 6 MCU provides a flexible solution for designing digital and analog applications. This application note documented the considerations that you need to keep in mind when you build a hardware system around PSoC 6 MCU.

Related Documents

[1] **AN79938** – Design Guidelines for Cypress BGA Packaged Devices

[2] **AN69061** – Design, Manufacturing, and Handling Guidelines for Cypress Wafer Level Chip Scale Packages

[3] **AN228571** – Getting Started with PSoC 6 MCU on ModusToolbox

[4] **AN221774** – Getting Started with PSoC 6 MCU on PSoC Creator

[5] **AN210781** – Getting Started with PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity

[6] **AN80994** – Design Considerations for Electrical Fast Transient (EFT) Immunity

[7] **AN57821** – PSoC 3, PSoC 4, and PSoC 5LP Mixed-Signal Circuit Board Layout Considerations

[8] **AN91445** – Antenna Design and RF Layout Guidelines

[9] **AN91184** – PSoC 4 BLE – Designing BLE Applications

[10] **AN95089** – PSoC 4/PRoC BLE Crystal Oscillator Selection and Tuning Techniques

[11] **AN85951** – PSoC 4 and PSoC Analog Coprocessor CapSense Design Guide

Appendix A - PCB Layout Tips

Before beginning a PCB layout for PSoC, it is a good idea to look at AN57821 – PSoC Mixed-Signal Circuit Board Layout Considerations. Appendix A of that application note shows example PCB layouts and schematics for various PSoC packages.

There are many classic techniques for designing PCBs for low noise and EMC. Some of these techniques include:

- **Multiple layers:** Although they are more expensive, it is best to use a multilayer PCB with separate layers dedicated to the V_{SS} and V_{DD} supplies. This gives good decoupling and shielding effects. Separate fills on these layers should be provided for V_{SSA}, V_{SSD}, V_{DDA}, V_{DDIO}, and V_{DDD}.

  To reduce cost, a two-layer or even a single-layer PCB can be used. In that case, you must have a good layout for all V_{SS} and V_{DD}.
- **Ground and power supply:** There should be a single point for gathering all ground returns. Avoid ground loops, or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding to create a shield, especially when using two-layer or single-layer PCBs.

  The power supply should be close to the ground line to minimize the area of the supply loop. The supply loop can act as an antenna and can be a major emitter or receiver of EMI.
- **Decoupling:** The standard decoupler for external power is a 100-µF capacitor. Supplementary 0.1-µF capacitors should be placed as close as possible to the V_{SS} and V_{DD} pins of the device to reduce high-frequency power supply ripple.

  Generally, you should decouple all sensitive or noisy signals to improve the EMC performance. Decoupling can be both capacitive and inductive.
- **Component position:** Separate the circuits on the PCB according to their EMI contribution. This will help reduce cross-coupling on the PCB. For example, separate noisy high-current circuits, low-voltage circuits, and digital components. The decoupling capacitors and the inductor (Buck Inductor) should be placed as close as possible to the device pins with minimum trace resistance.
- **Signal routing:** When designing an application, the following areas should be closely studied to improve the EMC performance:
  - Noisy signals. For example, signals with fast edge times
  - Sensitive and high-impedance signals
  - Signals that capture events, such as interrupts and strobe signals

  To improve the EMC performance, keep the trace lengths as short as possible and isolate the traces with V_{SS} traces. To avoid crosstalk, do not route them near to or parallel to other noisy and sensitive traces.

For more information, several references are available:

- *The Circuit Designer's Companion*, *Second Edition, (EDN Series for Design Engineers),* by Tim Williams
- *PCB Design for Real-World EMI Control (The Springer International Series in Engineering and Computer Science),* by Bruce R. Archambeault and James Drewniak
- *Printed Circuits Handbook* (McGraw Hill Handbooks), by Clyde Coombs
- *EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple*, by Mark I. Montrose
- *Signal Integrity Issues and Printed Circuit Board Design*, by Douglas Brooks

Appendix B - Schematic Checklist

The answer to each item in the following checklist should be Yes (Y) or Not Applicable (N.A.). For example, if you power a PSoC 6 MCU device with an unregulated external supply in your application, you can mark all the items of "Power (regulated external supply)" as N.A.

Catalog	Item	Y/N/N.A	Remark
Power	Are the power supply pin connections made in accordance with **Power Pin Connections**?		
	Are the 0.1-µF and 1-µF capacitors connected to each VDDD, VDDIO, VDDA, or VDDR pins?		
	Are the 10-µF and 0.1-µF capacitors connected to VDD_NS pin?		
	Are the voltages (including ripples) at the VDDD and VDDA pins in the range of 1.7 to 3.6 V?		
	Is the VCCD pin connected to a 4.7 µF capacitor?		
	If the VRF pin powers BLE, is the pin connected to a 10 µF capacitor?		
	For CY8C61x6/7, CY8C62x6/7, CY8C63x6/7 devices, is the 2.2-µH inductor connected between VIND1 and VIND2 pins? For CY8C61xA/8, CY8C62xA/8, CY8C61x5, CY8C62x5, CY8C62x4 devices, is the 2.2-µH inductor connected between VIND and VCCD pins?		
	Is the VRF pin connected to the VDCDC pin?		
	Is the VDDR pin connected to the VDCDC pin?		
	Is the VBACKUP pin connected to an appropriate supply (VDDD or the 1.4-V to 3.6-V source)?		
	Is the 1-µF capacitor connected to the VDDR_HVL pin, and has no external load?		
Clocking	Is the external clock connected to EXT_CLK pin?		
	Is the external clock's frequency less than or equal to 48 MHz (including tolerance)?		
	Is the external clock's duty cycle from 45 percent to 55 percent?		
	Is the external 32-MHz crystal connected to XI and XO for BLE operation?		
	Is the external MHz crystal connected to ECO pins for ECO operation?		
	Is the 32.768-kHz crystal connected to WCO for RTC operation? Are the WCO load capacitors connected?		
	Is the external 32.768-kHz square wave clock connected to WCO_OUT pin and WCO_IN left floating?		
Reset	Is the reset pin connection made in accordance with **Figure 17**?		
Programming and debugging	Are the SWD/JTAG/ETM signals connected as described in the **Programming and Debugging** section?		
GPIO pins	Is the assignment of your GPIO pins done in the sequence described in **I/O Pin Selection**? *Note: Simultaneous GPIO switching with unrestricted drive strengths and frequency can induce noise in on-chip*		

Appendix B - Schematic Checklist

Catalog	Item	Y/N/N.A	Remark
	*subsystems affecting CapSense and ADC results. See to the Errata section in the respective device **datasheet** for details.*		
	Is every GPIO pin's sink current lower than 8 mA?		
	Is every GPIO pin's source current lower than 4 mA?		
	Is the GPIO pins' total source current or sink current smaller than device capability?		
SCB	Is the assignment of the SCB's fixed pins in accordance with the device **datasheet**?		
CapSense	Are the pins with strong sink current kept away from the CapSense pins (the space is more than three pins)?		
	Is C_{MOD} connected to the **CMOD** (or **C_MOD**) pin for self-capacitive sensing?		
	Is C_{SH_TANK} connected to the **CTANK** (or **C_SH_TANK**) pin for self-capacitive sensing as explained in the **CapSense** section?		
	Are the C_{INT1} and C_{INT2} capacitors connected for mutual capacitive sensing?		
	Are the CapSense sensor, shield, Rx, and Tx signals selected based on preference provided in **Table 5**?		
Antenna	Is the Antenna design based on recommendations from **AN91445**?		

Revision history

Document version	Date of release	Description of changes
**	12/27/2016	New application note
*A	08/16/2017	Updated template. Updated Support for External Power Amplifier/Low-Noise Amplifier/RF Front-End. Updated **Figure 1**. Updated **Table 2**.
*B	04/27/2018	Updated **Figure 1**, **Figure 3**, **Section 3.2**, and **Appendix B** - Schematic Checklist
*C	11/01/2018	Updated for ModusToolbox
*D	04/09/2019	Updated the following sections: **GPIO Pins**, **CapSense**, and **SAR ADC** Updated decoupling capacitor values in the **Power Pin Connections** section
*E	09/16/2019	Added CY8C62x5 device support; Updated for ModusToolbox 2.0.
*F	12/16/2019	Updated WCO load capacitor connection diagram (**Figure 10**)
*G	03/27/2020	Updated ECO frequency range to 16 MHz to 35 MHz Updated ECO and WCO load capacitor calculation. Removed ECO configuration in ModusToolbox and PSoC Creator figures. Updated ECO load capacitor connection diagram (**Figure 8**) Updated WCO load capacitor connection diagram (**Figure 10**)
*H	07/23/2020	Added CY8C62x4 device. Updated **Power Pin Connections** – Added recommendations for buck regulator inductor and capacitor selection; Updated **Figure 1** and **Figure 2**. Updated **SAR ADC** – ADC sampling rate and acquisition time. Updated PILO accuracy.
*I	2021-03-08	Updated to Infineon Template

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