Endurance and Data Retention Characterization of Infineon Flash Memory

About this document

Scope and purpose

This document provides the endurance and data retention characterization of Infineon flash memory products.

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1 Introduction

Nonvolatile flash memory technology is subject to physical degradation that can eventually lead to device failure. Vendors use two end-of-life parameters to specify the performance of reprogrammable nonvolatile memory: Program/Erase endurance and data retention. Understanding the practical meaning of these parameters and their inter-relationship allows a designer to properly assess the capabilities in order to meet the system performance and reliability requirements.

This application note provides a perspective on nonvolatile flash memory reliability testing methodology and discusses the influence of key factors in terms of Program/Erase endurance and data retention. It also provides information on reliable usage models using Infineon products related to industry standards.

2 Industrial standard trend – Program/Erase cycling and data retention

JEDEC standard JESD22-A117 indicate that over-stressing a memory product during reliability evaluation will impact the data retention after Program/Erase cycling. This is not uncommon. Overstressing flash during pre-production and/or production tests can impact data retention of later operations.

> JESD22-A117
>
> 4.1.2.4 Intentional delays between cycles
>
> The degradation rate of EEPROM products may depend strongly on the cycling frequency.

This sentence indicates that significant overstress can excessively accelerate the degradation of nonvolatile flash memory performance. Design of high-reliability products based on a product usage model is a primary concern, especially for newer technologies. It is essential to comprehend the gap between the evaluation condition and field usage to adequately characterize the reliability of the application in the field. Understanding field usage models (cycling frequency per sector, temperature, etc.) and testing under the same conditions will avoid overstressing the device.

3 Testing procedure for Program/Erase cycling and data retention

3.1 Test procedure

JEDEC qualification standards JESD47, JESD22-A117, and AEC-Q100 require evaluation samples to undergo both endurance stress and data retention stress after completing endurance.

For endurance cycling, JEDEC specifies four primary points:

1. The cycling time is limited to 500 hours of actual cycling operations, not including inserted bake times used in cycling delays.
2. One must follow the inserted bake delay guideline in JESD22-A117.
3. High-temperature bakes are not to be inserted during room temperature endurance.
4. The delays plus the cycling time itself must not add up to more than 500 hours at 85 degree Celsius during high- temperature endurance.

The assumption of JEDEC's cycling condition is 1.5 years at 55 degree Celsius, which is equivalent to 500 hours at 85 degree Celsius when the assumed cycling de-trapping Ea is 1.1 eV for Floating gate technology.

For AEC-Q100, the primary concern of the endurance condition is the customer usage model. It recommends understanding the customer usage model, including the targeted Program/Erase cycling count, period, and temperature, because automotive products typically require a tighter field usage model. Moreover, Cycling shall be performed at temperature $T \geq 85^{o}C$, with total cycling time not exceeding 15 percent of the accelerated product life. (For example, 10 years product life in field allows 1.5 years Program/Erase cycling period in field.)

In cycling methodology, Infineon implements cycling in proportions of 100%, 10%, 1%, and less than 1% Program/Erase cycling on the same unit. At a minimum, Program/Erase cycling time of 100% and 10% areas occupy each one-third of total Program/Erase cycling time. **Figure 1** shows an example of sector assignment. The assigned sector number for each Program/Erase cycling target are intended to meet the 500 hours Program/Erase cycling period. **Figure 2** shows the allocation of cycling condition and time as one of conditions.

Row#	Sector#							
Row 31	248	249	250	251	252	253	254	255
Row 30	240	241	242	243	244	245	246	247
Row 29	232	233	234	235	236	237	238	239
Row 28	224	225	226	227	228	229	230	231
Row 27	216	217	218	219	220	221	222	223
Row 26	208	209	210	211	212	213	214	215
Row 25	200	201	202	203	204	205	206	207
Row 24	192	193	194	195	196	197	198	199
Row 23	184	185	186	187	188	189	190	191
Row 22	176	177	178	179	180	181	182	183
Row 21	168	169	170	171	172	173	174	175
Row 20	160	161	162	163	164	165	166	167
Row 19	152	153	154	155	156	157	158	159
Row 18	144	145	146	147	148	149	150	151
Row 17	136	137	138	139	140	141	142	143
Row 16	128	129	130	131	132	133	134	135
Row 15	120	121	122	123	124	125	126	127
Row 14	112	113	114	115	116	117	118	119
Row 13	104	105	106	107	108	109	110	111
Row 12	96	97	98	99	100	101	102	103
Row 11	88	89	90	91	92	93	94	95
Row 10	80	81	82	83	84	85	86	87
Row 9	72	73	74	75	76	77	78	79
Row 8	64	65	66	67	68	69	70	71
Row 7	56	57	58	59	60	61	62	63
Row 6	48	49	50	51	52	53	54	55
Row 5	40	41	42	43	44	45	46	47
Row 4	32	33	34	35	36	37	38	39
Row 3	24	25	26	27	28	29	30	31
Row 2	16	17	18	19	20	21	22	23
Row 1	8	9	10	11	12	13	14	15
Row 0	0	1	2	3	4	5	6	7

Figure 1 Example of Program/Erase Cycle Conditions in a Unit

Program/Erase Cycling condition		Assigned sector per a unit	Cycling count per a condition	Cycling time per a condition
Target percentage	Target cycling count per a sector			
100% Program/Erase cycling	100k Program /Erase cycles	2 sectors	200k Program /Erase cycles	Over 1/3 of 500 hours
10% Program/Erase cycling	10k Program /Erase cycles	20 sectors	200k Program /Erase cycles	Over 1/3 of 500 hours
Less than 10% Program/Erase cycling	1k Program /Erase cycles	40 sectors	40k Program /Erase cycles	Less than 1/3 of 500 hours
	100 Program /Erase cycles	80 sectors	8k Program /Erase cycles	
	10 Program /Erase cycles	80 sectors	0.8k Program /Erase cycles	
		Total	448.8k Program/Erase cycles	500 hours

Figure 2 Program/Erase cycling condition, allocation, and time

Note: Sector or block assignment depends on the specific product.

According to the JEDEC JESD47 specification, data retention lifetime for 100 percent Program/Erase cycling is required to meet 10 hours at 125 degree Celsius, and 10 percent Program/Erase cycling to meet 100 hours at 125 degree Celsius. (10 hours at 125 degree Celsius is equivalent with over 10 years at 55 degree Celsius in field when activation energy is 1.1 eV.) Data pattern during Data retention bake uses ChecKerBoarD(CKBD), Reverse-ChecKerBoarD(RCKBD), or Random. As an engineering study, data retention bake time is routinely extended to characterize the ability of data retention after Program/Erase cycling.

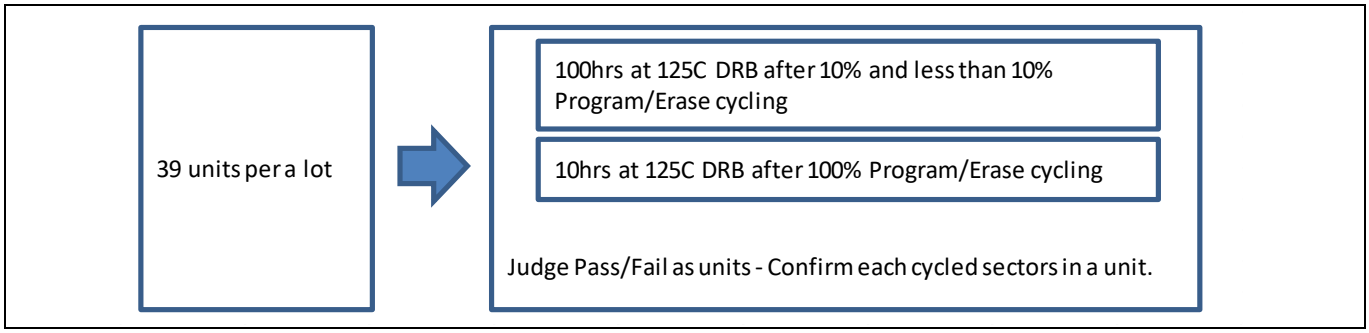

Figure 3 Data retention bake target

4 Impact of Program/Erase cycling condition

This section uses a simplified MirrorBit™ cell structure as a model and data. However, as a phenomenon, it is common both for NOR/NAND Flash Floating Gate technology and NOR Flash MirrorBit™ technology. Diminished data retention is possible with both NOR and NAND Flash because of high-frequency program/erase cycles to the same sectors.

The ideal program state of a flash memory MirrorBit™ cell is to have all stored electrons within the specific area of the Nitride layer of the cell as shown in **Figure 4** (a simplified rendering). Electrons are not de-trapped (diffused) easily from the Nitride layer, resulting in good data retention performance. In cases where Program/Erase is repeated rapidly, perhaps by using only a few sectors, the excess trapped electrons located near the Nitride layer increase significantly as shown in **Figure 5**. Those excess trapped electrons are easily de-trapped (diffused) and cause poorer data retention performance. If the product is run to a maximum cycle count (100 percent) in a days or even just a few hours, excess trapped electrons near the Nitride layer are accumulative due to the lack of a normal de-trapping effect between cycles. A higher cycling rate prevents relaxation recovery and it is a direct result of cycling overstress.

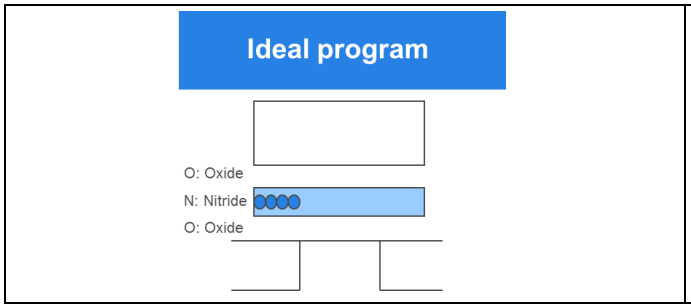

Figure 4 Ideal programming

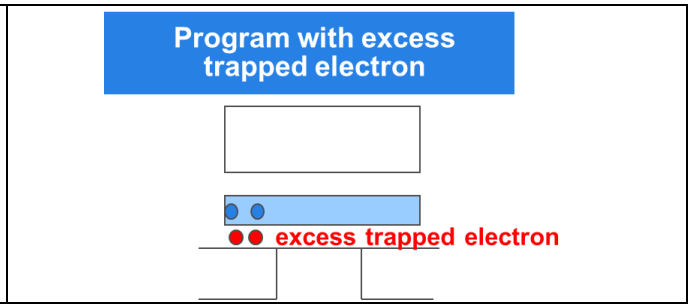

Figure 5 Overstressed programming

Note: Blue dots are electrons in the Nitride layer. Red dots are trapped electrons around the Nitride layer (ex, Oxide).

5 Factors affecting data retention lifetime after Program/Erase cycling

Post-Cycling Data retention is determined by three main parameters:

1. System Field Temperature (Program/Erase Cycling and Data Storage)
2. Total number of Program/Erase Cycles
3. Cycling Interval Time

These factors can significantly impact the retention lifetime after Program/Erase cycling. To ensure that the reliability design of the product is suitable for a particular customer application, a good understanding of these parameters is essential.

5.1 System field temperature (Program/Erase cycling and data storage)

Temperature is a significant modifier for endurance and data retention. One cannot universally assume that a part will work for its entire lifetime of 10 to 20 years by simply assuming a field average temperature such as 55 degree Celsius. In fact, there are a variety of temperature profiles based on real-world applications. Most of the time, a continuous high or low temperature is not typical for most applications. There is always a distribution of use at different temperatures. However, an average use temperature can be calculated from a complex temperature profile through the Arrhenius equation. Higher temperatures increase the impact to the average field temperature even if the actual time spent at the high temperature is small. Again, lower storage temperatures can increase retention lifetime while higher storage temperatures can decrease it significantly.

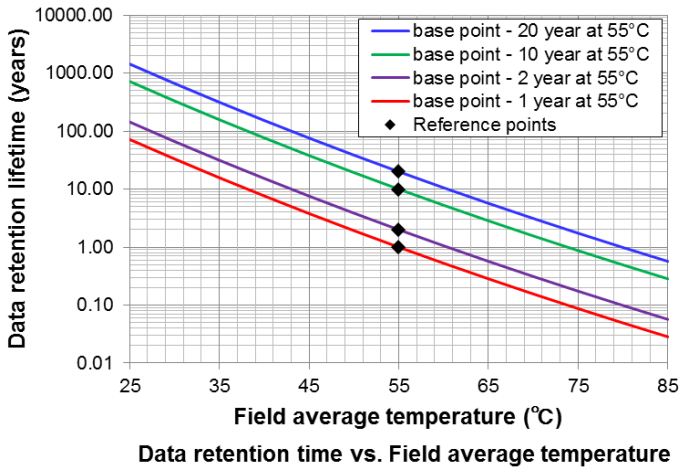

Figure 6 Data retention time vs. field average temperature

$$At = \exp\left[\left(\frac{Ea}{kb}\right)\times\left(\frac{1}{T_{field}}-\frac{1}{T_{reference}}\right)\right]$$

$$Lifetime_{FieldTemp} = At \times \left(Lifetime_{55°C}\right)$$

At: Acceleration temperature factor

Ea: MB activation energy: 1.2eV, Note: FG: 1.1eV

kb: Boltzmann constant= 8.62 1E-5 eV/K,

Tfield: Field average temperature (°C) + 273 K,

Treference: 55 (°C) + 273 K

Lifetime field: Data retention lifetime (years)

Lifetime 55 °C: Base points, 1/2/10/20 years at 55°C

Note: Assumptions are 1, 2, 10, and/or 20 years after Program/Erase cycling such as 10k or 100k cycles at 55 degree Celsius.

5.2 Total number of Program/Erase cycles

There is a trade-off between the Program/Erase cycling count and subsequent Data Retention capability. The larger the Program/Erase cycling count, the smaller the subsequent Data Retention after the completion of Program/Erase cycling. In general, they are inversely proportional; that is, if the number of Program/Erase cycles are increased by about one order (10x) of magnitude, it results in subsequent Data retention of about one order smaller (1/10x) of magnitude.

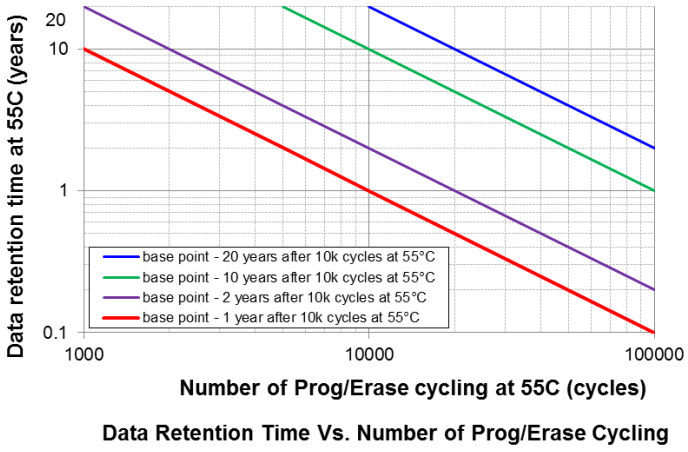

Figure 7 Relationship between data retention and Program/Erase cycling

The plotted lines are based on 1/2/10/20 year lifetime after 10k Program/Erase cycles at 55 °C.

5.3 Cycling Interval Time

The endurance specification of a flash device should be evaluated in terms of the projected in-system rate of erasure for any given sector. The sectors used for data logging may rapidly accumulate erase cycles depending on the frequency and size of the data being captured. Such use may ultimately lead to those sectors failing first. As such, the shorter the Program/Erase interval time between Program/Erase cycles, the worse the data retention. Longer interval times between Program/Erase cycles can de-trap the excess trapped electrons between Program/Erase cycles, resulting in better data retention. **Figure 8** shows an example of the retention lifetime over a variety of interval times, assuming 20 years retention lifetime after 10k Program/Erase cycles at an average of 55 degree Celsius cycling, under JEDEC test conditions.

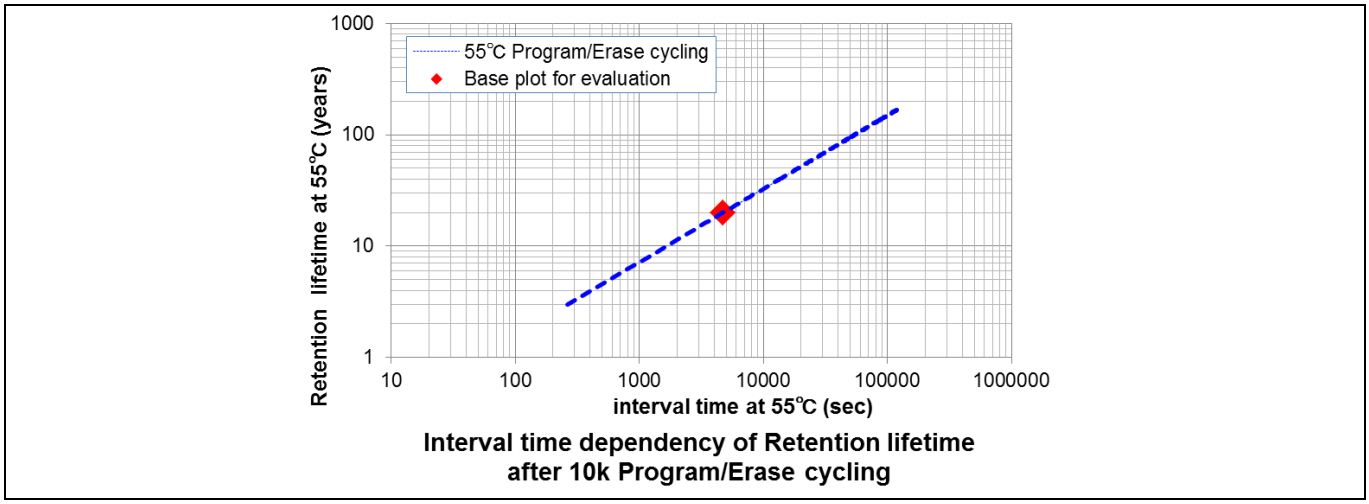

Figure 8 Retention lifetime vs. interval time between cycles of 10k Program/Erase cycling

Base plot of red dot is 20 years retention lifetime after 10k Program/Erase cycles at 55 degree Celsius under JEDEC test condition.

The slope of interval dependency came from empirically collected data.

The following interpretation applies to **Figure 8**:

- Assume that the time required to complete 10k Program/Erase cycling is spread over 20 years at 55 degree Celsius in field. (1~2 Program/Erase cycles per day)
- Average interval time between Program/Erase cycles = 20 (years) x 8760 (hours per a year) x 3600 (seconds per hour) / 10000 (Program/Erase cycles) = 63072 (seconds)
- Calculated Retention lifetime = 110.5 (years) at 55 degree Celsius
- Total product lifetime = 20 (years for Program/Erase cycling period) + 110.5 (years for data retention after 10k Program/Erase cycles) = 130.5 (years)
- Slope between data retention and interval time = 0.66

Note: The assumption uses an average interval time between Program/Erase cycles. In field usage, there is a biased frequency about interval time between Program/Erase cycles.

6 Considerations w.r.t field usage model

As a prerequisite, the baseline expectation for data retention is two years after 100k Program/Erase cycles at 55 degree Celsius and 20 years after 10k Program/Erase cycles at 55 degree Celsius in this section. Here, we present case studies for the usage models based on these assumptions.

6.1 Case study 1

Figure 9 shows two representative curves. One is the retention lifetime after 10k Program/Erase cycles at each field average temperature and another one is the retention lifetime after 100k Program/Erase cycles at each field average temperature, based on a 1.5 year of Program/Erase cycling period (10k or 100k cycles will have completed at 1.5 years). This results in a cycling interval time for 10k Program/Erase cycling of 1.314 hours and 100k Program/Erase cycling of 7.884 minutes.

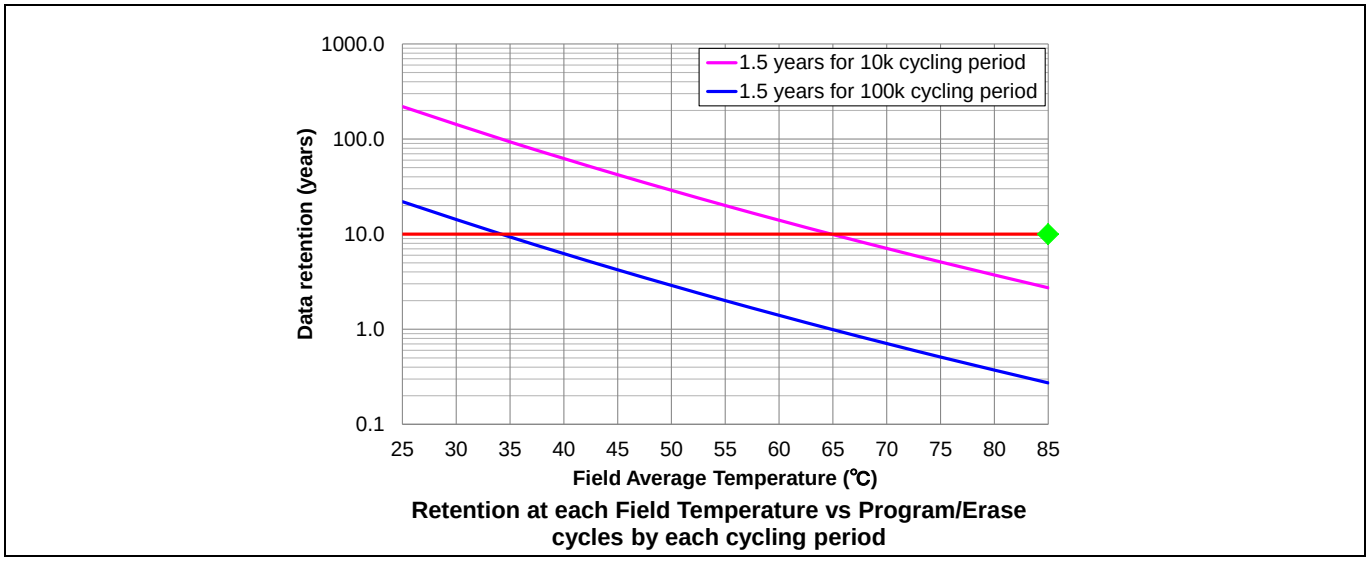

Figure 9 Retention Lifetime at Each Field Temperature versus Program/Erase Cycles by Each Interval Time

- The bright green dot shows 10 years of data retention after 2728 Program/Erase cycles at 85°C.
- Over 10 years of data retention is achieved when one assumes less than 65 degree Celsius average field temperature for 10k Program/ Erase cycles.
- Over 1 year of data retention is achieved when one assumes less than 65 degree Celsius average field temperature for 100k Program/ Erase cycles.

6.2 Case study 2

The retention lifetime after Program/Erase cycling becomes better when one considers a longer interval time between Program/Erase cycles. As an example, **Figure 9** becomes **Figure 10** when 10k and 100k Program/Erase cycles are completed over a 10 year or 20 year period.

Assumption of 10 years Program/Erase cycling period

10k Program/Erase cycling case – 8.76 hours interval time between Program/Erase cycles

100k Program/Erase cycling case – 52.56 minutes interval time between Program/Erase cycles

Assumption of 20 years Program/Erase cycling period

10k Program/Erase cycling case – 17.52 hours interval time between Program/Erase cycles

100k Program/Erase cycling case – 1.752 hours interval time between Program/Erase cycles

Note: *Interval time is approximate.*

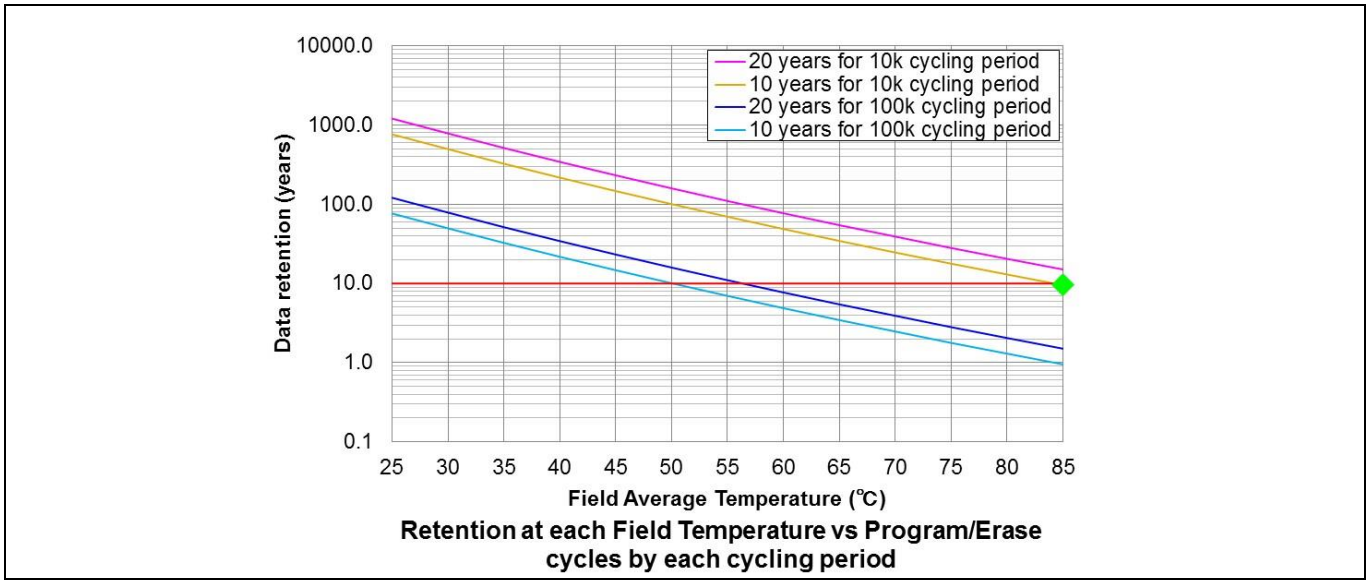

Figure 10 Retention lifetime at each field temperature vs. Program/Erase cycles by each interval time

- The bright green dot shows 10 years of data retention after 10k Program/ Erase cycles at 85 degree Celsius when the Program/ Erase cycling period is distributed over 10years.
- Over 10 years of data retention is achieved after 10k Program/Erase cycling when one assumes less than 85 degree Celsius average field temperature and Program/Erase cycling performed over 10 years.
- Over 10 years of data retention is achieved after 100k Program/Erase cycles when one assumes less than 57 degree Celsius average field temperature and Program/Erase cycling performed over 20 years.

Data retention becomes better if the usage model takes a longer Program/Erase interval time and/or longer Program/Erase cycling period. Infineon guarantees minimum retention lifetime after Program/Erase cycling with proper Program/ Erase cycling period based on the evaluated data for using the JEDEC test procedure. Infineon can provide the possibility and/or ability of data retention after Program/Erase cycling based on more detailed usage model analysis and empirical data if a realistic usage mode in field is provided.

7 Error correcting code (ECC)

ECC can significantly improve the quality and reliability of NOR Flash family products, as shown in **Figure 11**. For ultra-high quality and reliability applications, it is recommended to use ECC to improve the reliability and data retention dramatically.

As shown in **Figure 11**, it allows a 1E-08 RBER (raw bit failure rate) to meet 10 ppm unit failure rate when 1-bit ECC per 32 bytes is used.

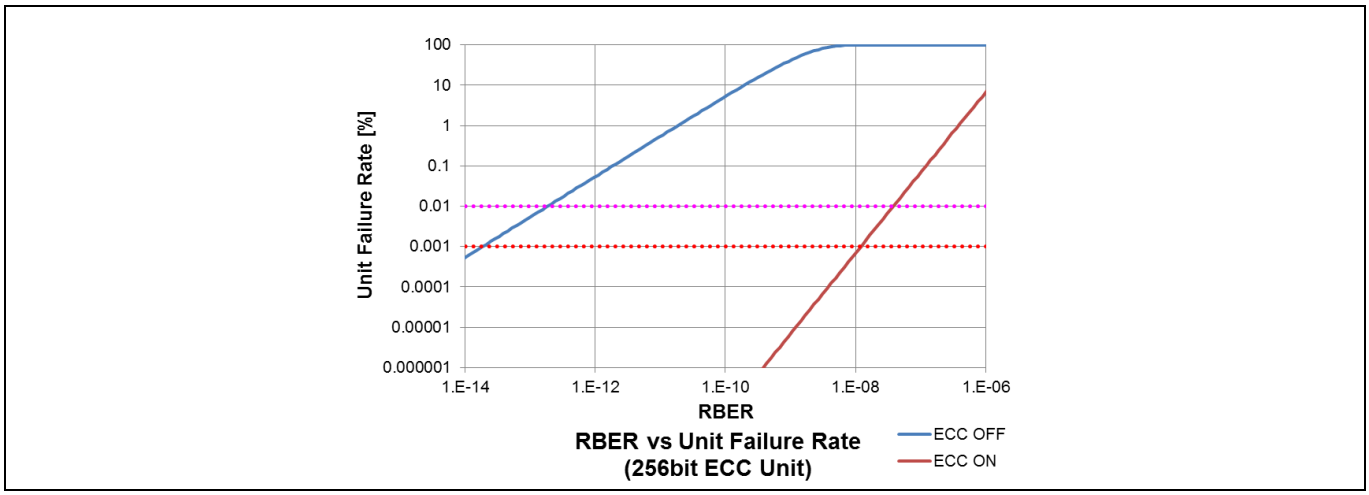

Figure 11 Unit failure rate vs. RBER

8 Summary

Endurance and data retention specifications are to be used as guidelines for designers to assess the ability of specific flash devices to meet end-of-life application requirements. Endurance and data retention are inter-dependent parameters. The effect of Program/Erase cycling can be mitigated by manipulation of how repetitively captured data is physically stored in flash memory array.

Data retention is a cell-level specification that indicates how long data can be expected to be reliably retrieved following programming under the usage model. The factors of endurance, system temperature in field, total number of Program/Erase cycling, and cycling interval time between Program/Erase cycles combined characterize the capability of flash memory. It should be noted that these factors can be controlled at the system level, provided that a good understanding of key factors is achieved.

If your application has a complex temperature profile, usage model, and/or utilizes stringent conditions, contact Infineon to obtain assistance to calculate data retention.

Revision history

Document version	Date of release	Description of Changes
**	2017-03-21	New application note.
*A	2017-05-29	Removed “confidential” marking from the footer Corrected tab in Figure 6 Optimized tab in Figure 7 Optimized to show the explanation of right side for Figure10
*B	2021-04-19	Updated to Infineon template

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