AN217000

Programmer's Guide for Cypress S25FL-L Serial NOR Flash Products

Author: Suhail Zain

Associated Part Family: S25FL-L

S25FL-L Serial NOR Flash family is Cypress's first high-performance multiple input/output Serial Flash memory product manufactured on 65-nm Floating Gate NOR technology. AN217000 describes, for software programmers and system engineers, how to use the S25FL-L family and successfully integrate it in their systems.

1 Introduction

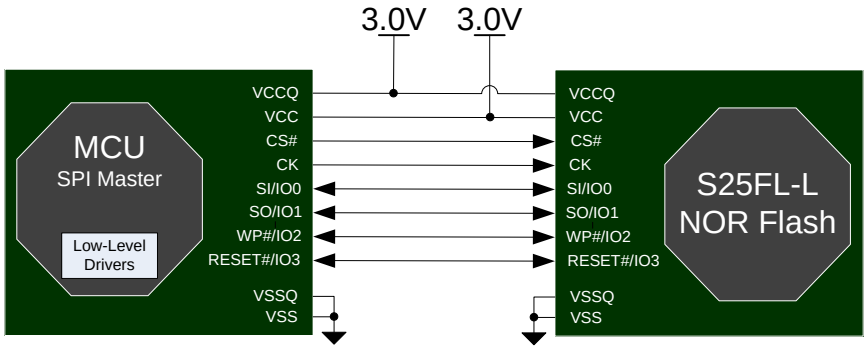
This document provides guidelines for integrating the S25FL-L Serial NOR Flash family of products into a system. For complete specifications, please refer to the datasheets.

2 S25FL-L Family Overview

S25FL-L is a 3.0-V, single-supply family of Serial NOR Flash memory products based on the advanced 65-nm Floating Gate process technology. This family pairs low signal count with a high-speed SPI-compatible bus interface. It features an advanced write protection logic and high-performance dual and quad input/output instructions for higher serial transfer speeds. Read bandwidth is further enhanced through Double Data Rate (DDR) instructions that transfer data on both edges of the clock.

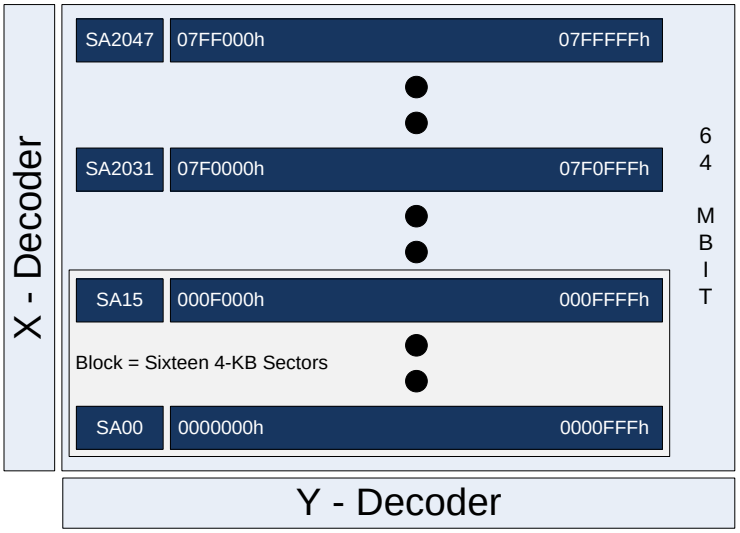
Figure 1 shows how a SPI master connects to an S25FL-L flash chip (SPI slave). Cypress provides the Low-Level Driver (LLD) software that enables read, program, and erase functions.

Figure 1. SPI Master Controller to S25FL-L



The S25FL-L family has a uniform sector architecture with a sector size of 4 KB, where a sector is the smallest erasable region. The S25FL-L family also defines Blocks (64 KB) and Half Blocks (32 KB) which are of 16 and 8 sectors respectively. Sector, Half Block, Block, and Chip erase instructions are available. Figure 2 shows the array block architecture of the S25FL064L device. Higher-density devices follow a similar architecture.

Figure 2. S25FL064L Array Architecture



S25FL-L devices have an internal 256-byte Page Programming Buffer, which is aligned by Page Program commands to a 256-byte page address in the Flash device. The Page Programming scope ranges from 1 byte to 256 bytes of the Page.

Device internal operations, such as erasing or programming, take a certain amount of time to complete and are called Embedded Operations (EO). During an EO, the device is busy and it ignores most commands. Read Status Register commands are used to determine the completion of the EO.

Read commands can start from any byte address in the memory array. The address is internally incremented to the next higher address in a sequential order after each byte is shifted out. The address automatically rolls over at the high address end of the Flash array to 000000h. Therefore, it is possible to read the entire memory array using a single read instruction that starts at any Flash address.

3 Status Register

S25FL-L has two 8-bit Status Registers that the host system can use to check the current state of the device, EO error status, or suspend status. Table 1 shows the Status Registers and their states.

Table 1. Status Registers and Default States

Status Register	Register Bit	Description	Possible States
1	WIP	Write in Progress - Device Busy	0 = Device Ready - No EO in Progress 1 = Device Busy - EO in Progress
2	E_ERR	Erase Error Occurred	0 = No Erase Error Occurred 1 = Erase Error Occurred
	P_ERR	Programming Error Occurred	0 = No Program Error Occurred 1 = Program Error Occurred
	ES	Erase Suspend	0 = Not in Erase Suspend Mode 1 = In Erase Suspend Mode
	PS	Program Suspend	0 = Not in Program Suspend Mode 1 = In Program Suspend Mode

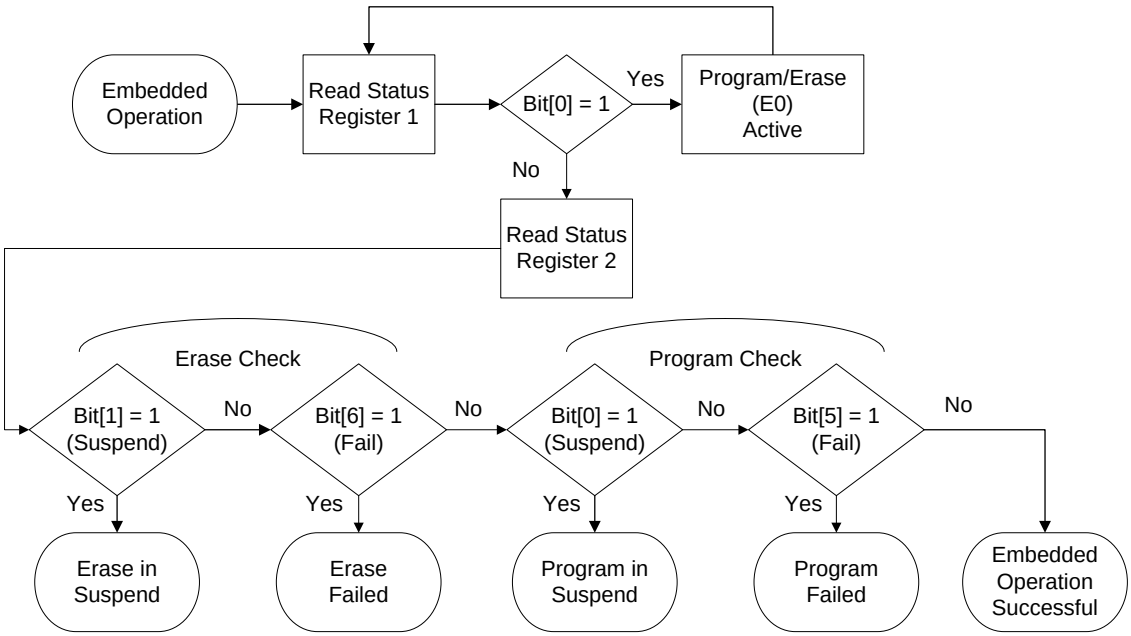
After issuing a command that triggers an EO, such as programming or erasing a sector, you should always check the Status Registers (SRs) to make sure that the EO has completed before proceeding to the next command. During an EO, only the program/erase suspend command or the Status Register Read command will be accepted. The device ignores all other commands.

Note: During a program or erase operation, you may issue a suspend command to suspend the EO in order to quickly go back to the read mode. The operation will be suspended until the resume command is entered.

If an error occurs during an EO, you must clear the error bit by using the Clear Status Register command before proceeding to the next command.

Figure 3 shows a polling function that uses the Status Register to determine the device status after starting an EO such as programing or erasing a sector. The algorithm here does not need to know the type of operation it is polling for.

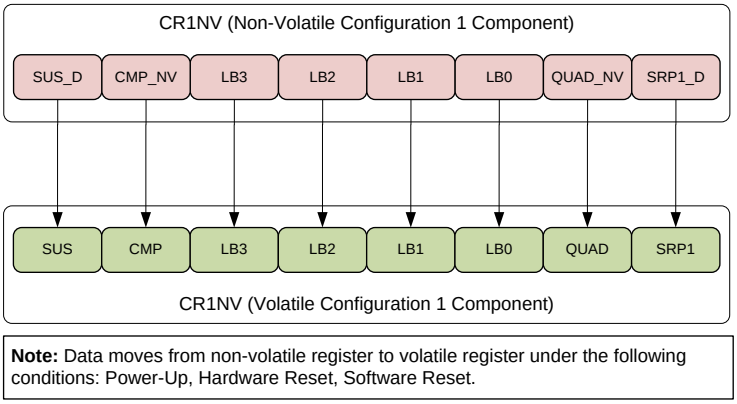
Figure 3. Status Polling Algorithm



4 Configuring S25FL-L Devices

S25FL-L devices have three 8-bit Configuration Registers. These devices provide Non-Volatile Configuration Registers (CR*NV) that are mapped bit-wise to their counterparts, Volatile Configuration Registers (CR*V). The CR*NV and CR*V registers are collectively referred to as the Configuration Register. Use CR*V registers to temporarily change configuration settings that persist until a register reset happens. The CR*V values will be reset to the corresponding bit values held in the CR*NV register after the next power cycle Power-On Reset (POR), hardware reset (RESET#), or software reset (99h). If a new non-volatile configuration is desired, the CR*NV register should be updated to the desired value through the Write Registers command (WRR 01h). Figure 4 shows how the Non-Volatile and Volatile register counterparts are related for Configuration Register 1. Configuration Registers 2 and 3 work in the same way.

Figure 4. Configuration Register Architecture



Note: Data moves from non-volatile register to volatile register under the following conditions: Power-Up, Hardware Reset, Software Reset.

Table 2 shows the default Configuration Register states from factory. Once the custom power-up default configuration has been set and fully debugged during the development phase, the CR1NV[0] SRP1 bit can be changed from '0' to '1' to permanently lock the configuration registers. The best practice during production is to program the Flash image as the first step, and to set and lock the configuration registers and Status Register 1 as the last step; the WRR (01h) command should never be used thereafter.

Table 2. Configuration Registers and Their Default States

Configuration Register	Register Bit	Description	Default Setting
1	SUS	Suspend Status - Read Only	0 - Erase/program Not Suspended
	CMP	Complement Protection Selection	0 - Normal Protection Map
	LB[3:0]	Security Region Lock Bits	000 - Security Regions Not Locked
	QUAD	Quad I/O mode Selection	0 - Dual or Serial Mode
	SRP1	Status Register Protection Selection	0 - Registers Unlocked
2	IO3R	IO3_Reset Selection	0 - Disabled - IO3 has no Alternate Function
	OI[1:0]	Output Impedance Selection	11 - Default (Refer to Device-Specific Datasheet)
	QPI	QPI Mode Selection	0 - QPI Disabled - Legacy SPI Protocols in use
	WPS	Data Protection Mechanism Selection	0 - Legacy Block Protection
	ADP	Address Length Selection	0 - 3-Byte Address
3	WL	Wrap Length Selection	11 - 64-Byte Wrap
	WE	Wrap Length Enable	1 - Wrap Disabled
	RL	Read Latency Selection	1000 - Default (Refer to Device Specific Datasheet)

4.1 After All Configurations Are Set

Table 2 shows the default Configuration Register states from factory. Once the power-up default configuration has been determined and fully debugged, you can send the CR1NV[0] SRP1 command to lock the registers. After the host programs the bit to a '1', the device configuration is permanently locked.

Note: SPR1 also locks Status Register 1. You must ensure the desired Status Register 1 behavior is determined and set before enabling SPR1.

5 Reset

There are three kinds of resets in S25FL-L devices: Power on Reset (POR), also called Cold Reset; Hardware Reset, also called Warm Reset triggered by the RESET# or IO3/RESET# signals; and the Software Reset triggered by the Software Reset Command (RSTEN 66h, RESET 99h) sequence. A Cold Reset loads all CR*V bit values from their corresponding CR*NV bit values and takes 300 µs to complete. Warm Reset and Software Reset also restore the device to its initial power up state, by reloading CR*V registers from CR*NV default values. However, the volatile SRP1 bit in the Configuration Register CR1V[0] and the volatile NVLOCK bit in the Protection Register are not changed. Warm Reset and Software Reset take 100 µs to complete. Software Reset will not affect any ongoing EOs; however, a Warm Reset will force an abort.

6 Maximizing Read Performance

In order to maximize the read performance, you may want to read the maximum length of contiguous data in a single read command sequence to avoid multiple read commands. To achieve this, the host controller should hold CS# LOW and continue to clock until all data is read. During this operation, you cannot simply use memcpy() or similar read functions that reads one byte at a time. You will need to implement a controller-specific function to read multiple bytes of contiguous data for the application-level software. This function should accept data length as one of the parameters and have the host memory controller-specific register settings necessary for the memory controller to send the correct signal protocol sequence to the S25FL-L memory.

7 Maximizing Programming Performance

S25FL-L family devices have a 256-byte write buffer, which is aligned on 256-byte boundaries (Pages). Programming data to the Flash is most efficient when writing in the 256-byte length and aligned increments. Although smaller writes are allowed, for best performance, software should, whenever possible, program data in full, address-aligned, write buffer increments.

8 Secure Silicon Region

S25FL-L devices have a 1024-byte addressable secure space called Secure Silicon Region (SSR) that is separate from the main Flash array. SSR is divided into four, individually lockable 256-byte regions. You can access the SSR by entering the SSR access instructions (SECRE Erase - 44h, SECRP Program - 42h, SECRR Read - 48h).

If data permanency is required in SSR, use the four Lock bits in the Configuration Register 1 (CR1NV, CR1V) that can be individually programmed (set to '1') to prevent any further erasing/programming of SSR regions. SSR regions 2 and 3 are special and allow added protection against erasing/programming through the Protection Register (PR) NVLock bit and the Password Protection Bit in the Individual and Region Protection (IRP) register.

Table 3 summarizes the SSR protection schemes.

Table 3. SSR Protection Schemes

SSR Region	CR1[2] Lock Bit 0 LB0 (OTP)	CR1[3] Lock Bit 1 LB1 (OTP)	CR1[4] Lock Bit 2 LB2 (OTP)	CR1[5] Lock Bit 3 LB3 (OTP)	PR[0] NVLOCK (Volatile)	IRP[2] PWDMLB Password Protection (OTP)
Region 0	Erase/ Program Protected					
Region 1		Erase/ Program Protected				
Region 2			Erase/ Program Protected		Erase/ Program Protected	Erase/Program Protected
Region 3				Erase/ Program Protected	Erase/ Program Protected	Read/Erase/ Program Protected

9 Conclusion

Cypress's S25FL-L family of Serial NOR Flash provides an easy transition from previous generations of SPI NOR devices, reduces the system cost, and helps achieve better system performance. Contact Cypress Customer Support for additional help when using S25FL-L family devices.

10 Related Documents

Table 4. Cypress NOR Flash Product Specific Datasheets

Product Family	Spec. Number	Title
FL-L Family	002-12878	S25FL064L Flash Datasheet - 64-Mbit (8-Mbyte) 3.0 V FL-L SPI Flash Memory
FL-L Family	002-00124	S25FL256L/S25FL128L, 256 Mbit (32 Mbyte)/128 Mbit (16 Mbyte), 3.0 V FL-L Flash Memory

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5509825	SZZX	11/11/2016	New Application Note
*A	5817574	AESATMP8	07/14/2017	Updated logo and Copyright.

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