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AN2161

PSoC® 1-Based Voltage-to-Frequency Converter

Author: Victor Kremin
Associated Project: Yes
Associated Part Family: CY8C29x66, CY8C28xxx, CY8C27x43, CY8C24x94 CY8C24x23A, CY8C24x33, CY8C23x33
Software Version: PSoC Designer™ 5.4 SP1 and higher
Related Application Notes: AN75320, AN2041

To get the latest version of this application note, or the associated project file, please visit http://www.cypress.com/AN2161.

AN2161 describes two methods for implementing a continuous time (CT) voltage-to-frequency (V/F) converter using the PSoC® 1 device. Both methods are implemented in hardware, and the CPU is not used during the operation.

Contents

1 Introduction

V/F converters are widely used in applications such as industrial electronics, frequency-shift keying modulators, phase-locked loop systems, analog-to-digital converters, and isolation amplifiers. Even though these converters are produced as standalone devices, they still require several external components and are relatively expensive compared with modern, low-cost analog integrated circuits.

The PSoC 1 device allows you to build a V/F converter with minimal external analog components. All the digital blocks, and the CPU, are at your disposal. This application note describes two methods of V/F conversion:

- Comparator-Based V/F Converter
- Integrator and Schmitt Trigger–Based V/F Converter

The comparator-based V/F converter uses two passive external components: a resistor and a small integrating capacitor. The advantage of this method is the high-frequency operation. However, the disadvantage is that the response curve of frequency versus voltage is not linear.

The integrator and Schmitt trigger–based V/F converter uses two analog PSoC blocks: a switched capacitor (SC) block as an integrator and a CT block as a Schmitt trigger. The advantage of this method is linear operation. The limitations of this method are the following:

- Low operation frequency (up to 10 kHz)
- A jitter in the output signal, so it is not suitable for audio applications

Two types of waveforms, square wave and triangular, can be obtained with both the circuits described in this application note.

This application note assumes that you are familiar with the PSoC 1 device architecture and the PSoC Designer™ Integrated Design Environment (IDE). If you are new to PSoC 1, refer to AN75320 – Getting Started with PSoC 1 to explore the PSoC 1 architecture and development tools.

2 PSoC Resources

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and quickly and effectively integrate the device into your design. In this document, PSoC refers to the PSoC 1 family of devices. To learn more about PSoC 1, refer to the application note AN75320 - *Getting Started with PSoC 1*.

The following is an abbreviated list for PSoC 1:

- **Overview:** PSoC Portfolio, PSoC Roadmap
- **Product Selectors:** PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP. In addition, PSoC Designer includes a device selection tool.
- **Datasheets:** Describe and provide electrical specifications for the PSoC 1 device family.
- **Application Notes and Code Examples:** Cover a broad range of topics, from basic to advanced level. Many of the application notes include code examples.
- **Technical Reference Manuals (TRM):** Provide detailed descriptions of the internal architecture of the PSoC 1 devices.
- **Development Kits:**
  - CY3210-PSOCEVAL1 Kit enables you to evaluate and experiment Cypress's PSoC 1 programmable system-on-chip design methodology and architecture.
  - CY8CKIT-001 is a common development platform for all PSoC family devices.
  - CY3215A-DK In-Circuit Emulation Lite Development Kit includes an in-circuit emulator (ICE). While the ICE-Cube is primarily used to debug PSoC 1 devices, it can also program PSoC 1 devices using ISSP.
- The MiniProg1 and MiniProg3 devices provide an interface for flash programming.

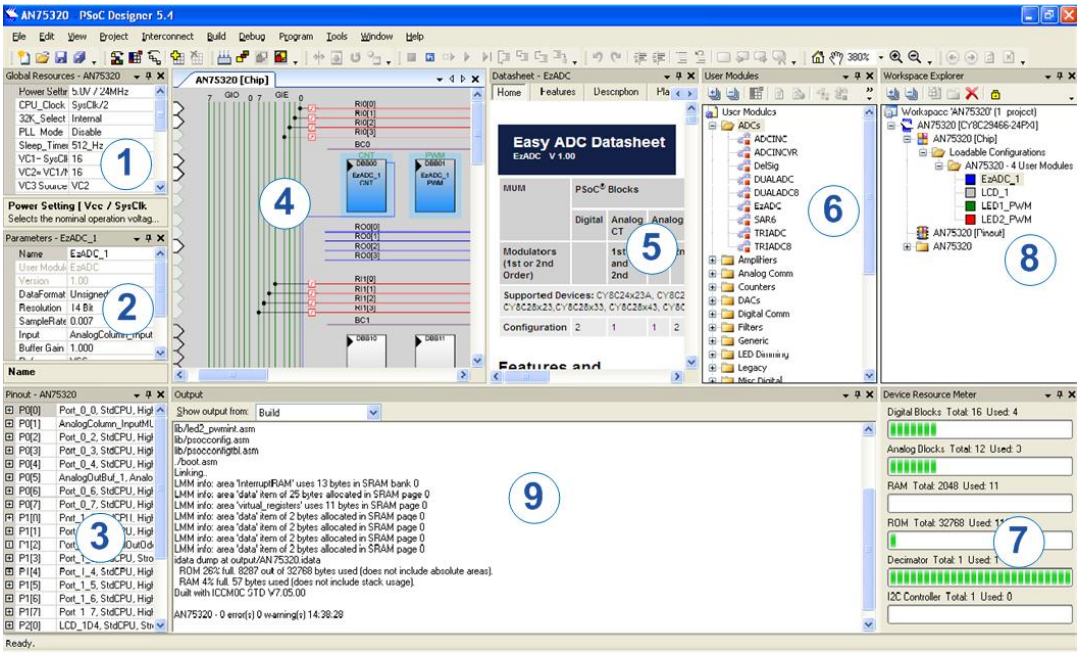
2.1 PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. Figure 1 shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources –** all device hardware settings.
2. **Parameters –** the parameters of the currently selected User Modules.
3. **Pinout –** information related to device pins.
4. **Chip-Level Editor –** a diagram of the resources available on the selected chip.
5. **Datasheet –** the datasheet for the currently selected UM
6. **User Modules –** all available User Modules for the selected device.
7. **Device Resource Meter –** device resource usage for the current project configuration.
8. **Workspace –** a tree level diagram of files associated with the project.
9. **Output –** output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to **PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide**.

Figure 1. PSoC Designer Layout



2.2 Code Examples

The following webpage lists the PSoC Designer based Code Examples. These Code Examples can speed up your design process by starting you off with a complete design, instead of a blank page and also show how PSoC Designer User modules can be used for various applications.

http://www.cypress.com/go/PSoC1Code Examples

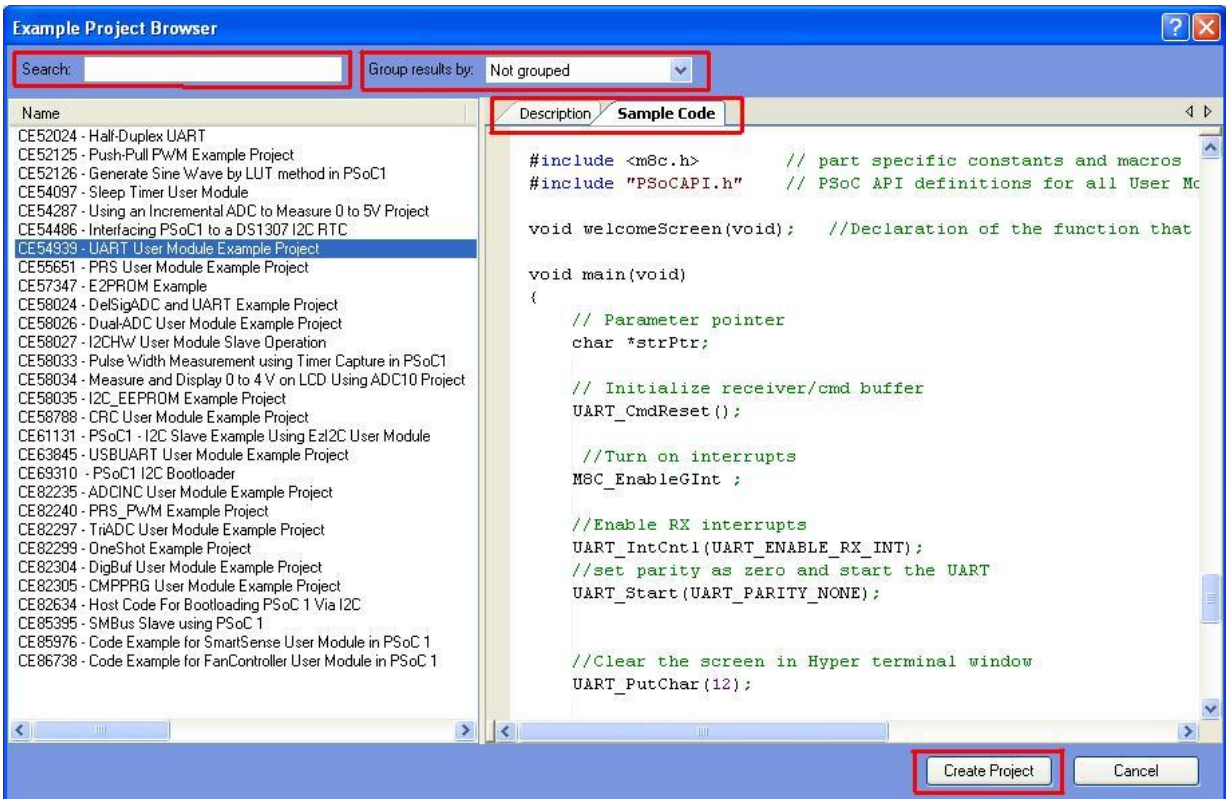
To access the Code Examples integrated with PSoC Designer, follow the path **Start Page > Design Catalog > Launch Example Browser** as shown in Figure 2.

Figure 2. Code Examples in PSoC Designer

In the Example Projects Browser shown in Figure 3 you have the following options.

- Keyword search to filter the projects.
- Listing the projects based on Category.
- Review the datasheet for the selection (on the Description tab).
- Review the code example for the selection. You can copy and paste code from this window to your project, which can help speed up code development, or
- Create a new project (and a new workspace if needed) based on the selection. This can speed up your design process by starting you off with a complete, basic design. You can then adapt that design to your application.

Figure 3. Code Example Projects, with Sample Codes



2.3 Technical Support

If you have any questions, our technical support team is happy to assist you. You can create a support request on the Cypress Technical Support page.

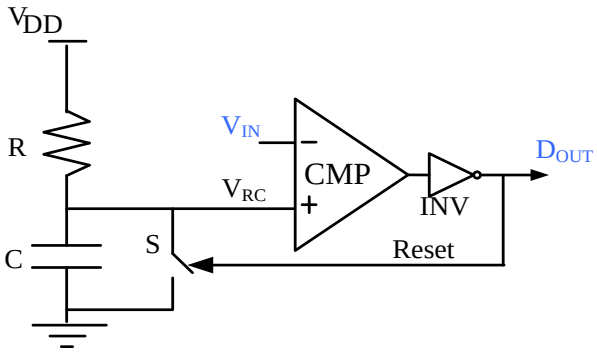
You can also use the following support resources if you need quick assistance.

- Self-help
- Local Sales Office Locations

3 Comparator-Based V/F Converter

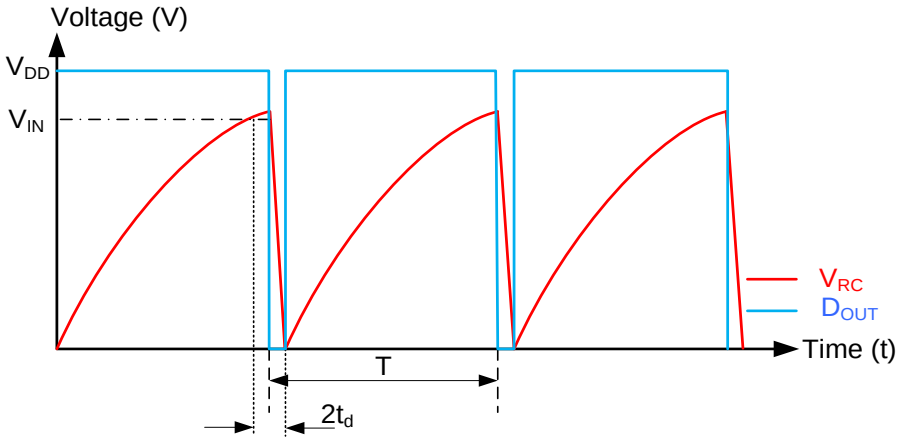
The circuit for the comparator-based V/F converter is provided in Figure 4. In the figure, the analog voltages are denoted by "V_{xx}" and the digital values are denoted by "D_{xxx}". Switch S is open when the output D_{OUT} is high, and thus Reset is high, and closed when D_{OUT} is low.

Figure 4. Comparator-Based V/F Converter



To understand the operation, consider the initial condition of capacitor C as a discharged state. The output signal D_{OUT} is high, and thus switch S is open. Capacitor C is exponentially charged, as shown in Figure 5, through resistor R.

Figure 5. Output and RC Waveforms



When the voltage on capacitor C, $V_{RC,}$ crosses the threshold level (V_{IN}), the comparator output, $D_{OUT,}$ switches to low. Since the output, and thus Reset, are low, switch S is closed. In this state, capacitor C discharges through the closed switch path. Thus the circuit returns to the initial state and repeats the process. And the digital signal, $D_{OUT,}$ goes through a cycle of high and low, with the period dependent on the input voltage, $V_{IN.}$ Period T and delay t_d are explained in Circuit Operation section.

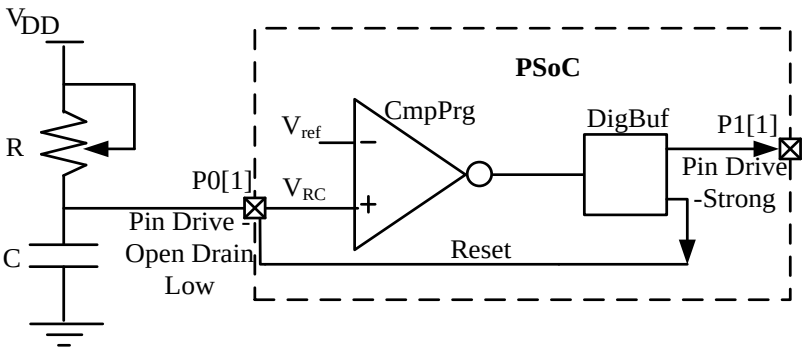
3.1 PSoC Implementation

The circuit discussed in this application note is built in PSoC 1 using the following blocks:

- Programmable comparator, CmpPrg, for CMP
- Inverter in comparator bus for INV
- Open drain low switch in a digital pin for S
- External resistor for R
- External capacitor for C

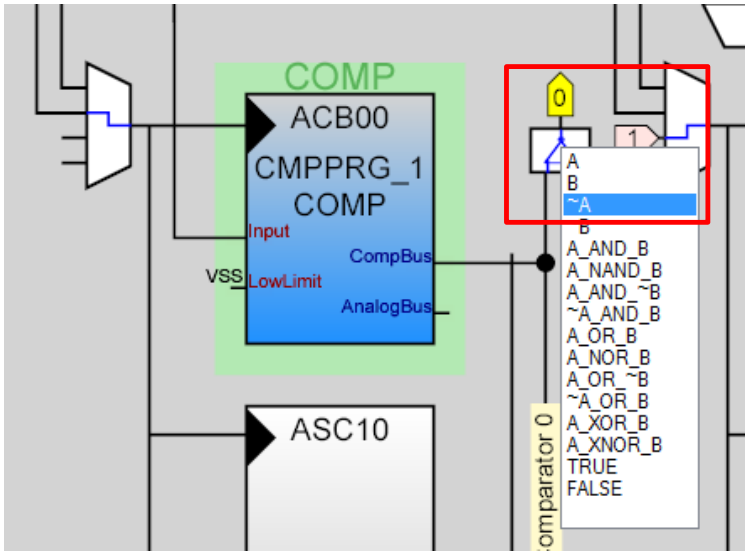
The block diagram of the implementation in PSoC 1 is shown in Figure 6. The digital buffer (DigBuf) is used to provide the flexibility to route the digital output signal to any pin on the package. This block is optional and can be saved by directly connecting the output of the comparator to the global bus by writing to register CMP_GO_EN. A complete description of this register is available in the PSoC 1 Technical Reference Manual (TRM).

Figure 6. V/F Converter with Internal Voltage Input



Note that the digital signal from CmpPrg must be inverted. In the project A.1 Example 1: Comparator-Based V/F Converter accompanying this application note, this is done by the NOT function of the comparator bus LUT, as shown in Figure 7. Other possible ways to invert CmpPrg digital signal are by using the “InvertInput1” parameter of the DigBuf User Module or the NOT function of the digital row LUT.

Figure 7. Implementation in PSoC 1 Highlighting the NOT Function



The comparator bus that is used to pass the signal from CmpPrg to the DigBuf User Module has its own latch that samples the signal. To avoid interference between the column clock and the generated signal, the comparator bus must be unsynchronized and the latches must be transparent (output tracks the input). The CMP_CR1 register is used to bypass synchronization of the comparator bus with the column clock, and the ACBxxCR2 register is used to make the comparator latch transparent. The following code illustrates the settings required. For more information on these registers, refer to the PSoC 1 TRM.

```
/* Disable comparator 1 and 2 bus synchronization with column clock */
CMP_CR1 |= COMP_BUS_SYNC_DISABLE;

/* Make the comparator control latch transparent */
CMPPRG_1_COMP_CR2 &= ~COMP_LATCH_TRANSPARENT;
```

3.2 Circuit Operation

The operation of the circuit with PSoC is same as the waveforms provided in Figure 5. The switch (S) works through a digital pin in “open drain, drive low” mode. The pin is in High-Z drive mode when the comparator output is high and in Strong mode when the output is low. Initially, capacitor C is discharged, and pin P0[1] is high. Since the pin is in High-Z, capacitor C is exponentially charged through resistor R. When the voltage on capacitor C goes higher than the threshold level, V_{ref}, the comparator (CmpPrg) trips and the output turns D_{OUT} low. Capacitor C then discharges through pin P0[1] in Strong mode. Due to the discharge of capacitor C, the output D_{OUT} goes “high,” and the circuit returns to the initial state. A periodic process is possible because of a propagation delay, t_d (about 0.1 µs), from the input of CmpPrg to the output driver. This delay allows capacitor C to discharge before the output driver is returned to the initial state. The main operation condition is that the discharge time must be less than t_d.

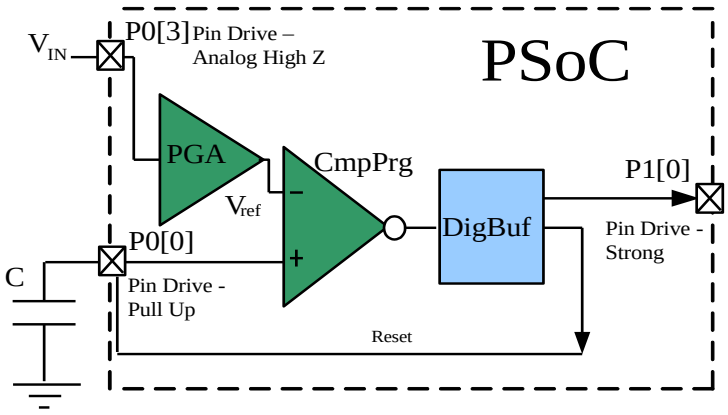
To find the period T, use Equation 1.

$$T = RC\ln\left[\frac{V_{DD}}{(V_{DD} - V_{ref})}\right] + 2t_d \quad \text{Equation 1}$$

When t_d << T, parameter t_d is ignored. If the external capacitor is comparable to the input capacitance of the pin, which is 10 pF, the sum of both capacitors must be considered. The output frequency is F = 1/T. Equation 1 shows a nonlinear relationship between frequency and voltage. Frequency depends on R, C, V_{DD}, V_{ref}, and t_d. High frequency can be achieved using the lower value of R and C. The highest frequency that can be achieved is limited by t_d.

In Figure 6, the internal reference voltage is converted into frequency. The same circuit can be used to connect the external V_{IN} to the comparator, as shown in Figure 8. Another modification shown in Figure 8 is the use of an internal pull-up resistor instead of the external resistor. In pull-up drive mode, the pin is in Resistive mode when the output is high and Strong mode when the output is low. Thus the same operation is achieved. The nominal value of an internal pull-up resistor is 5.6 kΩ. For high accuracy, use an external pull-up resistor.

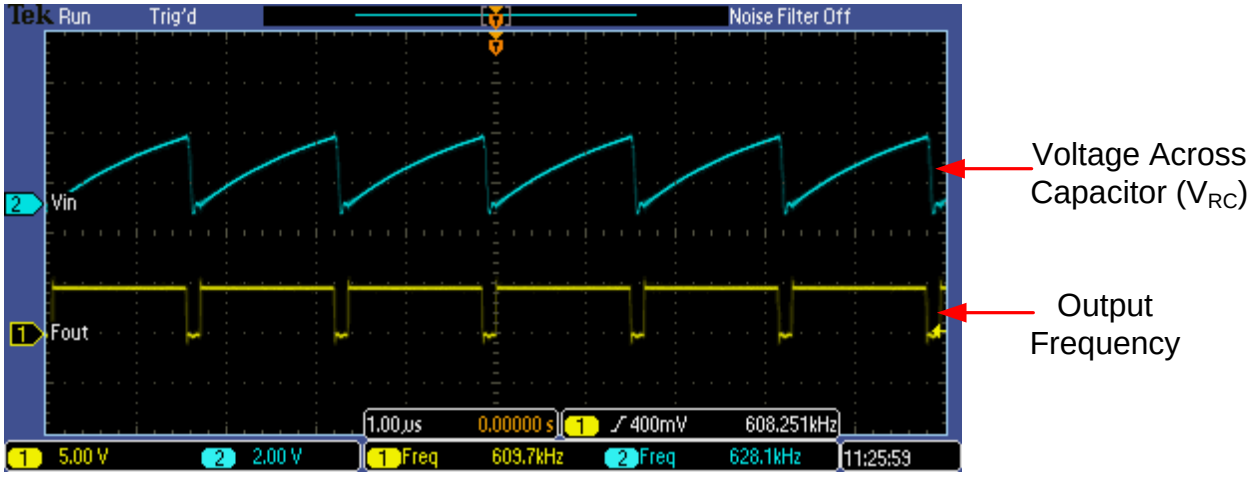
Figure 8. V/F with External Voltage Input



3.3 Test Results

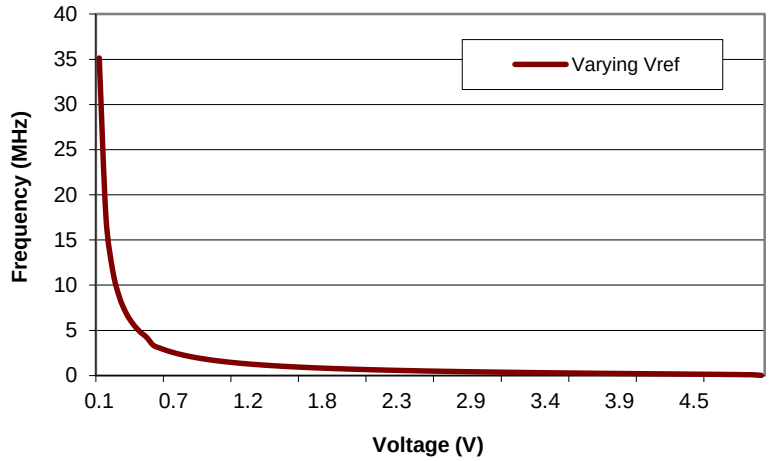
Figure 9 illustrates the test results for the schematic in Figure 6. The values used are C = 470 pF, R= 4.7 kΩ, V_{DD} = 5 V, and Vref = 2.5 V (based on the settings in CmpPrg). The expected frequency using Equation 1 is 577 kHz; the frequency observed is 609 kHz.

Figure 9. Output Waveforms of Relaxation Oscillator



In this type of implementation, the variation of frequency is not linear with voltage, as shown in Figure 10.

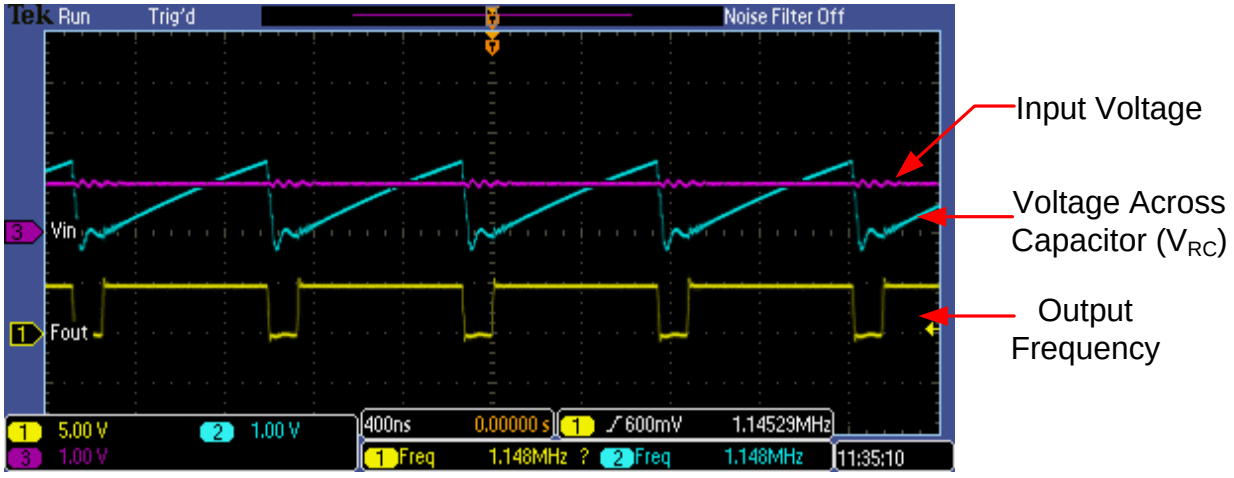
Figure 10. Frequency Variation with R and Vref



The graph is plotted with the assumption that the internal resistance is 5.6 kΩ. The Vref is calculated by the resistive divider method from Vdd.

Consider the input of PGA as V_{in} = 1 V. With the “LowLimit” of the comparator set to the output of the PGA and its “RefValue” set to 0.021, Vref = 1.1 V. The expected frequency for this setup using Equation 1 is 1.5 MHz. The measured value is 1.1 MHz, as shown in Figure 11.

Figure 11. Output Waveform of the V/F Converter



The deviation in the expected frequency from the observed frequency is because of the approximation of the pull-up resistor and the external capacitor. The capacitors are typically not precise and vary with temperature and voltage. So, the V/F relationship varies based on the variation in capacitance.

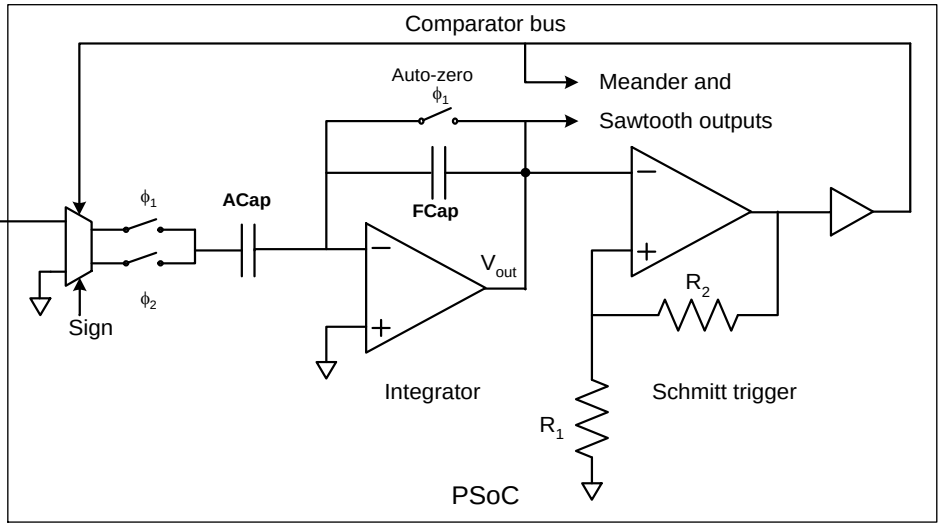
Refer to A.1 Example 1: Comparator-Based V/F Converter for details on testing the example project.

In applications that require a precise frequency for a given voltage level, a single-point calibration can be achieved with a voltage output multiplying digital-to-analog converter (MDAC). The MDAC output can be used to tune the frequency, using the internal main oscillator's reference and Vref as an input. By setting the voltage using the MDAC, the V/F relationship is more predictable.

4 Integrator and Schmitt Trigger–Based V/F Converter

The converter, shown in the block diagram of Figure 12, consists of a reversible integrator and a Schmitt trigger. The integrator has been built around a type C SC block with an analog modulator. The Schmitt trigger has been built using a CT block with internal resistors. For more details about SC block operation, see AN2041 – Understanding PSoC 1 Switched Capacitor Analog Blocks.

Figure 12. Converter Schematic Diagram



The integrator output voltage is determined by its output voltage from the previous sample and the state of the Schmitt trigger. The sign bit in the SC block is set to 1, which makes the integrator gain negative. The output state of the Schmitt trigger follows the polarity of the integrator output. When the Schmitt trigger output is negative, each column sample clock period decreases the integrator output voltage, V_{out}, by ΔV. This increment is determined by the input voltage, V_{in}, and the block ACap-to-FCap ratio:

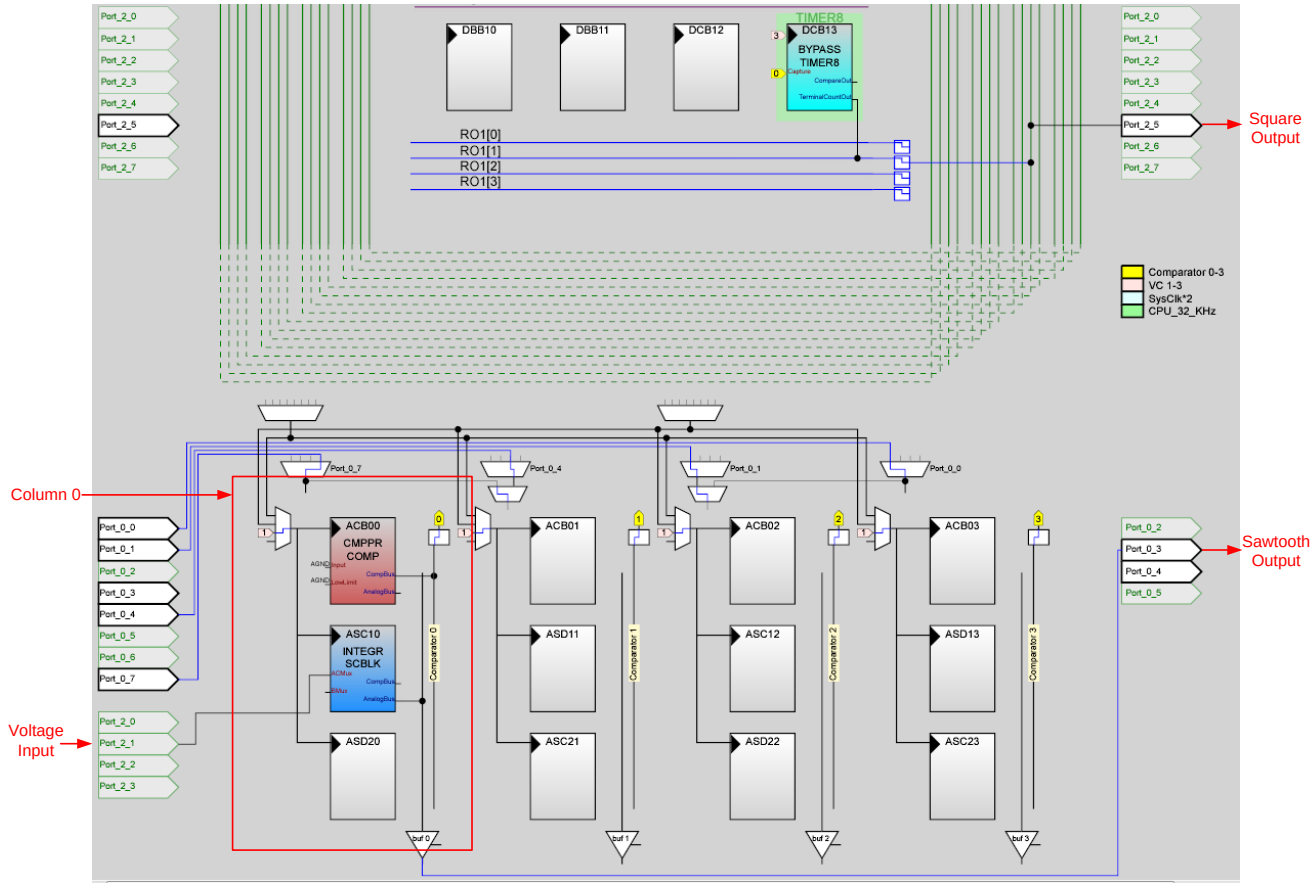
$$\Delta V = V_{in} \frac{ACap}{FCap} \qquad \text{Equation 2}$$

When V_{out} reaches the lower Schmitt trigger threshold, V^{th}_{low}, the trigger switches to the opposite state, driving the comparator bus high. This changes the integrator input voltage sign, causing the integrator signal to rise with the same ΔV at each column sample clock period. This process will continue until the integrator signal reaches the Schmitt trigger upper threshold value, V^{th}_{up}. At this point, the trigger drives the comparator bus low again, and the process is repeated.

4.1 PSoC Implementation

The V/F converter placement is shown in Figure 13. The converter is located in Column_0. The programmable threshold comparator is used to make the Schmitt trigger. The feedback resistors are rerouted manually in the firmware to the noninverting operational amplifier input. The inverting input is directly connected to the integrator output. Because the integrator uses auto-zero mode, the SC output alternates between the demanded output value and the AGND level for each clock period. However, the integrator has no influence on the converter operation due to Schmitt trigger hysteresis. You can disable auto-zero mode in the integrator when neither sawtooth signal symmetry nor 50 percent duty cycle for a rectangle signal are important. This allows larger output frequencies.

Figure 13. PSoC Internals



In this example, the integrator is located in the ASC10 block. The configurable SC block is used to make the integrator. ComparatorBus_0 is set as the modulator source. FCap is set to 32 and ACap to 1 to get the maximum possible integration steps per given input voltage. The input signal comes directly from the P2[1] input pin. The SC block serves an additional level-shifting function.

To process PSoC Vss ground-related input signals, the ARefMux reference is set to REFLO, and the RefMux is set to Vdd/2 ± Vdd/2. You should set ARefMux to AGND when you want to work with AGND-related input signals, such as those that come from another analog block. The integrator output voltage is sent to the P0[3] pin. The Timer_8 User Module is required to pass the comparator bus signal to an external pin. The timer function is changed to the CRC, and pass mode is enabled in the firmware. This module is required only when the digital V/F converter output is directly passed to an external pin. If the output is sent to another digital module, the pass block is not required.

4.2 Circuit Operation

The Schmitt trigger thresholds are determined by supply voltage, selected analog ground, and the ratio of the internal resistors. The Schmitt trigger thresholds, V^{th}_{low} and V^{th}_{up}, can be calculated easily using Equation 3 (all voltages are AGND related).

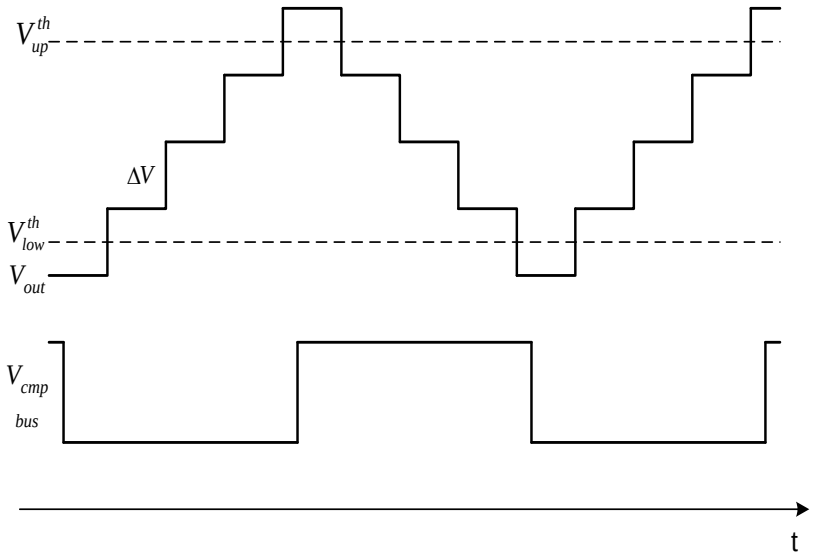
$$V^{th}_{low} = \frac{R_1}{R_1 + R_2} - V_{AGND};$$

$$V^{th}_{up} = \frac{R_1}{R_1 + R_2}\left(V_{dd} - V_{AGND}\right)$$

Equation 3

The SC integrator is a discrete system in that the integrator output voltage can be changed only during discrete time intervals. To switch the Schmitt trigger, the integrator signal should be greater than or equal to the trigger threshold. This results in two additional integration column sample clock periods for each output signal half-period integration time, as shown in Figure 14.

Figure 14. Converter Operation



The upper bound, N_{sup}, and the lower bound, N_{inf}, for the half-period integration time in units of column sample cycles can be estimated by using the following equations:

$$N_{sup} = \left[\frac{V^{th}_{up} - V^{th}_{low}}{\Delta V}\right] + 2; \quad N_{inf} = \left[\frac{V^{th}_{up} - V^{th}_{low}}{\Delta V}\right]$$

Equation 4

The [ ] denotes the integer part. The sample period for the SC block is the column clock signal, divided by 4, or:

$$T_i = \frac{4}{F_c}$$ Equation 5

F_c is the column frequency. Suppose that $N_{inf} >> 2$, $N_{cyc} = N_{inf} \sim N_{sup}$.

This takes into account that a single-period total integration time is a doubled half-period time:

$$T_{out} = 2T_i \cdot N_{cyc}$$ Equation 6

Combining Equations 2–5, the converter output frequency is given by:

$$F_{out} = \frac{F_c}{8} \times \left(1 + \frac{R_2}{R_1}\right) \times \frac{ACap}{FCap} \times \frac{V_{in}}{V_{dd}}$$ Equation 7

Note: It is useful to substitute the following:

$$\beta = \left(1 + \frac{R_2}{R_1}\right)^{-1}$$ Equation 8

This is because β can be assigned as a RefValue parameter in PSoC Designer when a programmable threshold comparator is used as a Schmitt trigger building block. So the final expression for the V/F output frequency, F_{out}, is given by:

$$F_{out} = \frac{F_c}{8\beta} \times \frac{ACap}{FCap} \times \frac{V_{in}}{V_{dd}}$$ Equation 9

A more accurate expression for the V/F converter output frequency can be obtained using the value N_{inf} for an output signal half-period integration time estimation:

$$F_{out} = \frac{F_c}{8}\left\{\beta \times \frac{V_{dd}}{V_{in}} \times \frac{FCap}{ACap} + 2\right\}^{-1}$$ Equation 10

Equation 10 shows a linear relationship between frequency and input voltage, and its frequency depends on β, V_{dd}, V_{in}, FCap, ACap, and F_c. The highest frequency of operation is limited by Fc, while other parameters are controlled by the user.

4.3 Test Results

Figure 15 illustrates the converter output signals. Figure 16 demonstrates the use of the converter as a frequency modulator.

Figure 15. Converter Output Signals

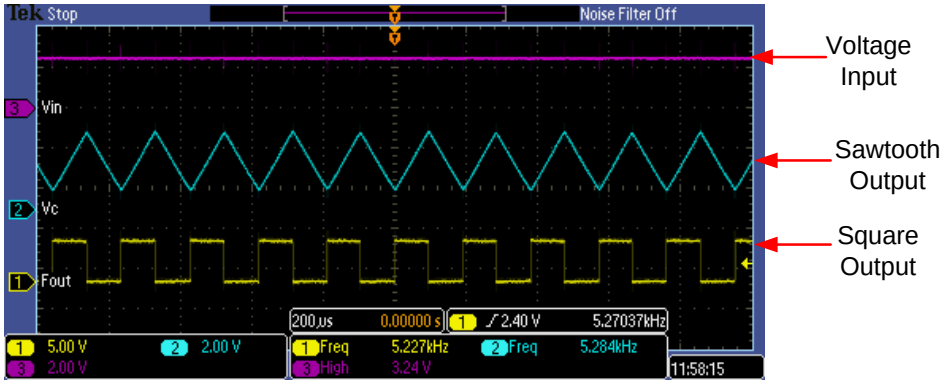
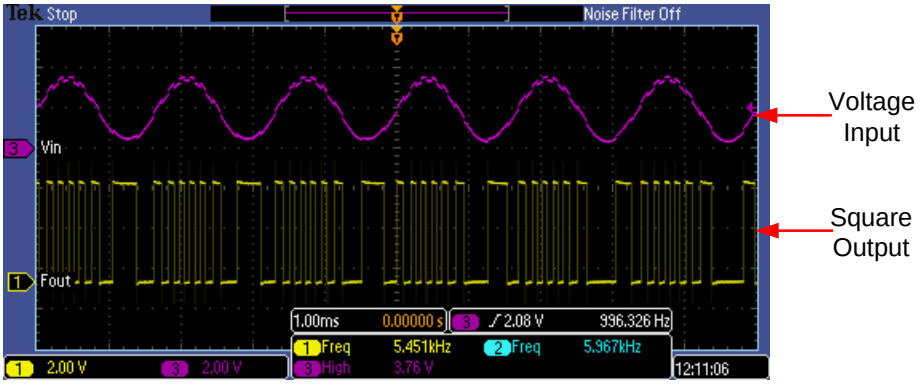


Figure 16. Converter as Frequency Modulator



To study converter transfer characteristics, the output frequency is measured for various input voltages, as shown in Figure 17. The ratio between the minimum and maximum frequency is near 100, which makes the converter suitable for many practical applications. Figure 18 depicts the transfer characteristic slope as a function of the input voltage. Note that the slope decreases with an increasing input voltage due to the constant value in the half-period integration time. See Equation 4. To examine the behavior of transfer characteristic slope with increasing input voltage, differentiate Equation 10 by V_{in}.

Figure 17. Transfer Characteristics

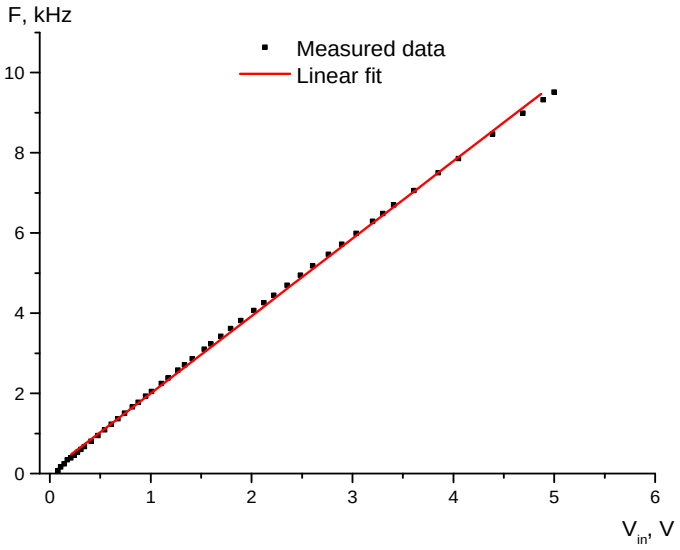
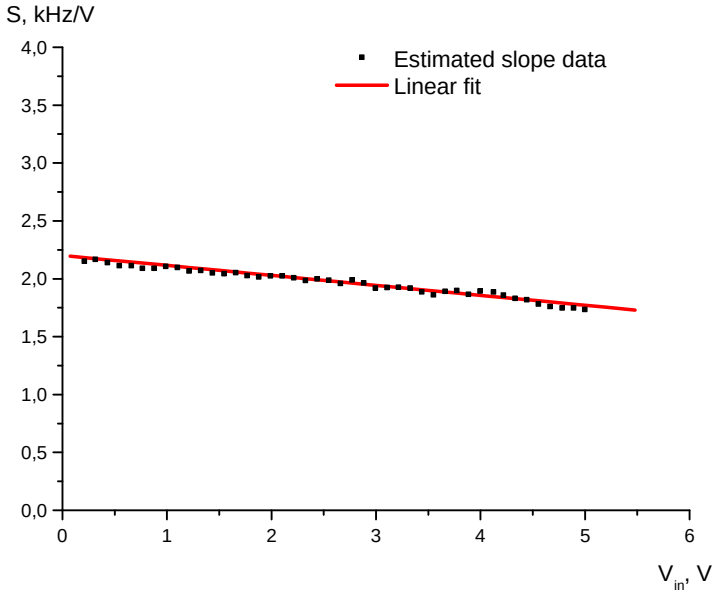
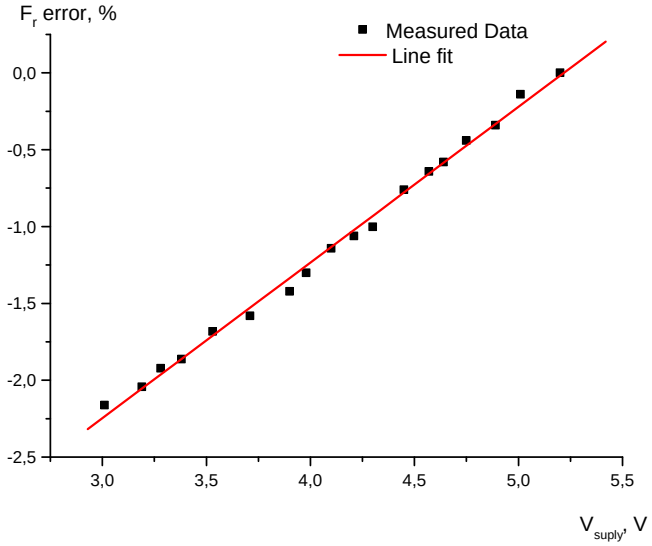


Figure 18. Transfer Characteristic Slope Versus Input Voltage



To study the influence of the power supply level on the output frequency, the PSoC supply is varied from 3.0 V to 5.25 V, and the input voltage is fixed to half the supply level. Figure 19 illustrates the relative frequency variation obtained during these measurements. The 5.25-V supply is used as a reference level.

Figure 19. Output Frequency Variation Versus Supply Level



Finally, the difference between the calculated and measured frequencies is estimated. For the 2.5-V input signal and 5-V supply level, the internal 24-MHz generator measures the frequency as 4993 Hz. The frequency calculated from Equation 9 is near 5212 Hz, which provides the relative frequency error of 4.2 percent. The primary error source is the assumption that the difference between the comparator thresholds is exactly equal to that of the integer number of the switched capacitance integrator voltage. As a result, the real half-period integration time is longer than the time evaluated by Equation 6. The more accurate Equation 10 predicts the value at 4938 Hz and the error at 1.1 percent.

Refer to Example 2: Integrator and Schmitt Trigger–Based V/F Converter for details on testing the example project.

5 Design Modifications

The proposed V/F converter can be used in various applications. Some adaptation may be required for certain situations. The integrator can be built using a CT block with an external resistor and capacitor. This will reduce possible jitter in the output signal at maximum frequencies, which improves the voltage conversion accuracy (when high-stability passive components are used) and linearity because the transfer characteristic slope is constant for the whole V_{IN} range. Because this design uses the power supply value as the converter reference voltage, the output frequency is dependent on the power supply value.

This is fine for sources such as strain gauges and some pressure sensors, which provide the ratiometric output signal, but it is problematic for devices that supply absolute voltage. In these situations, the two comparators that check the integrator signal relative to the internal reference can be used to switch a “memory cell” such as a Schmitt or LUT-based RS trigger to a control analog modulator.

6 Summary

This application note implemented a comparator-based and an integrator and Schmitt trigger–based V/F converter using PSoC 1. The advantage of the comparator-based V/F converter is its high frequency operation; its nonlinear response is a disadvantage. The integrator and Schmitt trigger–based V/F converter provides linear response, but it can be used only for frequencies less than 10 KHz. You can choose any method according to the application requirement.

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A Appendix A: Testing the Example Projects

A.1 Example 1: Comparator-Based V/F Converter

This project demonstrates a wide-range, continuous-type V/F converter implemented with a PSoC 1 CT block.

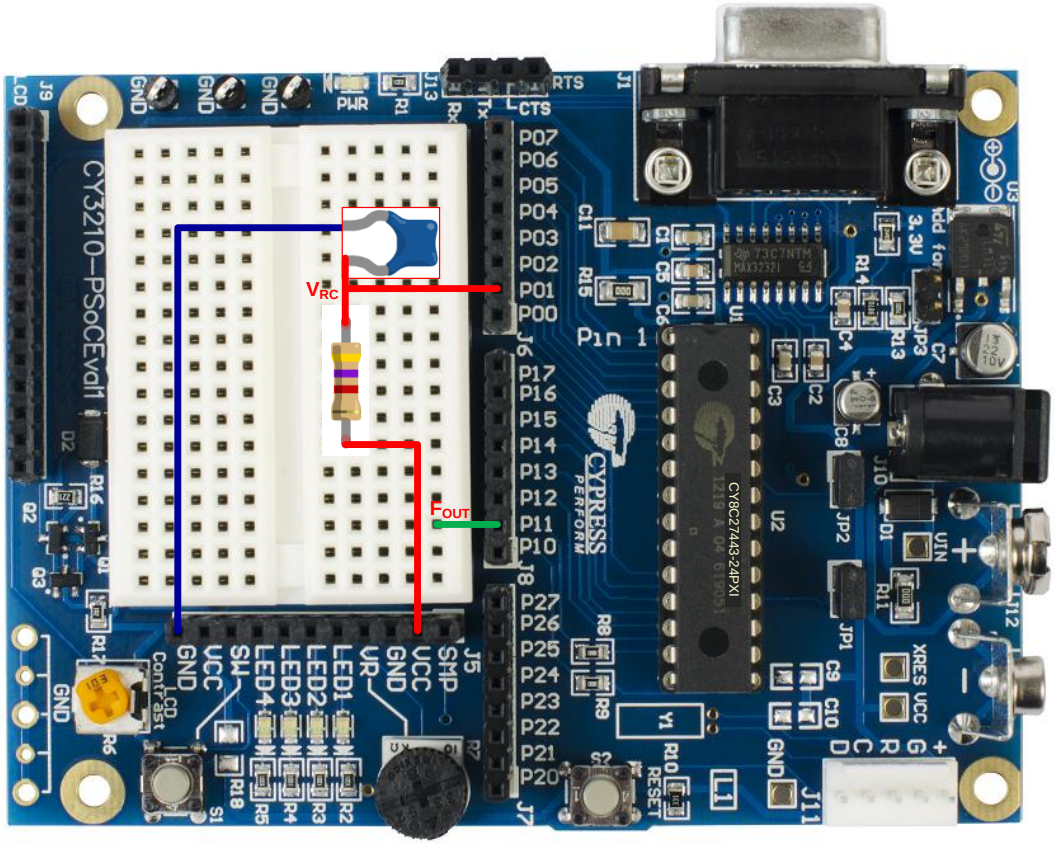
A.1.1 Hardware Required

- CY3210 PSoCEval1 with 28-pin CY8C27443-24PXI PDIP
- Discrete capacitor (470 pF) and resistor (4.7 kΩ)
- CY3217 MiniProg1 or CY8CKIT-002 MiniProg3
- Jumper wires
- Oscilloscope

A.1.2 Test Procedure

1. Insert the CY8C27443-24PXI device into the 28-pin IC socket provided on the CY3210-PSoCEval1 board.
2. Program the device using MiniProg1 or MiniProg3 with the *AN2161_Comparator_Based_VtoF.hex* file available in the root directory of the AN2161_Comparator_Based_VtoF project attached with this application note.
3. To test the project with internal input voltage, connect the 470-pF capacitor between pin P0[1] and ground. Connect the 4.7K resistor between the VCC pin on jumper J5 and pin P0[1], as shown in Figure 20.

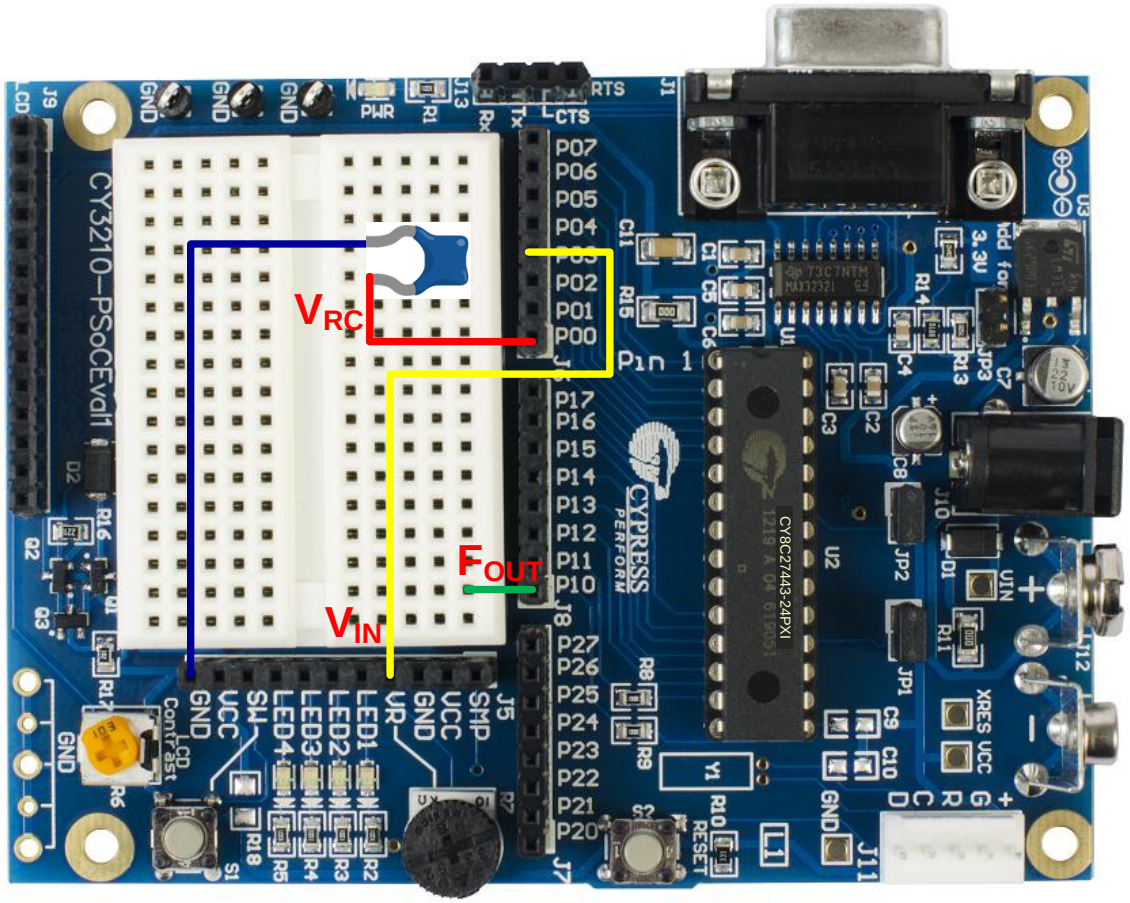
Figure 20. Hardware Connection for Testing Example 1 with Internal Input Voltage



4. Probe pins P0[1] and P1[1] to see the voltage across the capacitor and the output waveform respectively on the oscilloscope, as shown in Figure 9.

5. To test the project with external voltage input, connect the 470-pF capacitor between pin P0[0] and ground. Connect the input voltage to pin P0[3]. The input voltage can be derived from onboard potentiometer R7, as shown in Figure 21.

Figure 21. Hardware Connection for Testing Example 1 with External Input Voltage



6. Probe pins P0[3] and P1[0] to view the input and output waveform respectively on the oscilloscope, as shown in Figure 11.

A.2 Example 2: Integrator and Schmitt Trigger–Based V/F Converter

This project demonstrates a linear, continuous type of V/F converter implemented with PSoC 1 SC and CT blocks.

A.2.1 Hardware Required

- CY3210 PSoCEval1 with 28-pin CY8C27443-24PXI PDIP
- CY3217 MiniProg1 or CY8CKIT-002 MiniProg3
- Jumper wires
- Oscilloscope
- Function generator or DC power supply

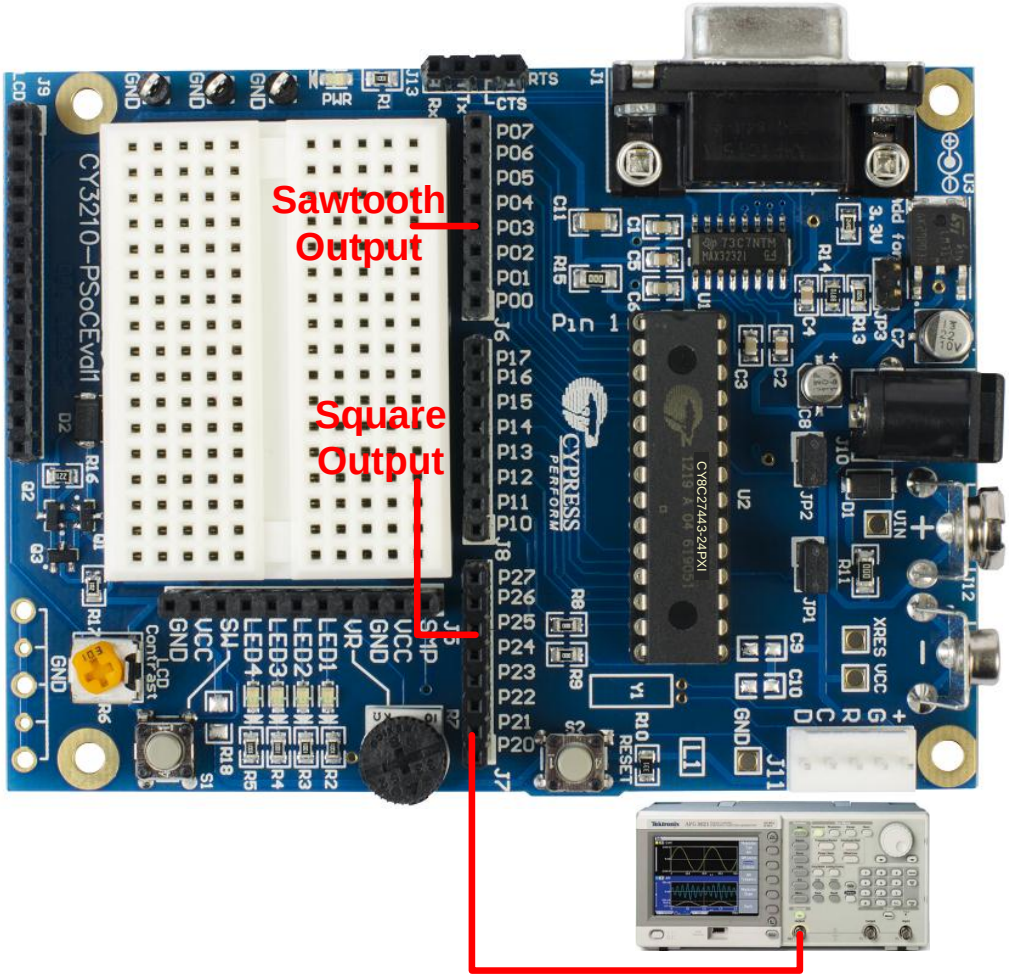
A.2.2 Test Procedure

1. Insert the CY8C27443-24PXI device into the 28-pin IC socket provided on the CY3210-PSoCEval1 board.
2. Program the device using a MiniProg1 or MiniProg3 device with the *AN2161_Integrator_Schmitt_Trigger_Based_VtoF.hex* file available in the root directory of the AN2161_Integrator_Schmitt_Trigger_Based_VtoF project attached with this application note.

3. Apply a sinusoidal input voltage from the function generator or a DC voltage from a power supply to pin P2[1], as shown in Figure 22.

   Note: The input voltage should be greater than 0 V. If the input voltage is less than 0 V, it should be level shifted by referencing the voltage with respect to AGND.

Figure 22. Hardware Connection for Testing Example 2



4. Probe pin P0[3] and pin P2[5] to see the sawtooth and square waveform respectively on the oscilloscope. The output waveform with a sinusoidal input voltage is shown in Figure 16, and the output voltage with a DC input voltage is shown in Figure 15.

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1513644	YARD_UKR	11/02/2007	New application note.
*A	3208958	BIOL_UKR	03/28/2011	Chip, boot.tpl, and UM versions updated.
*B	4383738	DCHE	05/19/2014	Sunset Review. Updated template.
*C	4856516	DCHE	07/28/2015	Merged AN58469 with this AN. Projects updated to PD5.4 SP1.

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