AN214945

PCB Layout Guidelines and Component Selection for Optimized PMU Performance

Associated Part Family: CYW4334

This application note describes Printed Circuit Board (PCB) component selection and layout to optimize Power Management Unit (PMU) performance for the Cypress CYW4334.

Contents

1 About This Document

The document covers the following PMU components:

- CBUCK
- LDO3P3
- CLDO
- LNLDO
- HSICLDO
- BT_PAVDD/BT_LDO_OUT

1.1 Purpose and Audience

This application note provides examples, guidelines, and requirements to help board designers do the following:

- Facilitate optimal board routing and chip performance
- Address noise coupling/electromagnetic interference (EMI) current-flow capability and PMU performance
- Understand the tradeoffs in PMU component selection (differing footprints and ratings) and the implications to overall PMU functionality and performance

The document includes information about the following CYW4334 packages:

- WLCSP (BCM94334CSPAGB)
- WLBGA (BCM94334WLAGB)

1.2 Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM4334	CYW4334

1.3 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

3 WLCSP Board Layout Design Guidelines

3.1 Component Selection and Placement

Table 2 identifies components and recommended placement in relation to their respective regulator pins. The reference designators refer to the BCM94334cspagb reference design.

Table 2. WLCSP Components

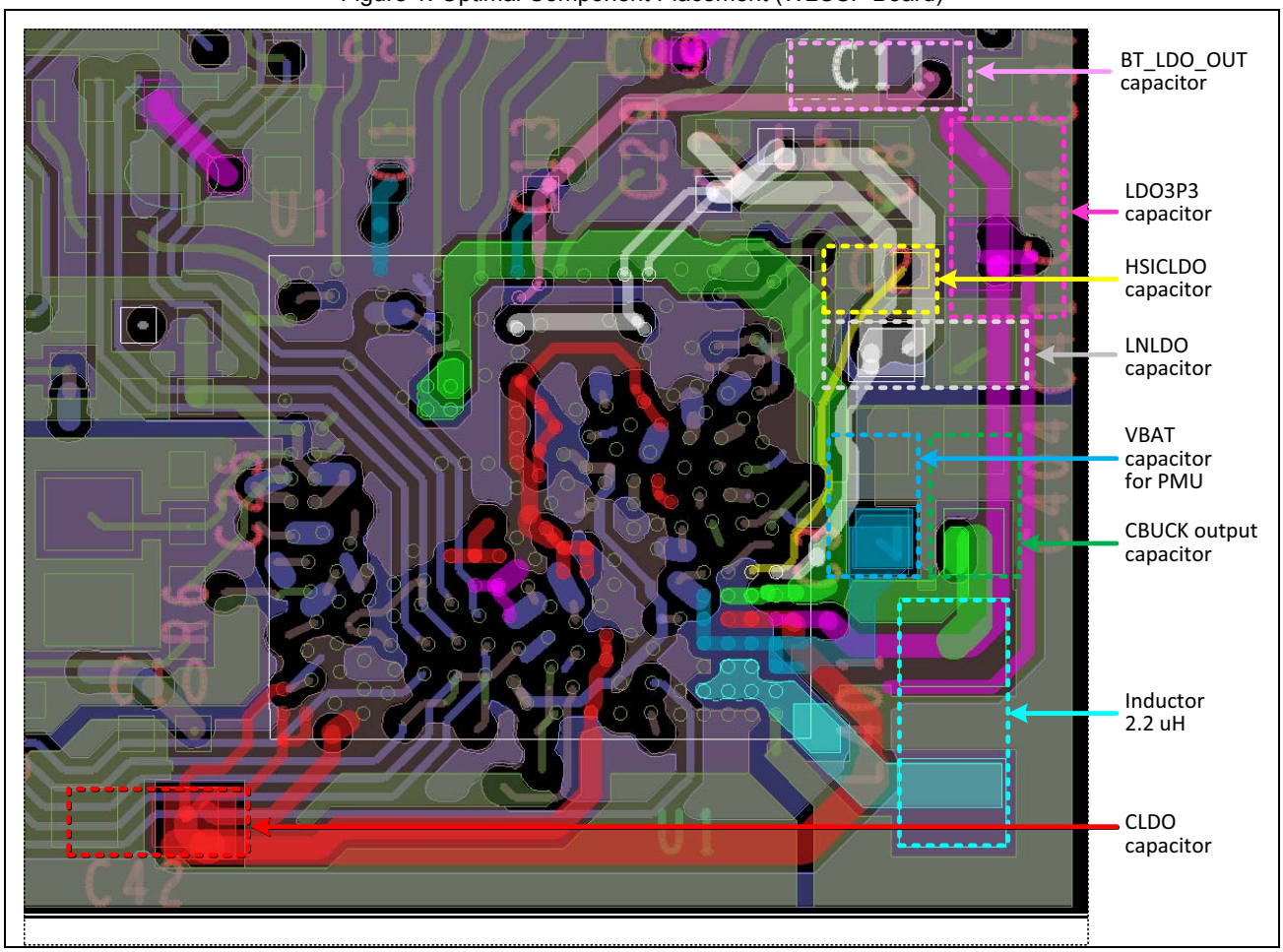
Reference Designator	Package Size (inches)	Component
L401	**0603**	SR_VLX pin driving CBUCK inductor
C404	**0402**	VBAT shared capacitor for SR_VDDBATP5V and SR_VDDBATA5V pins
C3	**0402**	CBUCK output capacitor
C42	**0402**	VOUT_CLDO capacitor
C41	**0402**	VOUT_LNLDO capacitor
C44	**0402**	VOUT_3P3 capacitor
C2	**0201**	VOUT_HSICLDO capacitor
C11	**0402**	BT_LDO_OUT capacitor

Note: For a complete list of PMU components, contact your Cypress representative for the BCM94334cspagb reference design package.

3.2 Optimal Component Placement for Board Routing

Figure 1 shows the optimal PMU-related component placement for the WLCSP reference board BCM94334cspagb). The dotted outlines indicate the component placement, color-coded to match the corresponding routing. The layout places the components near their connecting pins to route with minimal trace lengths.

Figure 1. Optimal Component Placement (WLCSP Board)



4 PMU Board Routing Requirements: WLCSP Board

Figure 2 and Table 3 describe top-layer routing and trace requirements for the components outlined in Figure 3.

Figure 2. PMU Component Routing (WLCSP Board)

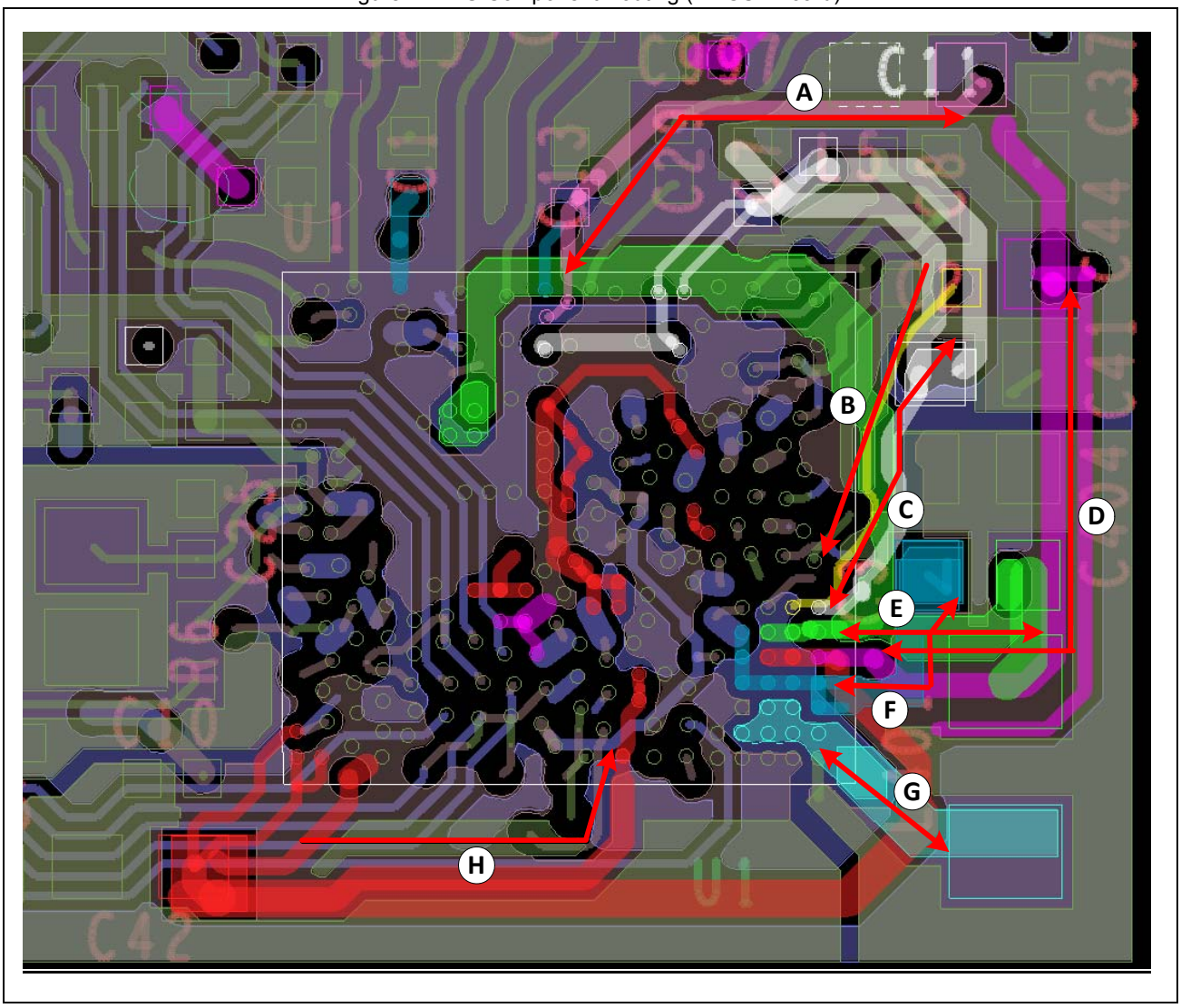


Table 3. PMU Component Routing Trace Requirements (WLCSP Board)

Figure Marker	Description	Trace Specifications (mils)	
		Length	Width
A	BT_LDO_OUT	< 100	≥ 10
B	HSICLDO[a]	< 100	≥ 10
C	LNLDO	< 100	≥ 10
D	LDO3P3	< 100	≥ 10
E	CBUCK capacitor to pin	< 60	≥ 15
F	VBAT capacitor to pin	< 40	≥ 15
G	Inductor to pin	< 100	≥ 15
H	CLDO capacitor to pin	< 100	≥ 10

a.HSICLDO must be routed from capacitor to pin using L1 and L2 traces only. Using layers deeper than L1 and L2 require a taller via stack, which increases via inductance and degrades HSIC jitter performance.

Using vias and routing layers other than the top layer is strongly discouraged due to the following:

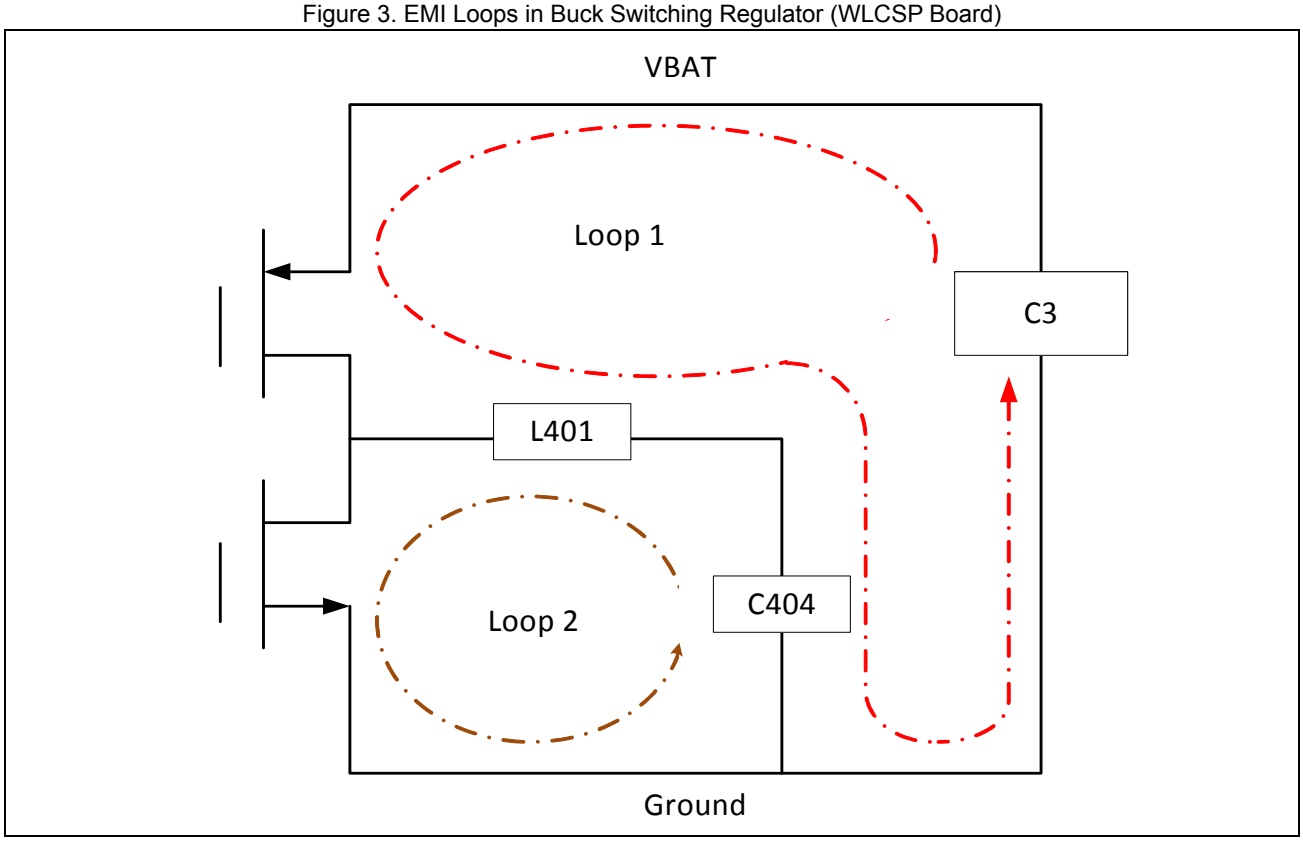
- Microvias have lower current carrying capability:
  - The VLX signal and inductor must carry up to 500 mADC with a ripple of 800 mA pk-pk.
  - The VBAT supply carries a maximum of 600 mA of combined average current for CBUCK /LDO3P3.
  - LDO3P3 sources a maximum of 50 mA. The CLDO maximum is 150 mA. The LNLDO maximum is 104 mA. The HSICLDO maximum is 80 mA. The BT_LDO_OUT maximum is 125 mA.
- Microvias have high parasitic resistance and inductances. These additional parasitics add to power losses and higher switching noise spikes, causing interference.
- Using microvias and lower layers increases the CBUCK switching loop area. This area is directly proportional to radiated EMI (see Figure on page 6).

In Figure on page 5, all of the routings are the shortest and widest possible to minimize parasitic resistance and inductances. Regulators are sensitive to routing parasitics, which can cause instability and power efficiency losses. In extreme cases, routing parasitics may even cause the loss of voltage regulation. Extreme parasitics caused by extended and slender traces can also create large switching voltage spikes, which in turn can lead to long-term chip reliability problems.

5 EMI Loops in the CBUCK Switching Regulator

Do not route sensitive signals through the areas bounded by the two loops that go through the power MOSFETs of the CBUCK, as shown in Figure . Each loop starts at a capacitor and ends at its ground terminal. The area within each loop is proportional to the radiated EMI.

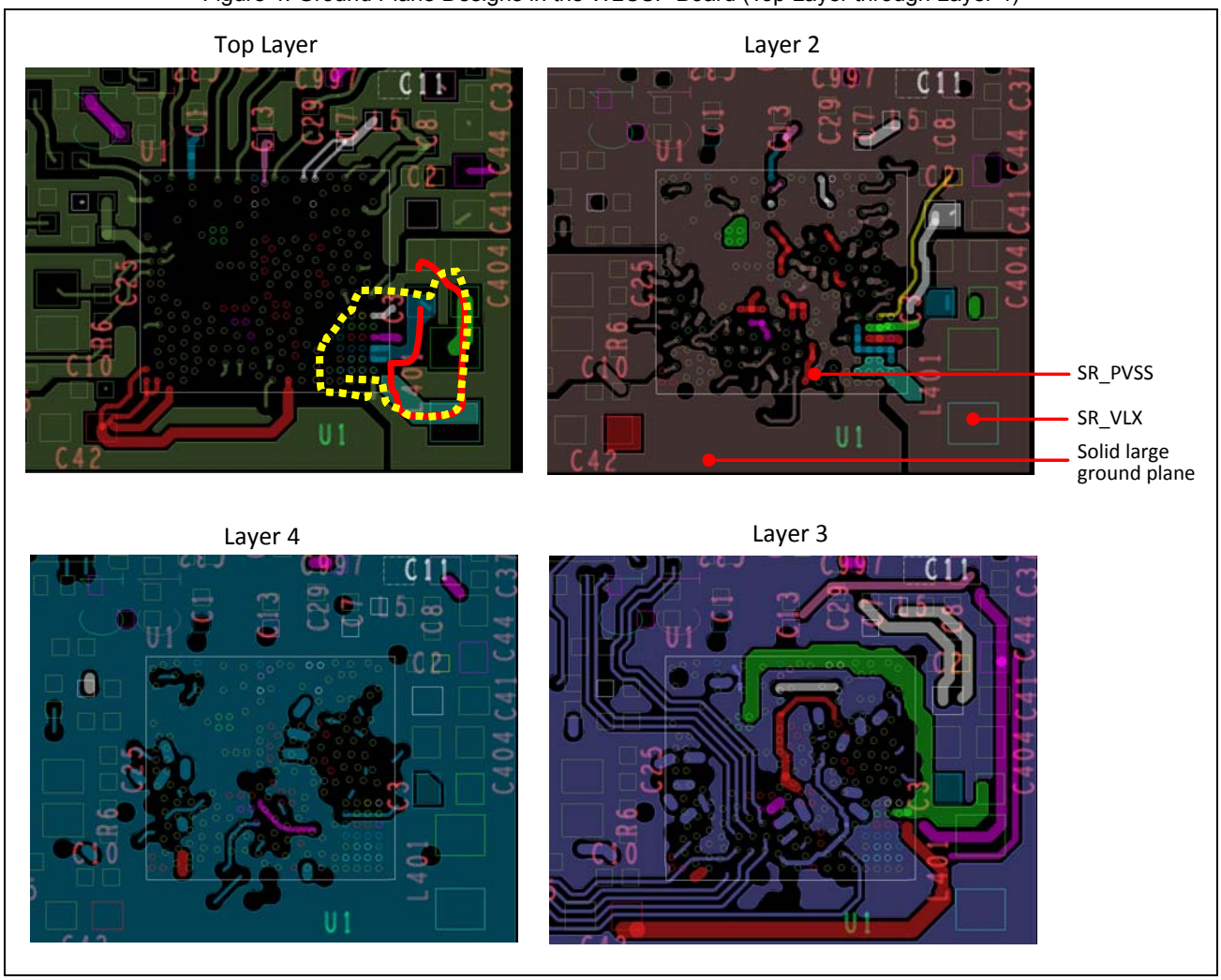
Figure 3. EMI Loops in Buck Switching Regulator (WLCSP Board)



6 Ground Plane Designs

Figure 4 shows how the four topmost layers are used around the PMU. The top layer (top left of the figure) shows the loops outlined in Figure on page 6: Loop 1 is shown as the red line, and Loop 2 is shown as the yellow dotted line.

Figure 4. Ground Plane Designs in the WLCSP Board (Top Layer through Layer 4)



Layer 2 is a solid large ground plane that covers most of the layer (top right in Figure). This layer connects all of the ground pins, including SR_PVSS (the CBUCK power ground pin). The layer is designed to contain noise in the area within Loops 1 and 2. The SR_VLX trace from pin SR_VLX to L401 (SR_VLX pin driving the CBUCK inductor) runs on top of the Layer 2 ground layer to mirror the ground return path in Loop 2.

The ground island under L401 on Layer 2 is densely populated by vias. These vias connect to another ground layer on Layer 3 and, finally, to the main ground plane on Layer 4 (bottom left in Figure on page 7). The vias can carry up to 500 mA of total current. Therefore, many vias must be used to reduce inductances and to avoid ringing on the SR_PVSS pin during CBUCK switching.

Figure shows grounding on the top layer covering the L401 inductor footprint and the regulator caps. This is to enable maximum ground coverage for the PMU and to allow more vias for the top layer ground plane to the underlying main ground plane.

Figure 5. Top Layer Grounding and Use of Ground Vias (WLCSP Board)

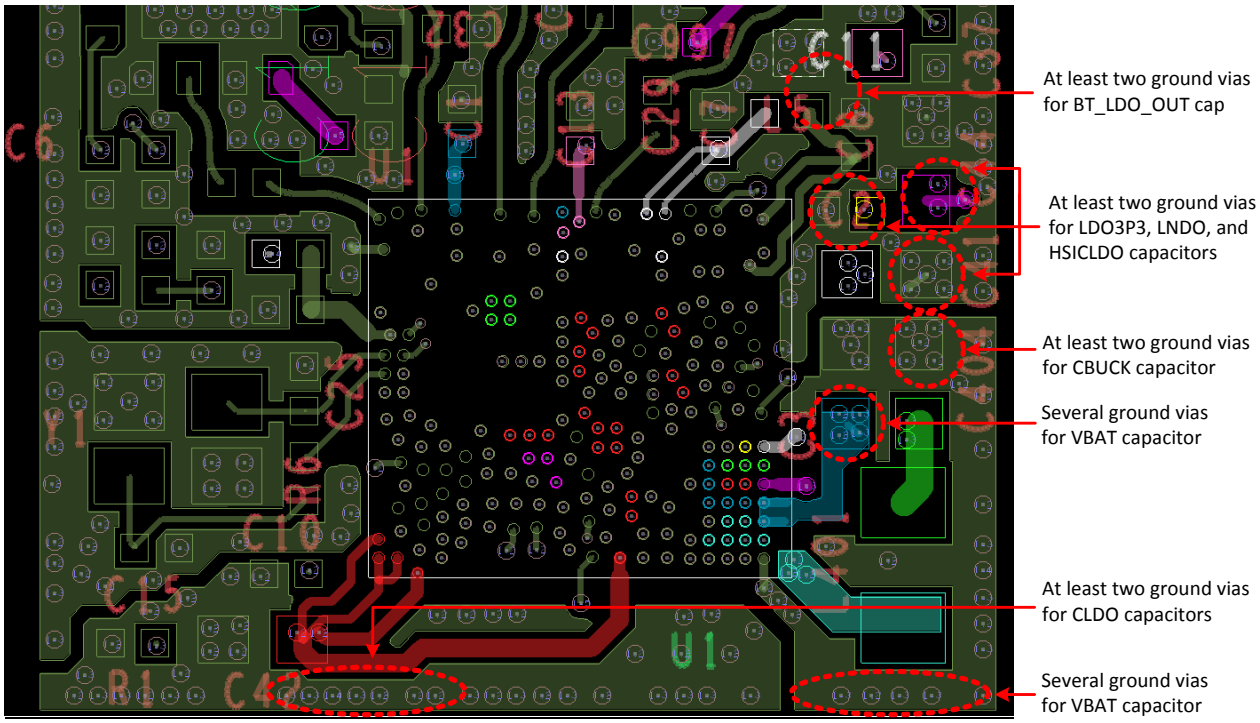
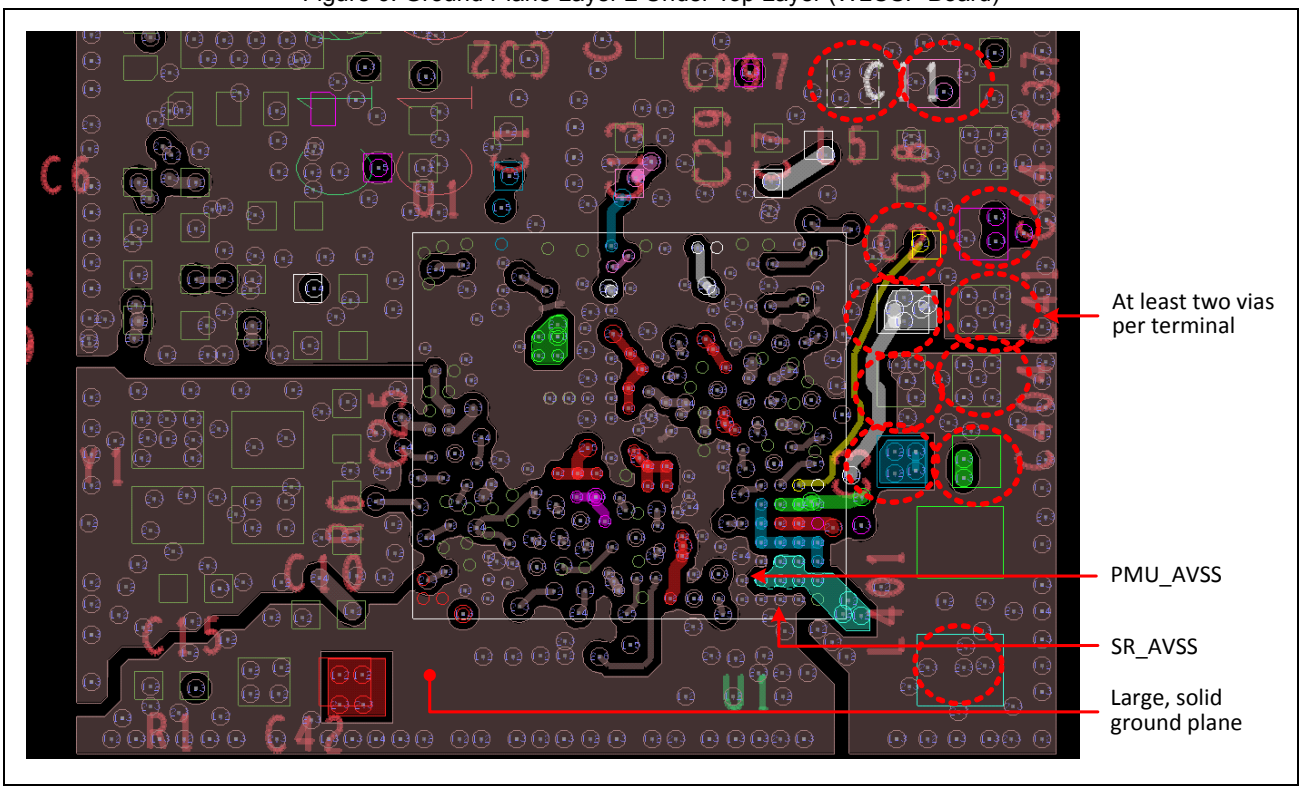


Figure shows Layer 2 with microvias added. The ground island under inductor L401 is populated with multiple vias for a good, low-parasitic connection to the ground plane on the lower layers. Also, all PMU capacitor terminals are connected by at least two vias per terminal for low-parasitic connections to the main ground plane.

Figure 6. Ground Plane Layer 2 Under Top Layer (WLCSP Board)



Layer 2 is the primary ground plane for PMU-related grounds (SR_PVSS and PMU_AVSS). Layer 2 is a large, solid ground plane (shown in brown) and is able to contain noisy signals while providing a low impedance return path for high PMU currents to respective grounds (SR_PVSS and PMU_AVSS).

7 WLBGA Board Layout Design Guidelines

7.1 Component Selection and Placement

Table 4 identifies components and recommended placements in relation to their respective regulator pins for the BCM94334cspagb reference design package. The reference designators refer to the BCM94334wlagb reference design.

Table 4. WLBGA Components

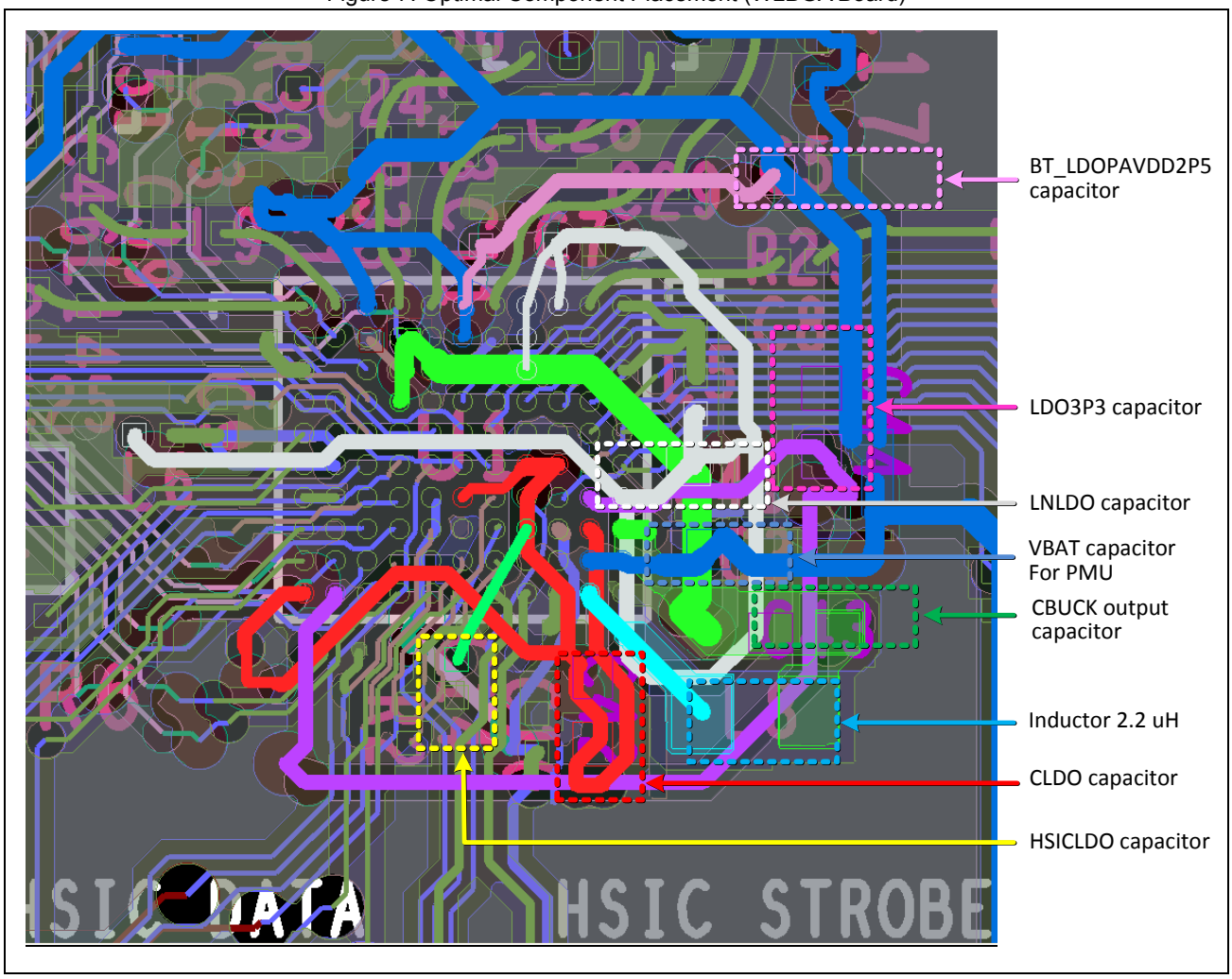
Reference Designator	Package Size (inches)	Component
L8	**0603**	SR_VLX pin driving CBUCK inductor
C43	**0402**	VBAT shared capacitor for SR_VDDBATP5V and SR_VDDBATA5V pins
C3	**0402**	CBUCK output capacitor
C42	**0402**	VOUT_CLDO capacitor
C41	**0402**	VOUT_LNLDO capacitor
C44	**0402**	VOUT_3P3 capacitor
C14	**0201**	VOUT_HSICLDO capacitor
C5	**0402**	BT_LDOPAVDD2P5 capacitor

Note: For a complete list of PMU components, contact your Cypress representative for the recommended BOM.

7.2 Optimal PMU Component Placement for Board Routing

Figure 7 shows the optimal PMU-related component placement for the WLBGA reference board (BCM94334wlagb). The dotted outlines indicate the component placement, color-coded to match the corresponding routing. The layout places the components near their connecting pins to route with minimal trace lengths.

Figure 7. Optimal Component Placement (WLBGA Board)



7.3 PMU Board Routing Requirements: WLBGA Board

Figure 8 and Table 5 on page 11 describe top-layer routing and trace requirements for the components outlined in Figure .9.

Figure 8. PMU Component Routing (WLBGA Board)

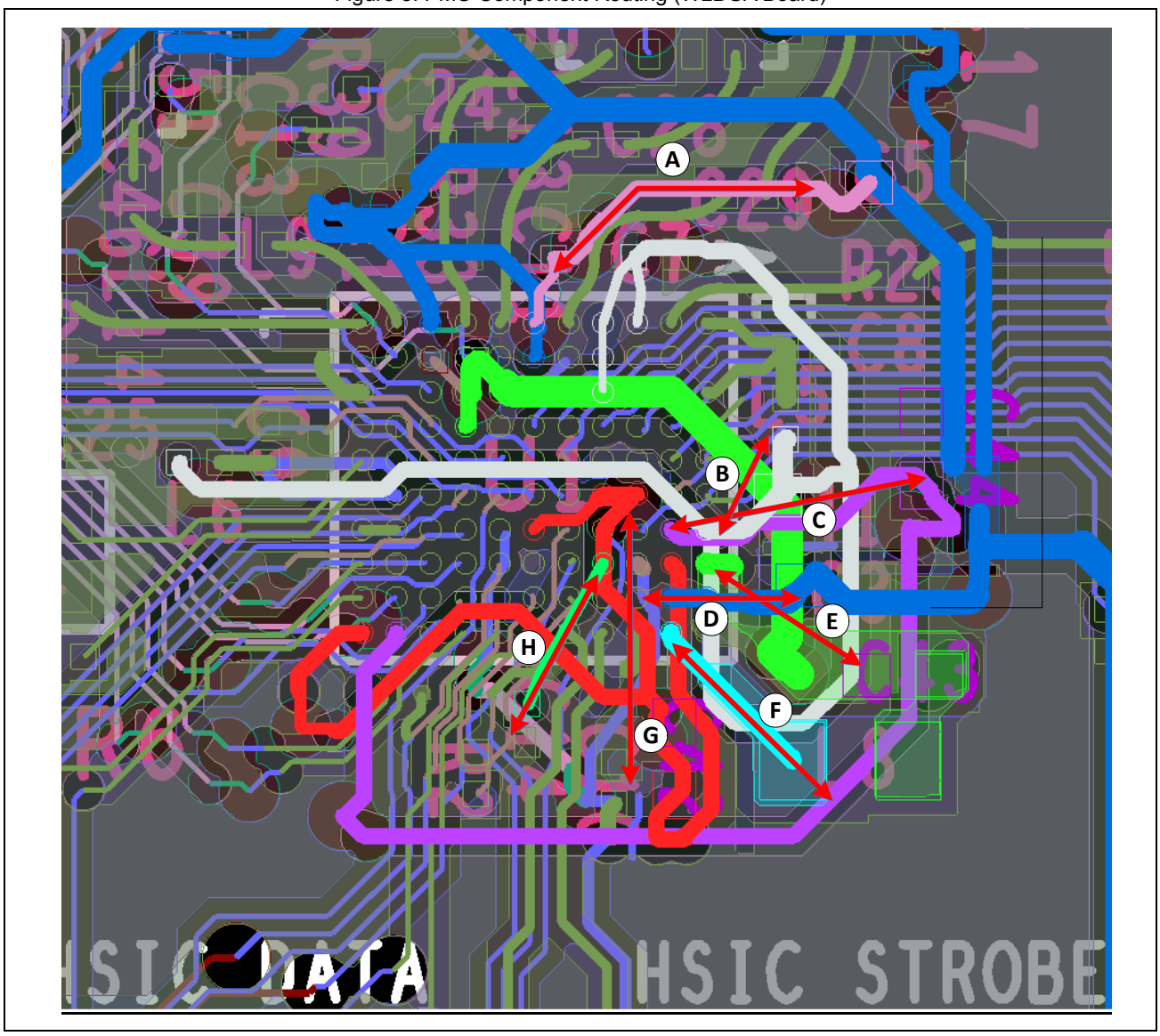


Table 5. PMU Component Routing Trace Requirements (WLBGA Board)

Figure Marker	Description	Trace Specifications (mils)	
		Length	Width
A	BT_LDOPAVDD2P5	< 100	≥ 10
B	LNLDO	< 40	≥ 10
C	LDO3P3	< 100	≥ 10
D	VBAT capacitor to pin	< 60	≥ 15
E	CBUCK capacitor to pin	< 40	≥ 15
F	Inductor to pin	< 80	≥ 15
G	CLDO capacitor to pin	< 100	≥ 10
H	HSICLDO[a]	< 100	≥ 10

a.HSICLDO must be routed from capacitor to pin using L1 and L2 traces only. Using layers deeper than L1 and L2 requires a taller via stack, which increases via inductance and degrades HSIC jitter performance.

The use of vias and routing layers other than the top layer is strongly discouraged due to the following:

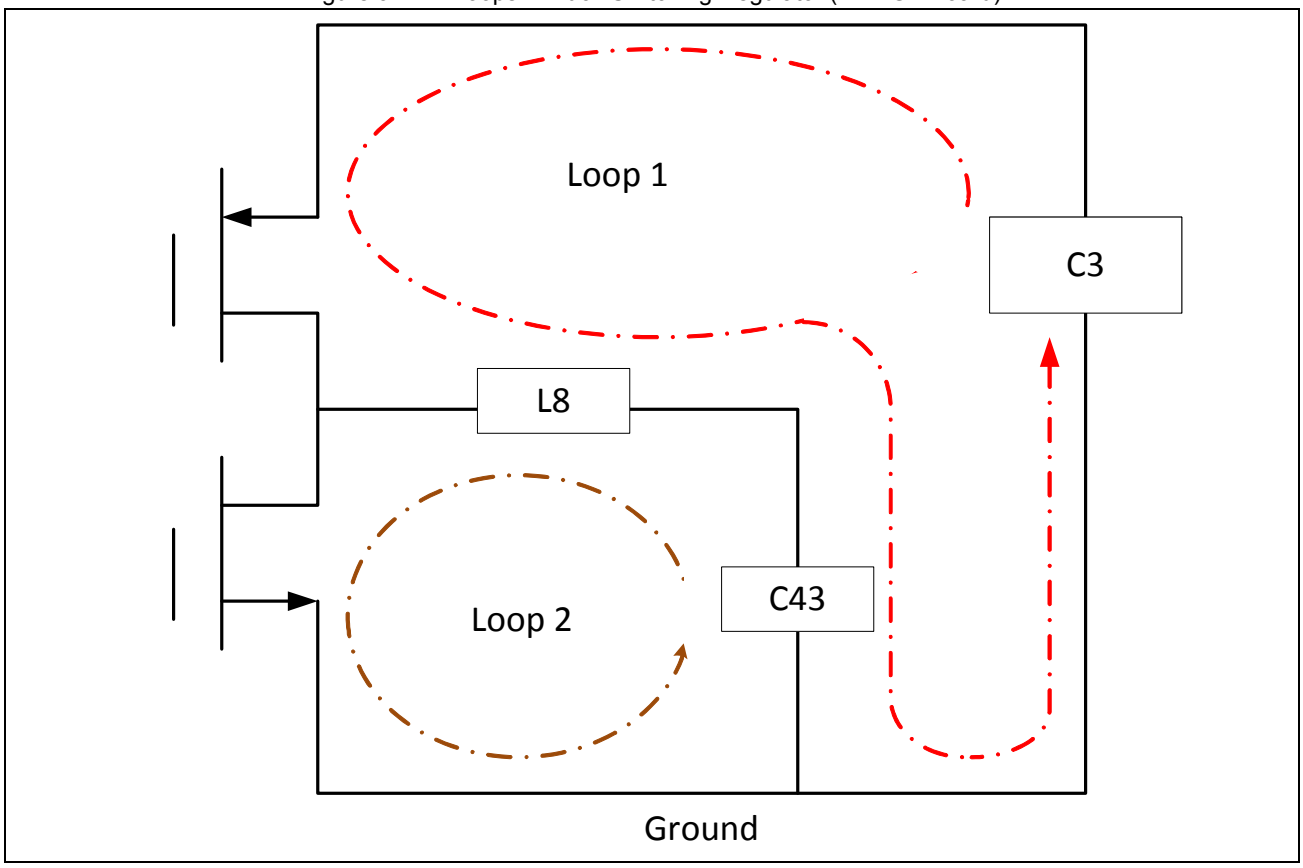
- Microvias have lower current carrying capability:
  - The VLX signal and inductor must carry up to 500 mADC with a ripple of 800 mA pk-pk.
  - The VBAT supply carries a maximum of 600 mA of combined average current for CBUCK /LDO3P3.
  - LDO3P3 sources a maximum of 50 mA. The CLDO maximum is 150 mA. The LNLDO maximum is 104 mA. The HSICLDO maximum is 80 mA. The BT_LDO_OUT maximum is 125 mA.
- Microvias have high parasitic resistance and inductances. These additional parasitics add to power losses and higher switching noise spikes, causing interference.
- Using microvias and lower layers increases the CBUCK switching loop area. This area is directly proportional to radiated EMI (see Figure on page 11).

In Figure on page 11, all the routings are the shortest and widest possible in order to minimize parasitic resistance and inductances. Regulators are sensitive to routing parasitics, which can cause instability, power efficiency losses, and, in extreme cases, may cause the loss of voltage regulation. Extreme parasitics due to extended and slender traces can also create large switching voltage spikes, which in turn can lead to long-term chip reliability problems.

7.4 EMI Loops in the CBUCK Switching Regulator

Do not route sensitive signals through the areas bounded by the two loops that go through the power MOSFETs of the CBUCK, as shown in Figure . Each loop starts at a capacitor and ends at its ground terminal. The area within each loop is proportional to the EMI. Routing of sensitive signals through the areas bounded by these two loops should be strictly avoided.

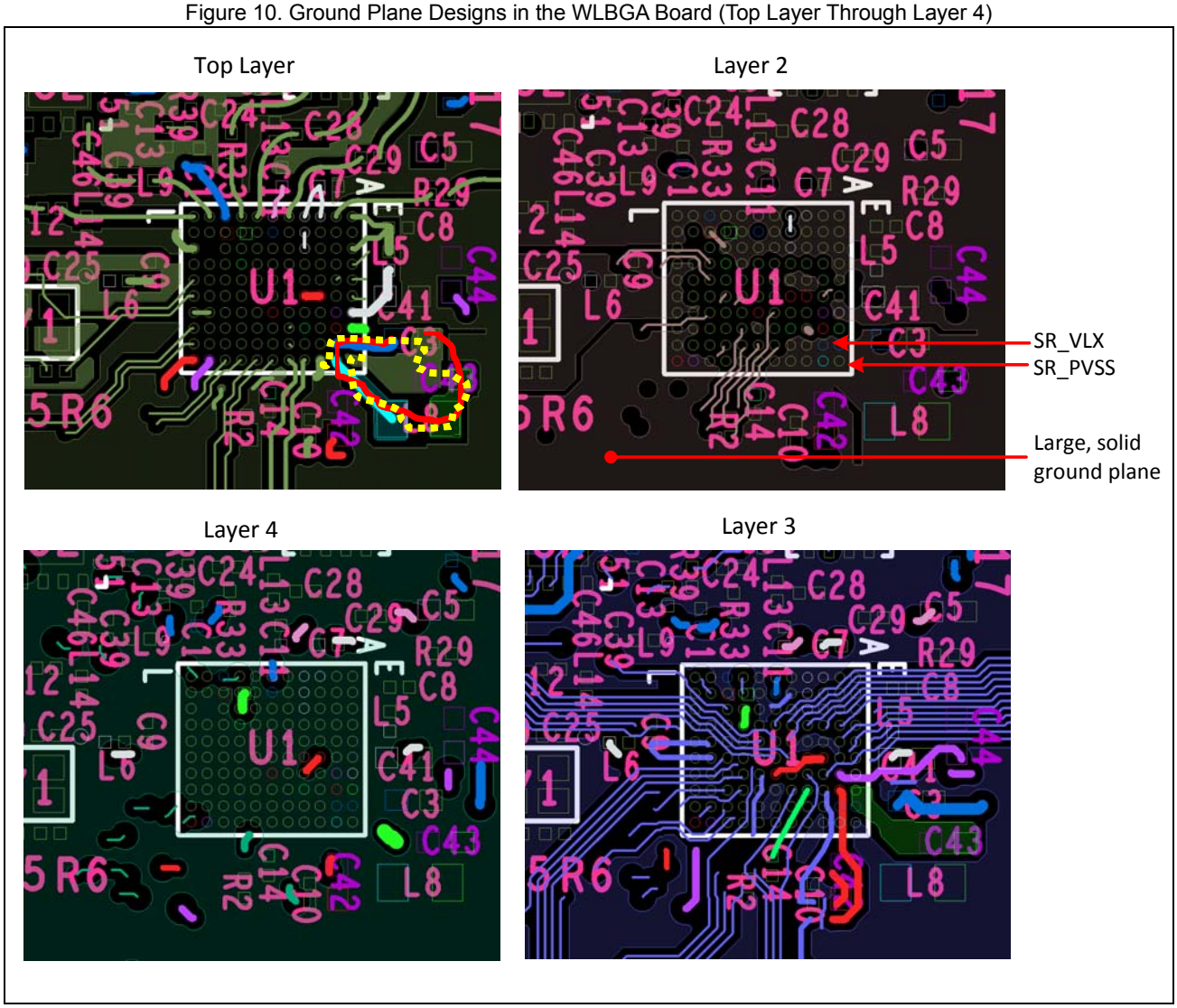
Figure 9. EMI Loops in Buck Switching Regulator (WLBGA Board)



8 Ground Plane Designs

Figure shows how the four topmost layers are used around the PMU. The top layer (top-left in the figure) shows the loops outlined in Figure on page 12: Loop 1 is shown as a red line, and Loop 2 is shown as a yellow dotted line.

Figure 10. Ground Plane Designs in the WLBGA Board (Top Layer Through Layer 4)



Layer 2 is a solid large ground plane that covers most of the layer (top-right in Figure). This layer connects all of the ground pins, including SR_PVSS (the CBUCK power ground pin). It serves the function of containing noise in the area within Loop 1 and Loop 2. The SR_VLX trace from pin SR_VLX to L8 (SR_VLX pin driving the CBUCK inductor) runs on top of the Layer 2 ground layer to mirror the ground return path in Loop 2.

The ground island under L8 on Layer 2 is densely populated with vias (see Figure on page 8). These vias connect to another ground layer on Layer 3 and, finally, to the main ground plane on Layer 4 (bottom left in Figure on page 13). The vias can carry up to 500 mA of total current. Thus, many vias must be used to reduce inductances and to avoid ringing on the SR_PVSS pin during CBUCK switching.

Figure shows grounding on the top layer covering the L8 inductor footprint and the regulator caps. This is to enable maximum ground coverage for the PMU and to allow more vias for the top layer ground plane to the underlying main ground plane.

Figure 11. Top Layer Grounding and Use of Ground Vias (WLBGA Board)

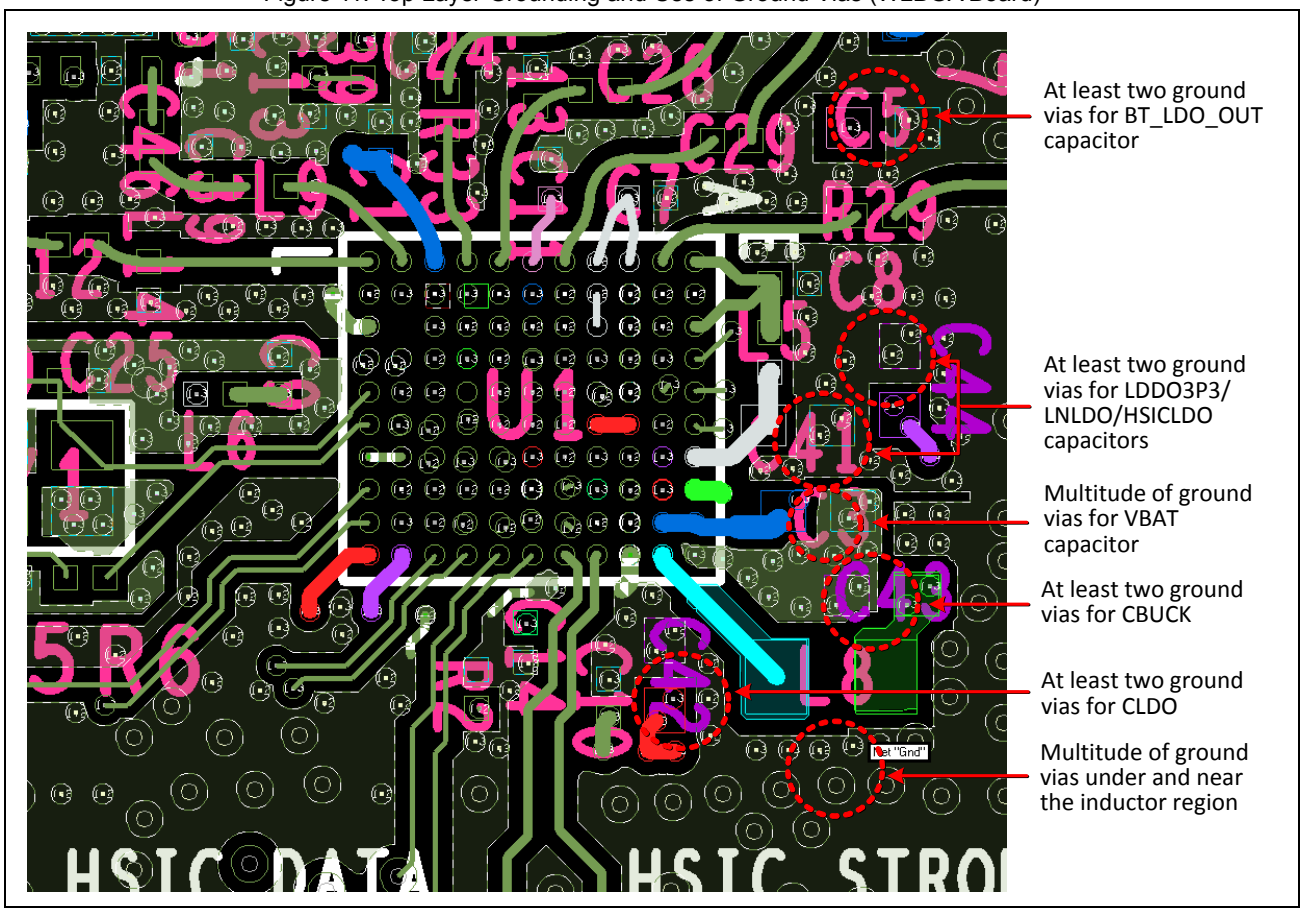
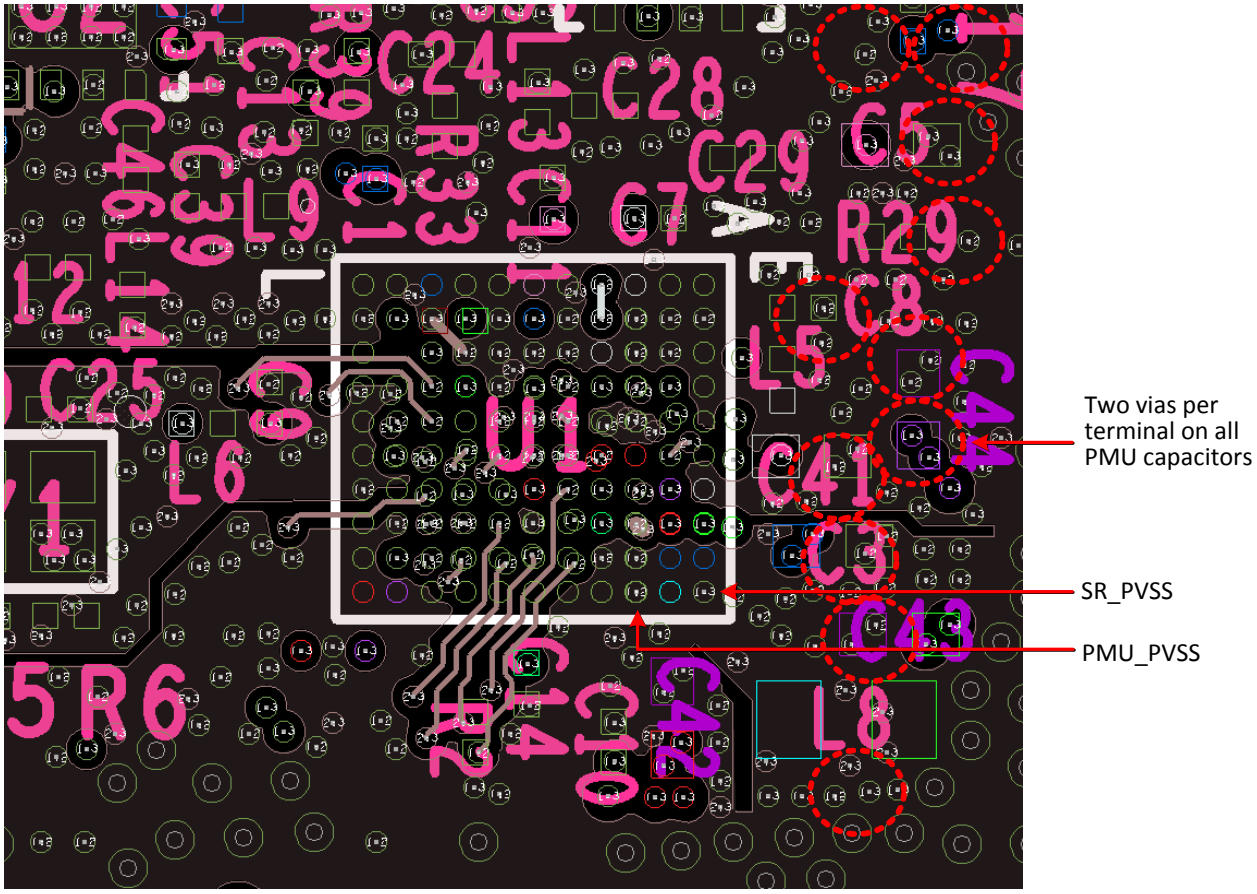


Figure shows Layer 2 with microvias added. The ground island under inductor L8 is populated with multiple vias for a good low-parasitic connection to the ground plane on the lower layers. Also, all PMU capacitor terminals are connected by at least two vias per terminal for low parasitic connections to the main ground plane.

Figure 12. Ground Plane Layer 2 Under Top Layer (WLBGA Board)



Layer 2 is the primary ground plane for PMU-related grounds (SR_PVSS and PMU_AVSS). Layer 2 is a large, solid ground plane (shown in brown) and is able to contain noisy signals while providing a low impedance return path for high PMU currents to respective grounds (SR_PVSS and PMU_AVSS).

9 PMU Component Selection

9.1 Component Variations

Components that typically have similar ratings may not function equally due to differing transient characteristics that cannot be comprehensively defined by component ratings alone.

Contact your Cypress PMU team for alternative component selections.

Cypress strongly advises designers to use only the recommended PMU components, because these components have been thoroughly validated in system characterizations.

9.2 Capacitors

Multilayer ceramic chip (MLCC) capacitors have the following characteristics and limitations:

- Part-to-part tolerance
- Capacitance droop under DC-voltage bias conditions
- Capacitance variation under temperature change (X5R)
- Aging effects

9.2.1 Minimum Capacitance

The minimum capacitance (minC) for each regulator is the minimum design limit needed to ensure basic regulator stability. Using capacitors that drop below the minC values may cause regulators to oscillate. This minC rule is absolute.

Cypress also recommends adding a safety margin to the minC to ensure good transient stability and noise performance.

Customers using capacitors outside of Cypress's recommended BOM list are strongly advised to consult their respective capacitor vendors about how to calculate the minimum capacitance caused by combined effect of all the following factors:

- Capacitance droop under DC-voltage bias: this is the most important factor to check in every capacitor.
- Part-to-part tolerance: ±10% is better than ±20%.
- Capacitance variation under temperature change (X5R): the default for X5R is ±15% capacitance change over a temperature range of –55°C to 85°C.
- Aging effects: Typical for X5R MLCC capacitors (10% drop in 100,000 hours)

There is no standard way of calculating the combined effect of the four minC factors listed; consult capacitor vendors for their preferred way of calculating these factors.

For capacitors that do not appear on the list of Cypress-recommended capacitors, the following formula can be used as a guide:

minC = TypC × (1 –Partol) × (1 – DCBias) × (1 – TempCo) × (1 – Aging)

where:

TypC is typical capacitance.

Partol is part-to-part tolerance (0.2 means ±20%).

DCBias is the mount of drop from TypC at target voltage (0.2 means a 20% drop).

Target voltage is the default voltage of regulator output.

TempCo is the capacitor variation over X5R range, –55°C to 85°C. (±15% = a TempCo of 0.15).

Aging is the amount of capacitor drop over time (a 10% drop in 100,000 hours = Aging of 0.1).

Note: his formula is only a guide. The capacitor manufacturer must guarantee the minimum capacitance value over large volume. Avoid using any capacitor if either of the following apply:

- The manufacturer's calculated capacitance for the part is lower than the minC for a regulator.
- The manufacturer cannot guarantee minC over volume.

9.2.2 Capacitance Recommendations

9.2.2.1 CBUCK Output Capacitance

The nominal CBUCK output capacitance value is 4.7 µF. The following rules apply:

- Effective capacitance must not drop more than 27% from nominal value under 1.5V bias.
- The minC is 2 µF.

Table 6 outlines the recommended capacitors for the CBUCK Output.

Table 6. Recommended Capacitors for CBUCK Output

Part	Manufacturer	Package size (inches)	Description
GRM188R60J475ME84D	Murata	0603	X5R 4.7 µF 20% 6.3V
GRM188R60J475ME19D	Murata	0603	X5R 4.7 µF 20% 6.3V
GRM188R61A475KE15	Murata	0603	X5R 4.7 µF 20% 10V
GRM155R60J475ME87D	Murata	0402	X5R 4.7 µF 20% 6.3V

9.2.2.2 SR_VDDBATP5V and SR_VDDBATA5V Shared Capacitance

The nominal SR_VDDBATP5V and SR_VDDBATA5V shared capacitance value is 4.7 µF. The following rules apply:

- Effective capacitance must not drop more than 80% from nominal value at 5.5V bias. Effective capacitance must not drop more than 73% from nominal value at 4.3V bias.
- For good VBAT, noise suppression is 1.2 µF at the 4.2V bat (voltage on the phone battery) level.

Table 7 outlines the recommended capacitors for the SR_VDDBATP5V and SR_VDDBATA5V .

Table 7. Recommended Capacitors for SR_VDDBATP5V and SR_VDDBATA5V

Part	Manufacturer	Package size (inches)	Description
GRM188R60J106ME84D	Murata	0603	X5R 10 µF 20% 6.3V
GRM188R60J106ME47D	Murata	0603	X5R 10 µF 20% 6.3V
GRM188R60J475ME84D	Murata	0603	X5R 4.7 µF 20% 6.3V
GRM188R60J475ME19D	Murata	0603	X5R 4.7 µF 20% 6.3V
GRM155R60J475M87D	Murata	0402	X5R 4.7 µF 20% 6.3V

9.2.2.3 CLDO Output Capacitance

The nominal CLDO output capacitance value is 1.0 µF. The following rules apply:

- Effective capacitance must not drop more than 10% from nominal value under 1.25V bias.
- The minC is 0.67 µF.

Table 8 outlines the recommended capacitors for the CLDO output.

Table 8. Recommended Capacitors for CLDO Output

Part	Manufacturer	Package size (inches)	Description
GRM188R60J105MA01	Murata	0603	X5R 1 µF 20% 6.3V
GRM155R60J105KE19D	Murata	0402	X5R 1 µF 10% 6.3V

9.2.2.4 LNLDO1 Output Capacitance

The nominal LNLDO1 output capacitance value is 1.0 µF. The following rules apply:

- Effective capacitance must not drop more than 10% from nominal value under 1.25V bias.
- The minC= is 0.67 µF

Table 9 outlines the recommended capacitors for the LNLDO1 output.

Table 9. Recommended Capacitors for LNLDO1 Output

Part	Manufacturer	Package size (inches)	Description
GRM188R60J105MA01	Murata	0603	X5R 1 µF 20% 6.3V
GRM155R60J105KE19D	Murata	0402	X5R 1 µF 10% 6.3V

9.2.2.5 LDO3P3 Output Capacitance

The nominal LDO3P3 output capacitance value is 1.0 µF. The following rules apply:

- Effective capacitance must not drop more than 30% from nominal value under 3.3V bias.
- The minC= is 0.44 µF.

Table 10 outlines the recommended capacitors for the LDO3P3 output.

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Table 10. Recommended Capacitors for LDO3P3 Output

Part	Manufacturer	Package size (inches)	Description
GRM188R61A105K	Murata	0603	X5R 1.0 µF 10% 10
GRM155R61A105KE15	Murata	0402	X5R 1.0 µF 10% 10V

9.2.2.6 LDO2P5 Output Capacitance

The nominal LDO2P5 output capacitance value is 2.2 µF. The following rules apply:

- Effective capacitance should not drop more than 41% from nominal value under 2.5V bias.
- The minC= is 0.57 µF.

Table 11 outlines the recommended capacitors for the LDO2P5 output.

Table 11. Recommended Capacitors for LDO2P5 Output.

Part	Manufacturer	Package size (inches)	Description
GRM188R61A225KE34	Murata	0603	X5R 2.2µF 10% 10V
GRM155R60J225ME15	Murata	0402	X5R 2.2µF 20% 6.3V

9.3 Inductors

The recommended default inductor for the CYW4334 CBUCK is FDK MIPSTZ1608D2R2B.

Table 12 a list of 0603-inch size inductors qualified to work with the CYW4334 CBUCK.

Table 12. Qualified Inductors

Vendor	*Part*	*0603-inch footprint Max Height (mm)*	*Rated (T<40C) Current mA*	*DCR mΩ*	*DCR tolerance ±%*	*L at 200 mA*	*L at 400 mA*	*Inductance Typical µH*	*tolerance ±%*
Chilisin	***MPA160808T-2R2M-N2A***	***0.95***	***500***	***550***	***30***	***1.7***	***1.35***	***2.2***	***20***
TDK	***MLP1608V2R2B***	***0.95***	***600***	***360***	***30***	***1.6***	***0.91***	***2.2***	***30***
TDK	***MLP1608H2R2B***	***0.95***	***750***	***300***	***30***	***1.4***	***0.8***	***2.2***	***30***
FDK	***MIPSTZ1608D2R2B***	***0.9***	***500***	***390***	***30***	***2***	***1.5***	***2.2***	***30***
Murata	***LQM18PN2R5ND0***	***0.75***	***600***	***240***	***25***	***1***	***0.6***	***2.5***	***30***
TDK	***MLP1608V2R2D***	***0.75***	***550***	***400***	***30***	***1.3***	***0.8333***	***2.2***	***30***

9.3.1 Comparative Criteria Defined

The listed inductors are multilayered and exhibit more dynamic characteristics than wire-wound inductors. The following definitions apply:

- DC Resistance (DCR): DCR contributes to CBUCK conduction power loss. Excessive DCR can lead to as much as a 5% power loss.
- AC Resistance (ACR): ACR contributes to CBUCK switching power loss.
  - ACR must be < 1Ω at 4 MHz under no-load conditions to ensure lower switching losses at low load.
  - ACR at 4 MHz over –40°C to +125°C at 372 mA load must be < 1Ω.
- Saturation current Isat1: Multilayered inductor data sheets typically do not address explicit Isat1 lower current level information.
  - Isat1 is defined as the load current that causes inductance to drop by 30% from nominal value.
  - Excessive drops in inductance can lead to more inductor losses due to increased inductor ripple current through ACR. Increased inductor ripple current can also lead to more switching current injection into ground.
  - For ideal peak PWM efficiency at a 200 mA load point, effective inductance at the 200 mA load level should be 2uH minimum for a nominal part.
- Saturation current Isat2: Isat2 is defined in multilayered data sheets as typically higher than Isat1.
  - Isat2 is defined as the saturation current that causes the inductor to self-heat by +40°C.
  - Isat2 should be 500 mA minimum.
- Inductance under Isat2 versus operating temperature range should be –40°C to +125°C.
  - Inductance must be characterized with Isat2 across the full inductor operating temperature range.
  - The recommended operating temperature range is –40°C to +125°C, inclusive of the inductor self-rise temperature (–40°C).

- The inductor peak operating temperature of +125°C (which includes inductor self-heating at +40°C) corresponds to the customer product temperature maximum of +85°C.
- Inductance must not vary more than +/-4% over the operating temperature range (–40°C to +125°C) above under Isat2.

- Shielding: Cypress highly recommends magnetic shielding, ferrite drum shielding, or magnetic-resin coated shielding to prevent of EMI issues.

9.3.2 Substitution Criteria

Cypress strongly discourages using inductors not listed in Table 12 on page 18. Do not consider such inductors until they have been be assessed by the Cypress PMU team based on the following parameters:

- Inductor part-to-part tolerance: +/–20% or at most +/–30%
- DC Resistance (DCR):
  - DCR versus temperature
- AC Resistance (ACR):
  - ACR versus frequency under no-load, mid-load, and maximum-load conditions.
  - ACR versus frequency under minimum, typical, and maximum operating temperatures at maximum-load.
  - ACR versus 4 MHz ripple current amplitude for no-load and maximum load conditions.
- Isat1: Saturation current based on (nominal inductance –30%).
- Isat2: Saturation current based on +40°C self-heating temperature rise.
- Inductance under Isat2 versus operating temperature range (such as –40°C to +125°C).
- Shielding

Note: All of the comparative criteria listed above must be satisfied before an inductor can be approved for CBUCK suitability.

10 References

The references in this section may be used in conjunction with this document.

Document (or Item) Name		Number	Source
Cypress Items			
[1]	*CYW4334* Data Sheet	4334-DS1xx-R	Cypress Developer Community
[2]	*Wafer-Scale Chip-Sized Package Overview and Assembly Guidelines* Application Note	PACKAGING-AN3xx-R	Cypress Developer Community
[3]	*Wafer-Level Ball Grid Array Overview and Assembly Guidelines* Application Note	PACKAGING-AN6xx-R	Cypress Developer Community
[4]	*Pkg Reflow Process Guidelines for Surface Mount Assemblies* Application Note	PACKAGING-AN1xx-R	Cypress Developer Community
[5]	*Printed Circuit Board Land Pattern Recommendations for Ball Grid Array* Application Note	PACKAGING-AN5xx-R	Cypress Developer Community

Document History Page

Document Title: AN214945 - PCB Layout Guidelines and Component Selection for Optimized PMU Performance Document Number: 002-14945				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	11/01/2011	4334-AN200-R Initial release
*A	–	–	08/01/2012	4334-AN201-R Added: Minimum Capacitance on page 16. Minimum capacitance values for recommended regulator specifications in Capacitance Recommendations on page 16. Updated: Throughout the document, clarified that component package dimensions are in inches. Table 12 on page 18 with additional recommended 0603-sized inductors Changed the Vbat value to 4.2Vbat from 4.3Vbat in SR_VDDBATP5V and SR_VDDBATA5V Shared Capacitance on page 17.
*B	5459506	UTSV	10/19/2016	Updated in Cypress template Added Cypress part numbering scheme
*C	5834576	BENV	07/27/2017	Updated logo and copyright

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